UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Sede Amministrativa: Università degli Studi di Padova

Sede Consorziata: Università degli Studi di Trieste

Dipartimento di Ingegneria Elettrica

SCUOLA DI DOTTORATO DI RICERCA IN : INGEGNERIA INDUSTRIALE

INDIRIZZO: INGEGNERIA ELETTROTECNICA

CICLO XXIV

REAL-TIME APPLICATIONS FOR ELECTRIC POWER GENERATION AND CONTROL

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31 Gennaio 2012

To Sabina, Giovanni and Elisabetta.

Abstract

Sommario.

Il controllo dei sistemi elettrici di potenza ha per scopo la fornitura di energia agli utilizzatori (carichi) garantendo una adeguata qualità malgrado le continue variazioni di topologia, le variazioni nella generazione e le fluttuazioni dei carichi che avvengono nel sistema stesso.

Questa tesi riguarda il problema della regolazione di uno tra i principali parametri che determina la qualità del servizio fornito: la tensione a cui l'energia viene fornita.

Una eventuale definizione di adeguata qualità è fuori dagli scopi del lavoro.

Molti dispositivi atti a regolare il valore della tensione in diverse parti del sistema sono stati sviluppati nel corso degli anni. In questa tesi vengono approfonditi alcuni aspetti dei dispositivi di regolazione della tensione che agiscono attraverso il controllo della potenza reattiva erogata dai generatori.

La regolazione della tensione nei sistemi elettrici è tradizionalmente suddivisa almeno in regolazione primaria, che avviene agendo sulla tensione di eccitazione dei singoli generatori, e regolazione secondaria, con il controllo della potenza reattiva di intere centrali. Entrambe, in ultima analisi, vengono attuate variando la tensione di eccitazione dei generatori sincroni.

In questo lavoro viene presentata una unica piattaforma hardware e software che ha permesso di implementare due dispositivi di controllo digitale:

- un sistema di controllo dell'eccitazione per la regolazione primaria della tensione nei generatori sincroni;
- un sistema di controllo della potenza reattiva per la regolazione secondaria della tensione nelle grandi centrali elettriche. Questo dispositivo è presente nel codice di rete italiano dal 2003 e viene chiamato SART (Sistema Automatico di Regolazione della Tensione).

Questi regolatori di tensione sono nati storicamente come apparati analogici e sono poi stati implementati come sistemi digitali con varie tecnologie. In questa tesi si tratta dell'implementazione di tali sistemi come controlli digitali utilizzando microprocessori e software di elaborazione matematica di uso generale equipaggiati con sistemi operativi di uso generale ma con caratteristiche real-time.

Una tecnica emergente per la prototipizzazione rapida di sistemi di controllo prevede l'utilizzo di strumenti di simulazione di alto livello in cui progettare e simulare il funzionamento dell'impianto e del controllo generando automaticamente il codice del controllo. In questa tesi è presentata e descritta l'applicazione della citata tecnica nell'ambito della produzione e regolazione dell'energia elettrica. I due sistemi di controllo oggetto di questa tesi sono progettati e simulati con un linguaggio di alto livello ed implementati con l'utilizzo di un sistema operativo Linux modificato (RTAI) per avere prestazioni real-time.

In questo lavoro vengono anche presentati i dati sperimentali di alcune sessioni di collaudo dell'apparato SART.

In fase finale è stata indagata la possibilità di utilizzare la piattaforma per sviluppare analoghi dispositivi di regolazione da applicare alla rete di distribuzione. La crescita della generazione di piccola e media taglia all'interno delle reti di distribuzione avvenuta nell'ultimo decennio ed ancora in corso, pone nuove problematiche per la regolazione di tensione. Viene quindi proposto un controllo della tensione per reti di distribuzione, in presenza di generazione distribuita, in cui dispositivi analoghi a quelli presentati per la rete di trasmissione possono trovare utile applicazione.

Summary.

The aim of an electric power control system is to supply electric energy to final users ensuring an adequate quality regardless to the constant changes in network topology, the variations in generation and the load fluctuations within the system itself.

This dissertation deals with the control aspects of one of the main parameters involved in the quality of the service provided: the voltage value energy is supplied.

It is herewith not intended to look at the definition of adequate quality of energy.

Over the years several devices have been developed to control the voltage value in different parts of the power system. This work aims at studying in deep some of the aspects of the voltage control systems regulating the reactive power absorbed and injected into the network by generators.

Voltage regulation in electrical systems is traditionally divided at primary level by operating on the reactive power of the single generator and by controlling the reactive power of entire power stations at secondary level. Ultimately these regulations are both carried out by varying the current or the excitation voltage in synchronous generators.

This work presents a single hardware and software platform enabling the implementation of two digitally controlled devices:

- a control system controlling the excitation in synchronous generators;
- a system controlling the reactive power of the secondary voltage control in large power plants. This device is prescribed in the Italian network code since 2003 and is called SART (Automatic System for Voltage Regulation).

These voltage regulators were historically born as analog devices and were subsequently implemented as digital controls using various technologies. The central topic of this dissertation is the implementation of the above-mentioned devices as digital control systems using microprocessors and general purpose computing systems, fitted out with operating systems for general use but with real-time characteristics.

An emerging technique to quickly prototype a control system implies the utilization of high level simulation tools to design and simulate the plant to be controlled and automatically generate a control code.

This work presents in detail the above-mentioned technique in the production and regulation of electric energy. The two control systems taken into consideration are designed and simulated using a high-level language and implemented with a modified Linux operating system (RTAI) in order to offer real-time performance. Furthermore, the experimental data of some SART device commissioning sessions are also included.

In conclusion, the possibility of using the same platform for the development of similar voltage control devices to apply in the distribution network was investigated. The growth of little and medium-sized generation units, within the distribution network, which has taken place in the last decade, has introduced new issues in voltage regulation. For this reason a new control strategy was suggested for voltage controlling in distribution networks, where the generation is spread and control devices similar to the ones presented for the transmission network can be applied.

Acknowledgements

Un sentito ringraziamento al mio tutor prof. Giorgio Sulligoi, per la fiducia che ha riposto in me e nelle mie competenze, spero sia stata ripagata dal lavoro svolto. Lo ringrazio per avermi spronato con continuità e con sempre nuovi obiettivi.

E' doveroso anche ringraziare l'Ing. Vittorio Arcidiacono, e' stata una grande fortuna ed un immenso onore poter lavorare al suo fianco.

Un grazie ai sig.ri (Vinc)Enzo Bordonaro, Fabi(ett)o Danini, Roberto Mariani, Fabio(ne) Veschi e Giuseppe Vit per la collaborazione e grande disponibilita' sempre dimostratami.

Un grande aiuto mi è arrivato dall'amico Marino, anche nella veste del prof. Miculan: il suo invito a cogliere l'opportunità offertami è stato decisivo.

A Massimo, Edi, Silvia e Daniela un abbraccio per la pazienza e le correzioni. Un grazie anche a Daniele per la lettura.

Un riconoscente ringraziamento al prof. Furio Honsell per avermi formato prima ed avermi permesso ora di affrancarmi temporaneamente dalla mia principale attività per questa sfida.

Many thanks to Mrs. Elisabetta Salvador and Miss. Sabina Damiani for all the corrections to the manuscript.

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Glossary

ADEOS Adaptive Domain Environment for Operating Systems

API Application Programming Interface

AVR Automatic Voltage Regulator

BVR Busbar Voltage Regulator

COTS Commercial-Off-The-Shelf

CSMA/CA Carrier sense multiple access with collision detect

DCOM Distribuited Component Object Model

DCS Distributed Control System

DG Distributed Generation

DMS Distribution Management Systems

DSP Digital Signal Processor

ECS Excitation Control System

EHV Extra High Voltage

EMS Energy Management System

GPP General Purpose Processor

GRPR Generator Reactive Power Regulators

HMI human-machine interface

HRT Hard Real Time

ISO Independent System Operator

LAN Local Area Networks

MMU Memory Management Unit

OEL Over Excitation Limiter

OLTC On-Line Tap Changers

OPC OLE for Process Control

OPC Open Productivity and Connectivity

OPC UA OPC Unified Architecture

OSI International Standard Organization

PCU Power Control Unit

PLC Programmable Logic Control

POSIX Portable Operating System Interface for Unix

PSS Power System Stabilizer

PVR Primary Voltage Regulation

RPL Reactive Power Level

RTAI Real Time Application Interface

RTOS Real Time Operating System

RVR Regional Voltage Regulator

SCADA Supervisor and Control and Data Acquisition

SVR Secondary Voltage Regulation

TCP Transmission Control Protocol

TDMA Time Division Multiple Access

TVR Tertiary Voltage Regulation

UDP User Datagram Protocol

UEL Under Excitation Limiter

WCET Worst Case Execution Time

1

Introduction

1.1 Objectives

This thesis concerns the use of real-time operating systems aimed at developing control devices to be used in power systems to control the voltage. The real-time performances of some real time operating systems have been compared with the dynamics requested by some voltage control devices used in power systems. Two different control devices have been developed. Simulation and extended experimental results obtained in real commissioning tests are shown. The possibility to use this kind of hardware and software platforms for developing control devices of the new grid (the so called Smart-Grid) is outlined.

1.2 Outline of the thesis

Electrical power systems are often cited as the most complex systems ever made by human being. The topology of an electric power system is continuously affected by changes due to maintenance, developments and also automatic operations. Also generation and loads, that should be continuously and rapidly balanced, fluctuate partially uncontrolled. The quality of the service strongly depends on some quantities (e.g. voltage and frequency) of the energy supplied to the customers while the power system is subject to a wide range of electromechanical and electromagnetic phenomena.

The voltage at fundamental frequency is a particularly important issue because any deviation from the nominal voltage to the supplied consumers can deteriorate their performance and continuity. Several electromechanical and electronic equipments require the voltage to be kept within a small range of variability around a nominal value. The complexity is traditionally

managed with a decomposition approach. Therefore the voltage problem is split on a geographical criteria separating the high voltage network from medium and low voltage networks and subdividing the high voltages network itself in different areas weakly coupled. The voltage problem is also decomposed with a time-horizon criteria according with the dynamics of the subsystem under consideration.

In chapter 2 the problem of voltage control is presented. The aim of this chapter is to describe the main characteristics of the control problems in which the developed devices have been applied. The focus will be on the voltage control through the reactive power control. In transmission system it can be shown how the voltage amplitudes strongly depend on the reactive power flow and are weakly coupled to active power flows. Different levels of control will be presented together with their dynamic characteristics: a primary voltage control through generators excitation control systems characterized by a dominant time constant (closed loop) of about 0.5-1 s, the reactive power control loops of the power stations characterized by a dominant time constant (closed loop) of about 5-10 s and grid pilot nodes voltages control loops characterized by a dominant time constant (closed loop) of about 50 s or higher.

These controls require an ever growing set of functionalities and flexibility to be integrated in complex control centers and therefore an emerging development strategy is to use general purposes processors endowed with a complete operating system with real-time performance. In chapter 3 a review on RTOS (Real Time Operating System) proceed specific performance analysis of RTAI (a Linux based RTOS) and comparisons among RTAI and other commonly used RTOSs. Comparisons and performance analysis are focused on applications, therefore the main parameter considered is the jitter of scheduling time. One of the advantages in using a complete RTOS concerns the communication features offered by these OSs. Some consideration on communication are outlined in chapter 4.

The proposed platform based on RTAI was used in order to develop two real-time control devices: a control excitation system for synchronous generators is presented in chapter 5 and a reactive control system used in secondary voltage control is described in chapter 6.

These two applications concern mainly the transmission system but new issue is arising in distribution systems: the connection of small size generators mainly to the medium and low voltage networks. The so called embedded or distributed generation introduces new challenges in voltage control. In chapter 7 the problem of voltage rise in distribution network in presence of distributed generation is reviewed and a new control strategy is presented and simulation results are shown. The implementation of this strategy is outlined with a kind of devices very

similar to those previously presented and therefore the technology presented is shown suitable for the architecture of the new grid.

2

Voltage Control

2.1 Introduction

Some aspects of power systems complexity and the decomposition of the control problem typically applied are introduced. The control issues treated in this work are then summarized. Requirements for the control devices bandwidth are drawn.

2.2 Complexity of power systems

An electric power system normally encompasses a very high number of machinery and devices and hence of physical quantities. It is essentially devoted to produce energy, transfer the produced energy near to consumers and distribute it to each one of the different users (called loads) at any moment and with the required quality (e.g. guaranteed frequency and voltage)[1].

This rough description has a precise counterpart in the physical structure of power systems: there is the presence of central stations devoted to the conversion of some kind of energy in electrical energy, an high voltage grid to transmit the energy over long distances and a distribution network using lower voltage levels to supply energy to the final users (e.g. private houses, stores and any kind of electrical device).

The overall network (comprising transmission and distribution grids) is meshed and continuously subject to modifications in topology (due to faults, improvements, maintanance), production (insertion and disconnection of generators) and consumes (fluctuation of the loads), therefore the operating point is continuously changing.

The system is not linear: although the grid can be represented by a linear system relating

current injected into the nodes and voltages of the nodes [2]:

$$[\bar{I}] = [\bar{Y}][\bar{V}] \tag{2.1}$$

the relations among node voltages and injected powers by generators and absorbed by loads are non linear:

$$P_h = V_h \sum V_k (G_{hk} \cos\theta_{hk} + B_{hk} \sin\theta_{hk}) \tag{2.2}$$

$$Q_h = V_h \sum V_k (G_{hk} \sin\theta_{hk} - B_{hk} \cos\theta_{hk}) \tag{2.3}$$

where:

- P_h, Q_h are real and reactive power injections at node h;
- V_h is node voltage amplitude at node h;
- θ_{hk} is phase displacement between voltages phasors at node h and k;
- $Y_{hk} = G_{hk} + jB_{hk}$ is the generic element of matrix $[Y]$.

In addiction to that, there are several devices inside the network, whose behavior is linear only if limited to an interval with the presence of saturation phenomena, or devices that are inherently not linear (e.g. switches).

The complexity of the control of such system is augmented by several factors:

- external constraints (as environmental issues) strongly limit the expansion of the system;
- while in the past the operations and management were vertically centralized and controlled, nowadays several actors participate in the control. Generation, transmission and distribution are now managed by different companies. Each participant in the system has different goals, thus an additional issue about the coordination of these independent operators arises;
- in the last decades the production of energy is changing rapidly with emerging distributed generation of medium and little (some kVA) size. Distributed generation has performed a rapidly growth due to environmental concerns leading to an incremented use of renewable resources and a better use of fossil fuels (e.g. the combined heat and power power plants of medium and small size) and to the open market of electricity: now it is possible to enter this market also with small productions (and thus small investments). This breaks

the traditional vertical structure in which energy used to be transferred following a top-to-bottom pattern.

Such a complex system is managed and controlled with multiple objectives three of the major being:

- supplying loads with adequate level of quality;
- optimizing the economic issues of the overall system;
- minimal environmental impact.

Further, the control objectives are dependent on the operating state of the system. The different operating points are for example classified as normal, alert, emergency, restorative.

A complete centralized control of the whole system is considered unfeasible. Therefore, the system is traditionally decomposed to use the ancient strategy "divide et impera".

Several subdivisions overlap [3]:

- at the voltage level, the electrical network is commonly divided into three main levels: the high voltage network (EHV or HV) , the medium voltage network (MV) and the low voltage network (LV). Each of these three can comprise a deeper subdivision with several different voltages. The HV network comprises the high voltage at 400 kV, the 220 kV level and the subtransmission network at 130 kV. The MV as well comprises levels from 60 kV to 20 kV and some parts in 15 kV and 10 kV. The LV is normally distributed in 400 V for the three phase and 230 for the monophase. Although different countries present some differences, for all of them it is common to have a functional subdivision into at least two main levels: a transmission network with high voltages and a distribution network with medium and a low voltage;
- a geographical criteria: although the transmission grid is connected at continent level, it is usually subdivided into different areas interconnected. Also, the distribution network can be subdivided into independent feeders. From the industrial point of view , Independent System Operators (ISO) are organized as national structures and also distribution companies are normally organized on geographical homogeneous areas;
- on time-horizon criteria, the power system comprises physical phenomena with different dynamic time scale. Description and control of the system can be therefore classified and divided on the basis of the dynamic time scales;

- decoupling of variables permits to separate control problems about variables, that are weakly coupled. In transmission networks, voltages are strictly dependent on reactive power flow, while frequency is strongly coupled with active power flows;

- small and large perturbations: the non linear power system is often linearized, thus separating the control problem of response to small perturbations from the problem of response to large perturbations;

- objective criteria: A power system is typically a multi-objective system and it is studied and controlled separately for each objective.

A big issue is to account for the overlapping among the different subproblems, but this will not be considered here. The focus will be only on some aspects of voltage control.

2.3 Voltage control

Electric power systems are built essentially with lines connecting generators and users. For the purpose of this thesis an AC line can be modeled as a linear and passive four terminal element. This represents the positive-sequence singular phase equivalent circuit of a line under steady state operating conditions.

Voltages propagates via two voltage waves with a speed w depending on the physical characteristics of the line. The wave length of a line is defined as the distance between two points of the line where at an instant the voltage phasors have a phase difference of 2π. Electrical short lines are those lines whose length is small compared to wavelength. The wavelength varies from 6000 km for typical 380 kV ahead lines to 1760 km for underground 15 kV lines. In short lines admittance is negligible and therefore a line can be modeled with the four terminal element shown in Fig. 2.1.

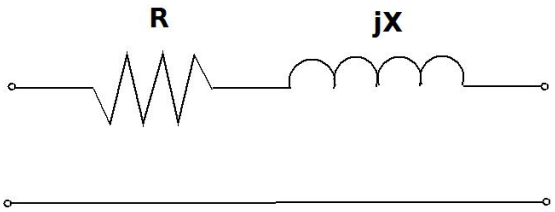


Figure 2.1: AC line - Equivalent circuit of short lines.

The resistance of lines accounting for stranding and skin effect can be determined from manufacturers' tables or calculated by:

$$r = \frac{\rho}{S}k \tag{2.4}$$

where:

ρ is the dc resistivity expressed in $\Omega \times mm^2/km$;

S is the cross section in mm^2;

k is a coefficient taking into account the temperature effect, the skin effect and the conductor construction.

The positive sequence inductance per unit length can be expressed as:

$$l = 0.46 \log_{10} \frac{2D}{kd} \qquad [mH/km] \tag{2.5}$$

where:

D is the geometric mean distance between the three conductors expressed in mm;

d is the diameter of the conductor (supposed equal for all the three conductors) expressed in mm;

k is a coefficient that takes into account the conductor composition, stranding and bundling. It can vary from 0.75 to 0.85.

Considered that the conductors in cable are much closer to each other than are the conductors of overhead lines the inductance per phase in underground cables is lower than in overhead lines.

Most of electrical lines of the distribution system can be considered electrically short.

The phasor diagram in Fig. 2.2 of the circuit allows to write the following relations between reactive power, active power and voltage drop in such a line:

$$V_1 - V_2 \simeq \frac{RP + XQ}{V_2} \tag{2.6}$$

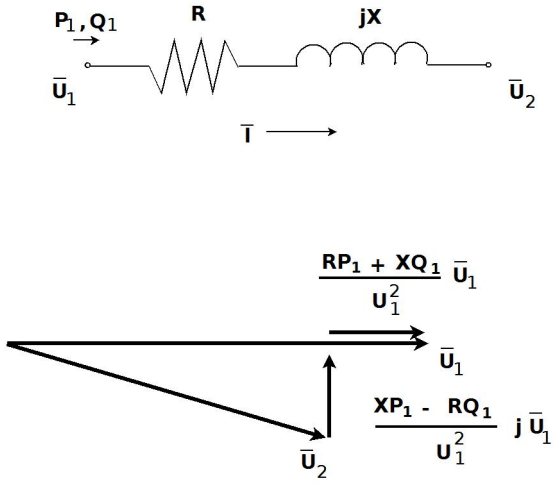


Figure 2.2: Phasor diagram - Phasor diagram for short lines.

For lines where also resistance is negligible if compared to reactance, the voltage drop can be expressed in terms of the only reactive power flowing through the line:

$$V_1 - V_2 \simeq \frac{XQ}{V_2} \tag{2.7}$$

Therefore the voltage problem control in the transmission grid (where resistance and admittance of the lines are neglected) depends on the flow of reactive power.

Several reactive power sources are used for controlling voltage

- shunt capacitors;
- shunt reactors;
- SVC Static VAR compensator;
- OLTC On Line Tap Changer;
- synchronous generators;

In this work, only voltage regulation based on generators will be considered.

2.3.1 Primary voltage control

Electrical energy generation in transmission networks is essentially constituted by synchronous generators. Therefore a first voltage regulation action is pursued through generators. This regulation action is called the primary voltage control and is provided by excitation control of

generating sets, which tends to reduce the difference between the actual voltage at generator terminals and the scheduled set point.

With the approximation of line impendance with the only reactance x_L (thus neglecting the influence of active power flow on voltage), the relation between the voltage at the generator terminal and at the load is expressed by the equation:

$$v_L = v - (x_t + x_L)q_L$$

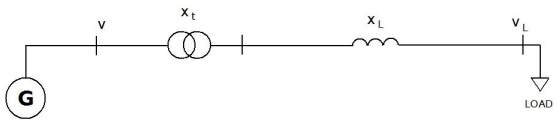


Figure 2.3: Primary Control - Generator supplying a load.

Under steady state, voltage at generator terminal can be expressed in terms of excitation voltage:

$$v = v_f - x_d i \tag{2.8}$$

where x_d is the direct axis synchronous reactance and v_f is the excitation voltage. The voltage control, acting on the excitation voltage, can support the voltage at load node, increasing the excitation voltage when reactive load increases.

When the active power flowing through a transmission line is lower than the natural power (i.e. natural load) of the line, the line generates reactive power. Therefore, to maintain a constant voltage to the load terminals, the generator should absorb reactive power.

It is possible to control the voltage at the alternator terminals acting on the excitation voltage.

The voltage control for a synchronous generator is performed via the Excitation Control Systems (ECS) whose structure is in Fig. 2.4 [4].

For the aim of the study of the primary regulation, a synchronous generator can be considered connected to a large power system modeled as an infinite bus (i.e. its inertia and short-circuit power is infinite to respect to those of the alternator and therefore bus voltage is constant under any load condition) through a single reactance x_R (the reactance x_R is that reactance viewed from the generator terminals).

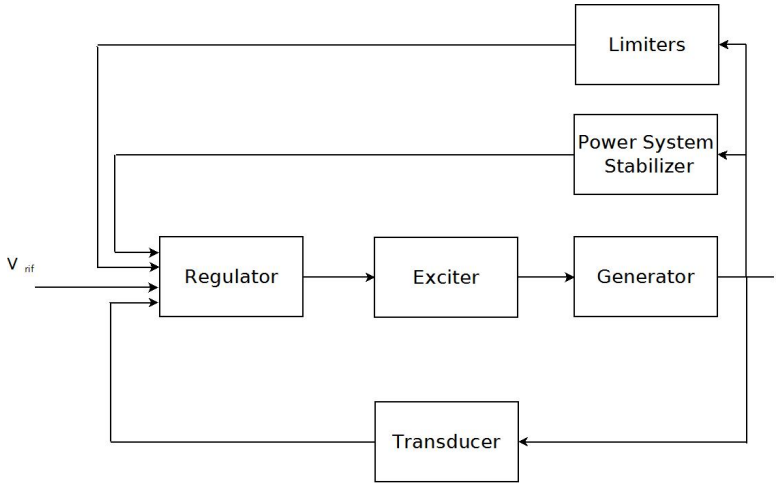


Figure 2.4: ECS - Functional block diagram of a synchronous generator excitation control system [4].

Merely to consider the voltage control loop we can refer to the approximated block diagram in Fig. 2.5

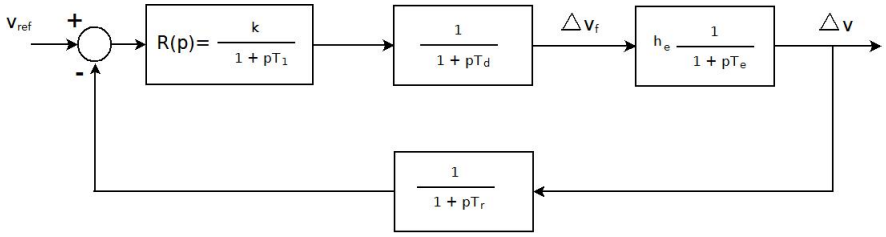


Figure 2.5: ECS diagram - Block diagram of the voltage control loop of a synchronous generator.

Considering that:

- T_1 is the high frequency dominant time constant of the voltage regulator which is approximated with a first order transfer function; k is the high frequency dynamic gain of the voltage regulator;
- T_r is the constant time of the transducer that, for modern systems, is of the order of 0.02 s;
- T_d is the time constant of the exciter and is negligible for static exciters, i.e. the static excitation system is approximated with a fast, comparing to the other subsystems, first order system.

To find the transfer function between excitation voltage and generator terminal voltage some approximation can be done. For small variations, assuming an asymptotic high frequency approximation (i.e. $\omega \gg 1/T_d^{'}$) and with a low (dynamic) load angle, the following approximated relations can be considered:

$$\Delta v \simeq \Delta v_q$$

Stator current and voltage and excitation voltage are related with the following expression[1]:

$$v_q = \frac{1}{1+pT_{d0}^{'}} v_f - x_d \frac{1+pT_d^{'}}{1+pT_{d0}^{'}} i_d \tag{2.9}$$

where :

- $T_{d0}^{'}$ is the direct-axis open circuit time constant: from 5 to 8 seconds;
- $T_d^{'}$ is the direct-axis transient short-circuit time constant: from 0.75 to 1.5 seconds;
- x_d is the direct-axis synchronous reactance: from 1 to 2.5 [p.u.];

The direct axis current i_d can be expressed in terms of the voltage machine and the network voltage:

$$i_d = \frac{v - v_R}{x_R} \tag{2.10}$$

Modeled the network as an infinite bus ($\Delta v_R = 0$), small variations of the armature current can be expressed as:

$$\Delta i_d = \frac{\Delta v}{x_R} \tag{2.11}$$

Therefore, for small variations:

$$\Delta v = \frac{1}{1+pT_{d0}^{'}} \Delta v_f - \frac{x_d}{x_R} \frac{1+pT_d^{'}}{1+pT_{d0}^{'}} \Delta v \tag{2.12}$$

It follows that the relation between excitation voltage and terminal voltage variations is:

$$\Delta v = h_e \frac{1}{1+pT_e} \Delta v_f \tag{2.13}$$

where:

- $h_e = \frac{x_R}{x_R + x_d}$ can be considered of 0.5 [p.u./p.u.];

[1] the additional circuits have no impact under steady-state operating conditions

- $T_e = T'_{d0}\frac{x_R+x'_d}{x_R+x_d}$ is therefore the time constant of the generator under load conditions.

Finally, from Fig. 2.5, the fact that that the voltage control loop for a synchronous generator has a cut-off frequency in the order of units of radiants (3 - 6 rad/sec), can be deduced (also in [5]) . In other words the closed loop time constant of the primary voltage control loop is lower than 1 second.

The sampling frequency for a digital control system has to be chosen according to the desired bandwith of the closed loop system. the rule that can be used to choose the sampling frequency in control system could be [6]:

$$f_s = (6 \quad to \quad 25) f_B^{CL} \tag{2.14}$$

where f_B^{CL} is the closed loop bandwidth. This requested sampling frequency will be compared with the real-time performance of the chosen hardware and software platform described in chapter 3.

Although SVC and OLTC are traditionally considered to be part of primary voltage control, they will not be analyzed in this work.

2.3.2 Secondary voltage control

Studies on real-time automatic control of power system voltage and reactive power started in the 1970s and led to significant proposals and applications. Hierarchical approaches in frequency-active power control of multimachine power systems for reducing the complexity of solutions with a large-ordes systems can be found in [7]. A centralized optimizing computational algorithm for the on-line control of voltage and reactive power is presented in [8] [9] and [10]. The stress is on real-time control of reactive power and voltage, using large-scale digital computing facilities and system-wide data transmission channels already installed for the automatic frequency control.

One of the implemented strategies of voltage control in EHV transmission networks consists in dividing a power system into several areas [11] and setting up a hierarchical voltage control system. The crucial idea to decompose a large power system into several blocks in such a way, that the electrical coupling between blocks can be made as small as possible, is also presented in [12].

Algorithms and control schemes using electric power plants as continuous sources of reactive power for voltage control, together with the subdivision of the power system into different

coordinated blocks, were then exploited and developed in several countries under different approaches.

Voltage hierarchical controls were studied and developed in Italy [13] and [14].

Also in France since the 1980s a secondary voltage control has been studied [15].

Hence, similar hierarchical controls for EHV transmission networks were adopted also in Spain [16] and South Africa [17].

The aim of the Secondary Voltage Regulation (SVR) is to keep constant the voltages of some HV nodes, upon load variations and perturbations in the system. As already seen, voltages in HV nodes are mainly affected by reactive power flows and several sources of reactive power are present in power sistems: generators, shunt capacitors and reactors, static VAR systems.

Once the appropriate operating voltages of the HV nodes is determined solving optimal power flow problems, an automatic system is desired acting on reactive power sources, to maintain such voltages constant despite the perturbations in the system. A centralized control, reading all selected HV node voltages and acting simultaneously on all reactive power sources in the system to maintain the voltages in those nodes constant, has always been considered unfeasible.

The main reasons against a centralized control are the complexity of the transmission data system, the computing time for a central unit to cover all the system and the reliability of a centralized architecture.

Node voltages variations and reactive power variations of the linearized power system, can be expressed with a linear relation:

$$[\Delta v] = [A][\Delta Q] \tag{2.15}$$

where $[A]$ is a voltage sensitivity matrix.

A transmission power system is conveniently subdivided into subsets of nodes and therefore the linear relations above can be written as:

$$\begin{bmatrix} A_{1,1} & \vdots & A_{1,j} & \vdots & & \vdots & \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ & \vdots & A_{i,i} & \vdots & A_{i,j} & \vdots & \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ & \vdots & & \vdots & & \vdots & \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ & \vdots & & \vdots & & \vdots & A_{n,n} \end{bmatrix} \begin{bmatrix} \Delta Q_{S1} \\ \\ \cdots \\ \Delta Q_{Si} \\ \cdots \\ \\ \cdots \\ \\ \Delta Q_{Sn} \end{bmatrix} = \begin{bmatrix} \Delta v_{S1} \\ \\ \cdots \\ \Delta v_{Si} \\ \cdots \\ \\ \cdots \\ \\ \Delta v_{Sn} \end{bmatrix} \tag{2.16}$$

In a decentralized control scheme each subsystem is controlled independently, i.e. the non diagonal submatrices $A_{i.j}$ where $i \neq j$ are neglected.

In Fig 2.6 the original schematic diagram of the hierarchical voltage control system is reported as it was presented in 1983 in [14] for the italian HV power system.

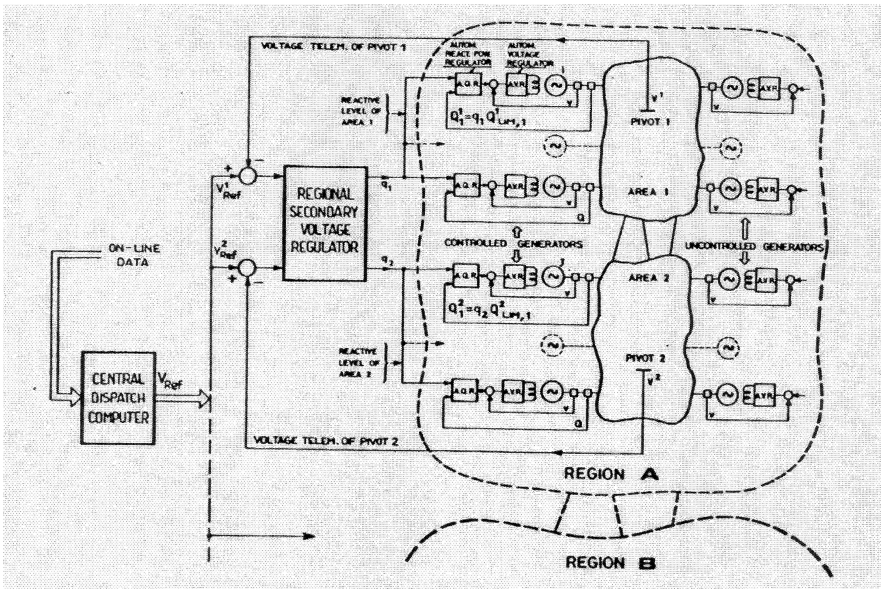


Figure 2.6: SVR diagram - Schematic diagram of the hierarchical voltage control as it was presented in 1983.

The above diagram is still relevant and in chapter 6 the same schema is presented with the terminology as it stands now according to the Italian national grid code. The first hierarchical level is constituted by the conventional voltage regulator of each generator (i.e. AVRs). The second level consists of the regional secondary voltage regulators and the reactive power station regulators (called Automatic Reactive Power Regulator - AQR in the schema 2.6 and called SART in the Italian Grid code as it will be described in chapter 6). The regional secondary voltage regulator controls the voltage of pilot nodes through an integral action while the SARTs apparatus actuates the reactive power level required by the regional controller acting on the AVRs. The regional regulator receives the voltage values of its pivot nodes and compares these values with the reference values fixed by the tertiary regulator and sends a reactive level signal to each of the reactive power regulators of its area. The reference of reactive regulators is the reactive level (a scalar quantity q in the range of $-1 \leq q \leq 1$ multiplied by the reactive power limit (depending on the size of the generators and their operating point, i.e. depending on the

capability curves):

$$Q_{ref} = q_{ref} \cdot Q_{lim} \tag{2.17}$$

where:

- Q_{ref} is the reactive power requested to the generator;
- Q_{lim} is the reactive power limit of the generator;
- q_{ref} is the reactive level transmitted.

The third hierarchical level is made at central level and has the purpose to determine optimum values of the voltages of some nodes (called pilot nodes), that are controlled by the secondary regulators. The architecture and implementation of the AQR (now called SART) apparatus is the main topic of this work.

The reactive power control loop implemented by SART apparatus is shown in Fig 2.7.

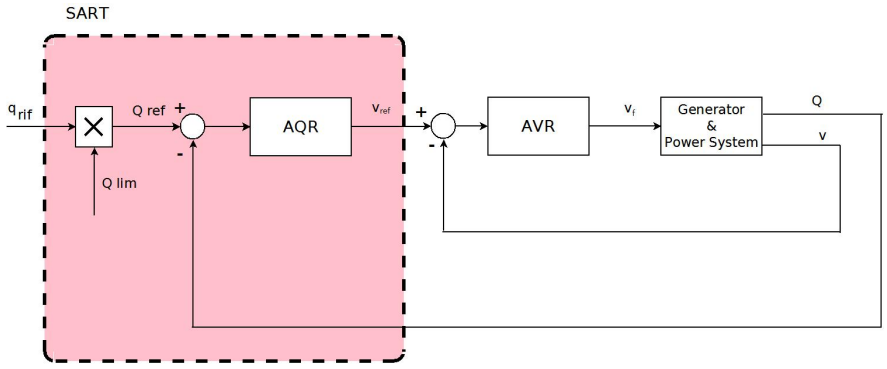


Figure 2.7: RPR diagram - Block diagram of the reactive power control loop of the secondary voltage regulation.

The closed-loop time constant of the reactive power control loop of a power plant is set to be ten times lower than the inner voltage control loop (i.e. the one before described and implemented with AVRs), and therefore is usually in the range from 5 to 10 seconds.

2.3.3 Voltage control in distribution network

Despite the differences that can be noticed across the world, some common elements in the realization and mode of operation and connection in the distribution networks can be found:

- the network is normally designed in a radial way: starting from HV/MV substations, conductors take different directions with a tree structure;
- every country imposes constraints on the characteristics of voltage signals limiting amplitudes fluctations (often a ±5% limit is considered);
- although it is hard to highlight a constant type of conductor the main physical characteristics used are
  - aluminum (and combinations aluminum-steel) cables with sections varying from 50 mm^2 to 500 mm^2;
  - copper (and combinations copper-steel) cables with sections varying from 40 mm^2 to 150 mm^2;
- MV lines are normally three-phased feeders with or without a neutral conductor. The three (or four in case of distributed neutral) conductors can be overhead or underground, being the latter the most common choice in urban areas.

The voltage drop in a distribution feeder can be expressed as in equation 7.2, here reported:

$$V_1 - V_2 \simeq \frac{RP + XQ}{V_2} \tag{2.18}$$

This approximation is true if the angle between the voltages of the input and output of the line is small (as it is for short lines not highly charged).

Differently from transmission networks, where the term RP can be neglected due to the low value of the R/X ratio, in distribution networks both terms must be considered, as R/X is higher. Table 2.1 reports some typical values for longitudinal primary constant of lines as in [18].

Type of line	**r[ohm/km]**	**l[mH/km]**	**x[ohm/km]**	**R/X**
380 kV overhead line, single conductor	0.029	1,22	0.383	0.075
380 kV overhead line, twin conductors	0.028	0.99	0.310	0.090
220 kV overhead line	0.084	1.30	0.408	0.206
130 kV overhead line	0.228	1.26	0.395	0.577
380 kv underground cable	0.028	0.22	0.069	0.406
220 kV underground cable	0.056	0.37	0.116	0.483
15 kV underground cable	0.150	0.30	0.094	1.596

Table 2.1: Line cable data - Line data for different type of cables at 50Hz.

In traditional distribution networks, the power flow is unidirectional: it goes from the HV/MV station to the consumers. Therefore the voltage decreases between the distribution substation to the end of the feeder. When in presence of generators in the distribution network, due to the injection of active power, the voltage profile can be non monotonically descendant.

To guarantee equipment safety (too high voltage can reduce the lifespan of users' appliances) and correct functioning, the voltage has to be kept within its contractual range defined on the grid code.

The main control devices used in distribution feeders to regulate the voltage in order to guarantee the contractual limits are On-Load Tap Changers (OLTC) transformers and auto transformers. These are devices in which is possible to alter the transformation ratio by discrete steps. The voltage of MV buses is adjusted in function of the variations of loads and the evolution of the upstream voltage. Although some industrial customers connected to the MV network having their own means of reactive compensation (e.g. capacitor banks and static var compensators), no other voltage control is made in distribution grids apart than those discrete regulations with transformers described.

An evolution in distribution networks has taken place over the past few years with the introduction of the so called Distributed Generation. A deep exploitation of the problems leaded by the introduction of DG can be found in [19]. In chapter 7 the impacts on the voltage profile because of the active power injections, when in presence of productions of electrical energy connected to the distribution network, will be described and a possible strategy of voltage/var control is presented.

2.4 Conclusions

Due to the complexity of power systems, their control is split into a number of subproblems. Some aspects of voltage control were reported. Time constant of the voltage control loop for synchronous generators is commonly reported to be in the range $0.2 \div 1$ second. For the secondary voltage control, the power plant reactive power control loop time constant is usually around 5 seconds. Time constants of these control loops have to be compared to real-time performances of the operating system, that is described in next chapter.

3

Real-time operating systems

3.1 Introduction

A review of real-time operating systems and their performance is reported. RTAI has been chosen and its structure and development tools are detailed. Adequacy of RTAI to the development of control systems for electrical energy production and regulation is attested through measurements of its performance under different working conditions. The design and development methodology used are presented.

3.2 Real-time control systems

Several different hardware and software architectures are available to build real-time controls, each with an impressive variety of different commercial or open source products. We have focused on utilizing common hardware, which is easy to maintain, with general-purpose widely used processors and operating systems which can be profitably integrated in a distributed environment. Often, Hard Real Time (HRT) control tasks are accomplished by employing specific dedicated processing units. An example is the wide use of Digital Signal Processors (DSPs) or micro controllers which guarantee a bounded interrupt latency. The key issue in HRT is that the control system has to guarantee signal processing timing, without missing deadlines for interrupts and keeping latency bounded within a level compatible with the sampling time of the process. As in [20], a real-time system has to respond to externally generated input stimuli within a finite and specifiable delay.

A general control algorithm can be simplified with the code in Fig. 3.1: a control law is designed according to discrete-time control system theory and implemented as a real-time

periodic task:

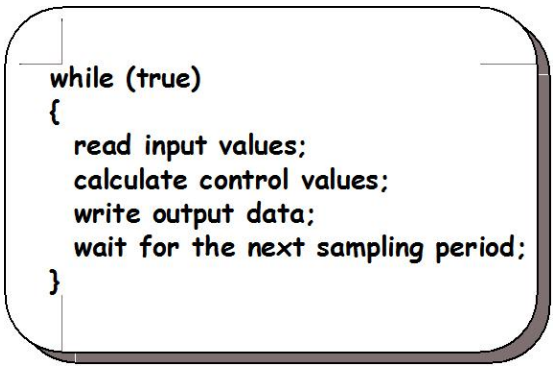


Figure 3.1: Control - General schema of a controller.

In the design process of a digital control system there are two fundamental constraints which have to be fulfilled by the device implementing the control:

- Computational power: inspecting the algorithm and its implementation code is possible to exactly determine how many fundamental mathematical functions have to be executed. The computational requests of the control task can be expressed in floating point operations per second. To simplify all this, it is possible to measure the execution time of the control loop on the target hardware platform;
- Temporal constraints: several temporal requirements can be found in the control algorithm. The first requirement is the frequency at which the control task is executed.

From the control designer's point of view, the variation of the scheduling time is important and determines if a chosen hardware and software platform is suitable for a certain control task.

For the frequencies requested by control algorithms described in chapter 2, considered the computational performance of modern 32 and 64 bit CPUs, the computational time requested for the control algorithm is normally well beyond the period of the control system. Also, the computational time itself presents a negligible variation. Differently from DSPs, that have an architecture focused on numerical computations, and are also designed to have a strong determinism in computational time, General Purpose Processors (GPPs) have been developed for general purpose computing and are not specifically designed and optimized to keep a guaranteed scheduling jitter.

GPPs that can be found in personal computers, servers, network apparatuses but also in personal entertainment devices, present a strong, non-deterministic behaviour in computational

time: several tasks (some of them completely out of the control designer's control) fight for the use of the processor units.

Therefore, GPPs while presents adequate performance to carry out signal processing tasks, they do not have suitable deterministic timing characteristics for real-time controls.

The use of Commercial-Off-The-Shelf (COTS) low cost personal computers (and all their hardware and software components) for digital programming and signal processing can lead to a reduction of the cost of the final device. Utilization of cheap microprocessors for real-time systems has been investigated since the 1980s [21].

The great progress made by the semiconductor industry has provided cheaper 32 and 64 bit processors with Memory Management Unit (MMU) . One of the features provided by MMU is the memory protection, which gives a higher level of fault tolerance in software development because different tasks can function in a separate and protected memory space [22].

Therefore there are several CPUs on the market with an extremely high computation power, available at low prices, as a complete set of motherboards and entire COTS computing systems ready for running. The main disadvantage of these systems is that they were not designed for real-time, but even if GPPs are not specifically designed and optimized to carry out signal processing tasks keeping a guaranteed scheduling jitter, an RTOS can make them suitable for real-time applications.

3.2.1 Operating systems

An Operating System (OS) is commonly identified as the software that controls and manages the hardware of a computing system; one of its main purposes is to implement the interface used by all the other users' programs to have access to the hardware itself. This interface is a collection of software programs that implement the system-calls. The system calls are all the basic functions required to operate with the hardware. The set constituted by the system calls is what the OS offers to programmers.

For the x86 32 bit architecture of the Linux kernel 2.6.29 there are circa three hundred system calls whose names and numbers can be found in the *include/asm-x86/unistd_32.h* file in the Linux sources. As an example of system calls these could be taken into consideration:

sys_fork to create a child process;

sys_exit to terminate the current process;

sys_open to open and possibly create a file descriptor;

sys_close to close a file descriptor;

sys_read to read from a file descriptor;

sys_write to write to a file descriptor;

sys_mount to mount a file system;

Therefore the set of system calls represents the core (often called kernel) of an OS. On all those system calls several higher level functionalities are built in a modern OS. Although the functionalities that an operating system have to offer to programmers is universally accepted, the way this functionalities are presented is a matter of standard. There are several standards on how system calls ought to be used .

One of the most used standards for the Application Programming Interface (API) offered by an operating system is the standard Portable Operating System Interface for Unix (POSIX). POSIX is an IEEE standard and defines the interface for each feature: it defines all the functions an Unix operating system has to implement.

Unix is one of the most important operating systems. Unix has become important because in it the most of the fundamental ideas on design of OS (ideas that have been implemented also by most of all the other OS on the market) were first implemented, nonetheless Unix, in one of the several existing implementations, is still one of the most used OSs.

Unix was born in the Bell laboratories during the 1960s and 1970s and is the result of the effort by many people, the most famous names that can be remembered are Ken Thomson, Dennis Richie and Brian Kernighan. Multitasking, multiuser and virtual memory management are three pillars of Unix that can now be found in every OS. The Unix source code was published by Bell laboratories to accomplish US antitrust laws and several different Unix-like OSs have since been autonomously developed by different groups and companies.

3.2.2 Linux

Among all those that pursued their studies and development on Unix, prof. Tanenbaum from University of Vrije of Amsterdam and his collaborators wrote an Unix kernel named Minix [23]. Minix, at that time, was one of the few running on the cheap x386 platform . To get the Minix source code one only had to to buy prof. Tanenbaum book on operating systems [22].

One of the users of Minix was a Finnish student : Linus Torvald. He went some steps forward: he started writing a new, free Unix-like OS. When his kernel was approximately running, during

the month of October 1991 he looked for help: as a consequence a new community of developers started.

Linux is one of the several General Purpose Operating Systems (GPOS) which have been developed for 32 and 64 bit processors with MMU that has become widely used. It is known as the GNU/Linux system: it is composed by a kernel [24] [25] and a collection of system software [26] whose source code is freely available under the Generic Public License (GPL) [27] .

3.2.3 Real Time Operating Systems

Even if GPPs which are normally present on commercial PCs are not specifically designed for real-time, a RTOS can make them suitable for real-time applications.

Several commercially supported embedded operating systems have been proposed in the last two decades: a list of RTOS on wikipaedia includes 106 different ones [28]. Commercial RTOS often require to pay per-unit-royalties but, when adequately supported by the developing companies (normally with an added maintenance cost), they do not require a complete understanding of the hardware and software platform in order to develop an application. Moreover they leave the developer to concentrate their efforts on the application itself rather than on the RTOS used. On the other hand, some commercial RTOS do not rely on an open architecture and do not always offer a standard API. Therefore it can be difficult to migrate to other platforms and thus the developer and the product destiny are too strictly closed to the RTOS company with the risk, when the company disappears, to be left out in the cold.

Some of the RTOS have been designed from ground up starting from a real-time kernel and adding new features to became a complete operating system. The computer performance and the capacity improvements have increased the demand of functionality of each processing device (e.g. the request of graphical interfaces), boosting the request for RTOS to present all the features of a GPOS.

Economical reasons lead to the emerging approach to extend a GPOS to be an RTOS, in particular starting from open source operating systems. Therefore along with the RTOS born as a real-time system, several RTOS have been built as extension of existing non real-time OS.

There are also different strategies in extending an OS to an RTOS: single kernel approach or multi kernel approach. In [29] is presented a summary of different real-time extensions of Linux (therefore different strategies to extend an OS, focused only on Linux).

Although the majority of RTOSs have a Unix-like structure, Windows CE is a version of Windows with real-time performance.

Among consolidated or new emerging RTOSs which can be used with GPPs, the following can be quoted:

- RTLinux: it started at New Mexico Institute of Technology [33]; several other projects based on Linux followed this approach, although the original solution was patented [34];
- Real Time Application Interface (RTAI) : it was developed at Politecnico of Milano [30] and has also been used for distributed controls [31];
- QNX: a commercial RTOS based on a microkernel, born on 1982 [32];
- VxWorks: born 25 years ago, it is still one of the worlds leading RTOS.

The listed RTOSs differ for a lot of characteristics. RTLinux and RTAI are two patches that have to be applied to a Linux kernel [1] to make it a real-time system. This means that they are extensions of an existing OS. They do not live by themselves but only as a part of an open source OS. Both are based on Linux and therefore the development of all their parts not strictly implied in the real-time core is left to the international volunteer community of developers.

Having RTLinux been patented, it presents some limitations in its commercial use. On the other hand, RTAI is published under the GPL and is freely usable also for commercial purposes without any royalty.

QNX and VxWorks are two complete RTOSs, they do not depend on other OS. Both OSs are owned by private companies and are maintained, upgraded and ported to different kinds of hardware by those companies.

From a more technical point of view, QNX has a microkernel structure while the others are monolithic kernels. From the user's point of view, the fact that it is based on a microkernel architecture or on a monolithic one does not have any practical effects. Most experts agree on the fact that a microkernel architecture is more appropriate for modern OSs including a huge and always increasing list of functionalities but the majority of the OS on the market are monolithic. All the four OSs can be defined Unix-like because each of them is a POSIX compliant.

Some operating system vendors offer not an extension of their GPOSs but a limited version of them with real-time capabilities; the already mentioned Windows CE is a (limited) version of Windows while Chorus OS from Sun Microsystems is a real-time flavor of the Solaris OS.

[1] An original so called vanilla kernel that can be downloaded from http://kernel.org

An analytical review and comparison of all the presented RTOSs is beyond the scope of this work.

This work will present some applications related to the production and management of electrical energy with RTAI. Most of the considerations could be applicable to all the other mentioned RTOSs. All the two implemented devices that will be detailed in the next chapters could be also developed with one of the other RTOS, probably with a similar performance and comparable efforts. Therefore, several different RTOSs could be chosen to develop a real-time device which is easy to integrate in a complex SCADA system, is ready to be ported on different hardware platforms, is open to different communication protocols and has a good performance.

RTAI was chosen for this project.

3.3 RTAI

Real-time performance in modern OSs is strictly related to one of the most common characteristics of general purpose OSs: multitasking. There still exist real-time devices implemented in the old DOS: this is possible because DOS was not a multitasking OS. When a single task is running on a CPU there are minimal problems to control interrupts coming from the hardware (e.g. an interrupt coming from a clock saying that the control task has to start). In multitasking systems there are several active processes but only one (in single processor systems) running at a specific time: when a single processor is presented in a system, it executes only one instruction at a time and this instruction belongs to a unique process among those which are active. When an interrupt arrives from the hardware (e.g. the interrupt from a timer to wake up the control loop shown in Fig 3.1) the running task has to be suspended to respond to the interrupt: a real-time system assures that each interrupt will be elaborated in a specific, deterministic time. Therefore each process, no matter if it is running kernel-code or user-code, has to be interruptible and the context switch has to be executed in a specified amount of time.

3.3.1 Why Linux is not real-time

There are several reasons why Linux is not considered a real-time system:

- System calls are not-preemptible: this is strictly true only with the older version 2.4 of Linux. Although the latest 2.6 versions of Linux kernel system calls are preemptible, the granularity level is such that the real-time performance is limited;
- Virtual memory swapping activity can introduce unpredictable delays and latencies;

- I/O activity is normally buffered and scheduled in a non-deterministic way.

There are also some aspects which are strongly related to the hardware architecture that leads to non real-time systems:

- Pipelining: in modern processors, instructions are divided in several phases that are parallelized and loaded in advance. When an inversion in the order of the instructions happens, as for executing an interrupt handler code, the pipeline has to be destroyed, leading to a non deterministic delay;
- Cache: as mentioned before, the load of code following an interrupt destroys all the codes and data actually present in cache, introducing extra work with its unexpected delay.

In a standard 2.6 Linux kernel, a call to kernel code (made through a system call) cannot be pre-emptied. This means that if a user-space process makes a system call, a high-priority process must wait until that call is completed before it can use the CPU. For this reason, if a task is running kernel-code and an interrupt from a timer rises to wake up the control loop, this is delayed until the kernel code has finished, leading to a latency in real-time scheduling. This happens because the kernel code is protected by locks to prevent the preemption of a critical code: unfortunately this locks contain a huge amount of code and were not designed to satisfy real-time requirements but to run the computer safely and fast (on an average basis).

One patch (the so called Realtime Preemption patch by Ingo Molnar), which re-implements all the locks used in the Linux kernel and introduces high resolution kernel timers, gains hard real-time capabilities at the cost of intruding into most of the core kernel code and a slightly lower throughput and possible performance degradation.

Other two ways to gain hard real-time characteristics are:

- Interrupt abstraction: interrupts are managed directly by a module which is set to serve real-time tasks with higher priority;
- Nanokernel: there is a kernel with minimal functionalities which manages hardware and process scheduling: the standard Linux non real-time kernel is simply a process scheduled with the real-time declared tasks.

The two systems are actually very similar: being the first one covered by a patent, the second one is widely used. Both methods have their roots in a development which started at New Mexico Institute of Mining and Technology [35][36][37] and has become a mature technology under

the name of RTLinux and has also been patented [38]. Other similar ideas, like the Adaptive Domain Environment for Operating Systems (Adeos) [39] and individual developments, have given to all the community different patches to the Linux kernel, which offer real-time performance. RTAI (Real Time Application Interface) [40] is one of these. The simple graph in Fig 3.2 depicts the RTAI structure: a nanokernel (here called ADEOS) which is implemented as a module, manages hardware and therefore abstracts all interrupts and real-time tasks. The original Linux kernel is only one of the tasks managed by the nanokernel.

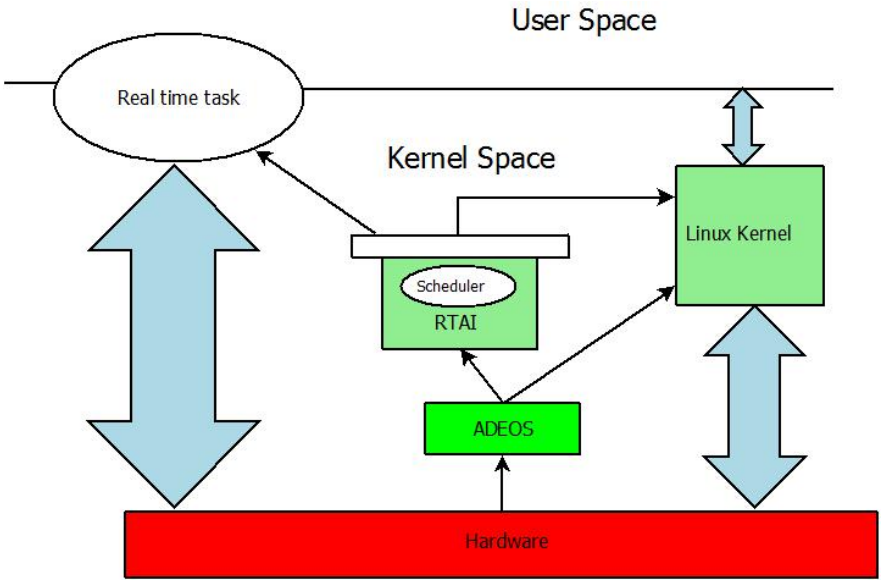


Figure 3.2: RTAI - RTAI Architecture.

The same picture shown in Fig. 3.2 could have been drawn with the module named HAL instead of ADEOS: HAL (Hardware Abstraction Layer) was the name of the module that made the interrupt abstraction in the first versions of RTAI. Its working principle has been patented in 2001 by Victor Yodaiken. Prof. Yodaiken presented a detailed description in which a general purpose operating system is preempted as needed for the real-time tasks and is prevented from blocking preemption of the non real-time tasks. Karim Yaghmour described in [39] a similar, even more general concept. The Adaptive Domain Environment for Operating Systems (Adeos) is an environment to share hardware resources among multiple operating systems. Adeos is not strictly related to real-time but is a more general tool. An example of application of this environment is to have a nanokernel covering all the interrupts to have a real-time response and, in parallel to this, another complete Linux kernel (running on non real-time) to offer all other

functionalities requested to an operating system. Another application is the virtualization of different OSs on the same hardware. Since Adeos was published and not covered by any patent, it was used to publish RTAI with a GPL license: the code differences from HAL module and Adeos were practically negligible.

3.4 Real-time performance

There are several aspects that can be considered when valuating the real-time performance of a RTOS, but when judging an RTOS, two major elements can be considered: performance (the time taken to respond to an external interrupt) and determinism (the variation of this performance, i.e. the variation of the time it takes to respond) [41]. These two elements are often reported in literature as latency and jitter of latency. Together they represent the performance of an RTOS and describe its suitability for use in real-time systems.

The main indexes used are therefore the measure of latency and jitter of a certain event:

- the latency is defined as the difference between the time an event is expected to occur and the time an event actually occurs [42], thus a random variable C over N samples can be defined, where C_n is the latency of the nth event. If a task is scheduled to start every 10 milliseconds, the actual time it starts is a random variable and the time between one start and the following start of the task is another random variable (the latter is a random variable of the period of the task);

- the jitter is a piece of information about the variation of the latency in the set of N samples previously measured; the standard deviation can be considered with regards to the set of N latency measurements or the maximum value over the same set. Considering the jitter of the random variable describing the period gives a measure of how precise the scheduling of a task is.

An hard real-time system means being aware of the Worst Case Execution Time (WCET) . Hardware platforms based on GPUs endowed with RTOSs cannot provide all control loops with equidistant sampling because of the presence of multiple tasks contending hardware resources. Furthermore in these platforms WCET is not analytically calculated for the inherent complexity of the code executed. Some latency and some jitter commonly considered in real-time systems are for example the interrupt latency (the delay between an interrupt and the activation of the appropriate routine) and its jitter (a random variation from one latency measurement to

another); the scheduling latency (the delay between the time a task is supposed to be scheduled and the time it is actually scheduled) and its jitter. The scheduling jitter is used to refer to sampling period variations. In literature, several works concerning real-time measures can be found.

A comparison among different RTOSs on different hardware is presented in [43], where three very popular RTOS based on Linux (RTAI, Xenomai and RT-Preempt patch) are compared. The three software solutions are compared also using three different hardware platforms, like Intel x86, ARM and PowerPC. These three hardware platforms are all commonly used in building embedded systems and the first (Intel x86) is the hardware platform chosen for the control systems that will be described in chapter 5 and chapter 6.

One of the hardware considered in [43] comprises a hard disk composed of a compact flash memory with an IDE adapter. The jitter is measured by generating a square wave signal on an I/O port through a real-time task and by measuring the time differences of several cycles. The jitter of the square wave period time has been measured varying from 2 μs to 15 μs on the x86 platform, depending on the load conditions of the CPU.

In [44] a single hardware platform was chosen (a VMEbus board with a MPC74755 PowerPC processor) and four software solutions are being compared: VXWorks, Linux, RTAI and Xenomai. The main variables measured are the interrupt latency and the communication delays through real-time Ethernet communication (means of communication will be analyzed in chapter 4) . The interrupt latency is measured recording with an oscilloscope the delay between an input signal that generates an interrupt and the output signal generated by the interrupt handler of the system. Jitter and interrupt latency resulted similar for all the four software solutions, although for the original Linux kernel the measures were proved to be strongly affected by workload. Thus RTAI and Xenomai have a registered performance which is very close to that of VxWorks. The measured delay varies from 69.2 μs to 73.2 μs showing a difference of 5 % between the fastest and the slowest and grading RTAI in the middle. The jitter of this delay is of 0.15 μs for RTAI (the lower) and of 0.50 μs for VxWorks (the higher).

Being RTAI strongly related to RTLinux, it is interesting to see also measurement of real-time performance of RTLinux. In [45] the measure of scheduling jitter on RTLinux is obtained by running a simple periodic task at 500 μs and logging its starting time stamps (for every cycle). The jitter measured was around 5 μs and some differences have been recognized in the way the timer is programmed: one-shot mode (the timer is reprogrammed for each cycle)

or pure periodic (in which the timer is programmed only at the first start) both preserving advantages and disadvantages.

Similar results are shown in [46] where RTAI, RTLinux and VRTXsa [1] have been compared on a Motorola Freescale PQ2FADS-VF equipped with a PowerPC 8275 CPU. RTAI and RTLinux are aligned in performance in all the tests.

3.4.1 Jitter scheduling measurements

All the previously presented tests were taken running real-time tasks in kernel space. RTAI offers also an interface for high-level tools and languages as MATLAB/Simulink and Scilab/Scicos to develop control systems [47]. In Matlab, the RTW toolbox generates C-code from a Simulink model without the need of any specific programming knowledge and the real-time code runs in user space. It is therefore interesting to show the according results obtained in user-space and kernel-space.

A simple task can be designed in Simulink to read the start time of each cycle in way similar to [45]. The jitter of the scheduled period is shown in Fig. 3.3. It varies inside a range of -10 $+10$ micro-seconds.

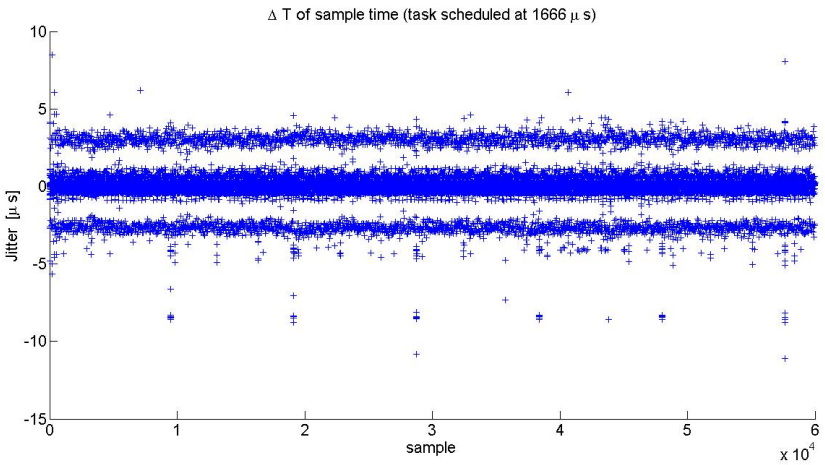


Figure 3.3: Scheduling jitter - Jitter in time scheduling of a single real-time task.

However, the test is representative only of the good or bad RTAI installation, as it does not take into account I/O signal processing and control activities: the task contains only one thread which does not compute anything. It was therefore decided to measure the period inside a full control code. This new test was carried out for a couple of hours. Indeed many anomalies

[1] Versatile Real-Time Executive (VRXT) isa a RTOS by Mentor Graphics Inc.

which can occur in a system endowed with an RTAI GNU/Linux operating system are related to very low-probability and sporadic events (which mean periods in the order of minutes). A few hours are sufficient to measure the real-time performance of an RTAI system correctly configured.

Fig 3.4 shows the probability density function of the random variable Ts (sampling time) of a control task scheduled to run every 1 ms. The difference between the designed duration of the cicle and the actual duration is measured reading an internal timer through the *rt_timer_read* RTAI function. The test was performed for the duration of a couple of hours (ten million loops of 1 ms); 11 I/O channels were active, as in [48].

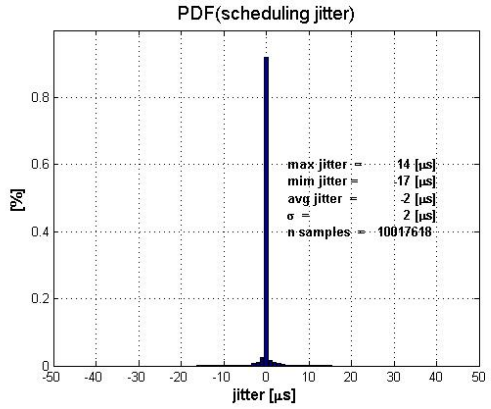


Figure 3.4: Scheduling jitter pdf 11 I/O - Probability density function of the scheduling jitter on a Pentium 4 system with 11 I/O channels.

The same control task (a repetition of the scheme shown in Fig. 3.1) was expanded with additional I/O activity adding 50 I/O channels (both analog and digital). Results are shown in Fig. 3.5.

Finally, a 100 I/O channels control system with additional computation instructions was measured. Results are presented in Fig 3.6

As a result it has to be considered that to I/O activity strongly affects the worst case sampling period which has increased form 14 μs to more than 200 μs.

The jitter can also be measured through an oscilloscope printing the output of a squared wave. From a Matlab model a squared wave with a frequency of 300 Hz and a duty cicle of 50% is generated and it is output through comedi drivers on a digital board 3.7.

The squared wave is then recorded with an oscilloscope and can be used to test the real-time execution of the control.

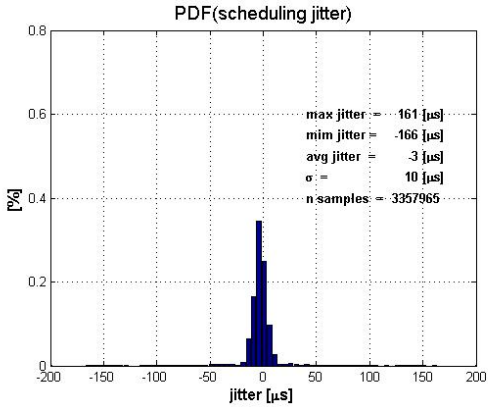


Figure 3.5: Scheduling jitter pdf 50 I/O - Probability density function of the scheduling jitter on a Pentium 4 system with 50 I/O.

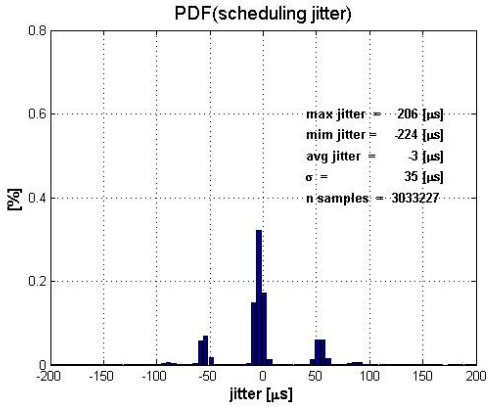


Figure 3.6: Scheduling jitter pdf 100 I/O - Probability density function of the scheduling jitter on a Pentium 4 system with 100 I/O.

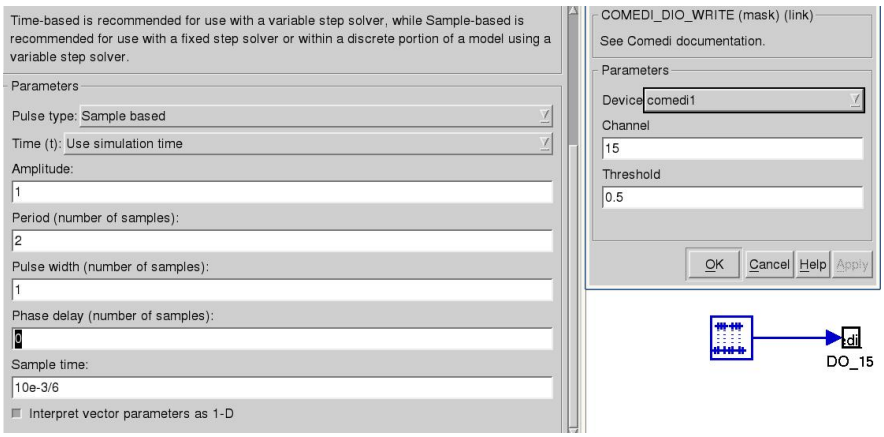


Figure 3.7: Square wave model - Simple Matlab code to generate a squared wave

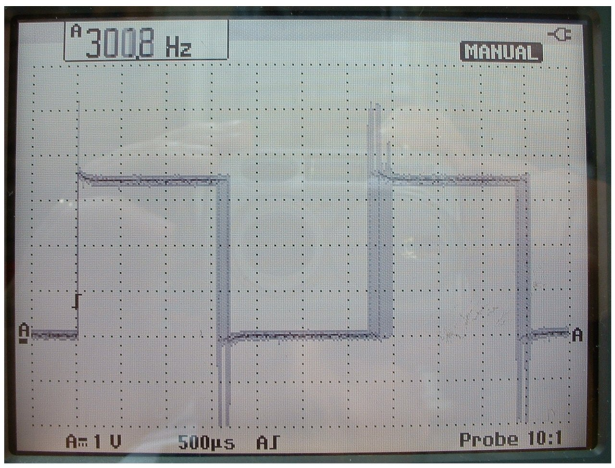


Figure 3.8: Square wave output - Registered squared wave.

3.4.2 Results analysis

The above presented results show that the latency is strongly dependent on the I/O activity and the complexity of the control code. Moreover with a considerable number of I/O lines the worst case (whose probability is in the order of one case out of a million) is less than 10% of the sampling time and it can be considered acceptable. Only in the third case presented, adding computation load to I/O activity, a worse case in the order of the 20% of the sampling time could be measured and also in this case the positive factor is that the probability of this worse case is extremely low (under 10^{-5}).

This shows that an RTAI system is suitable to control devices with several physical variables to be measured. The SART device that will be presented in chapter 6, embeds several logical functions normally implemented with programmable logic controllers (PLCs), and therefore needs to read several logical variables from the field.

Shown results increases the appeal of this solution in all those situations with a consistent number of I/O lines. The control designer must take into consideration that the I/O activity modifies the real-time performance of the system, also when this I/O activity is performed through real-time drivers. Therefore the latency test should be carried out not only with a different load activity (as it has been reported by literature) but also in consideration of the I/O channels requested by the specific application and the complexity of the control code. In

Fig. 3.6 the two symmetrical peaks in the probability jitter suggest a common origin. The same pattern can be observed also without I/O activity (it is not shown here but this case has been also measured) and its origin can be addressed to the cache access, in scheduler decisions and in the Pentium architecture [45].

3.4.3 Reading sinusoidal waves

It is of practical interest the effects of the jitter while reading sinusoidal waves at industrial frequency (50 Hz). As previously reported the scheduling jitter varies among 5 μs, to tens of μs . To develop a control excitation system of a synchronous generator, a three phase system of currents and voltages are read. With twelve samples in a period at industrial frequency (i.e. 50 Hz) a sample time of 1.666 ms is obtained. Two sinusoids synchronized and offset by 120 degrees from each other are read (calculating the third one), and a mean value of the maximum amplitude is calculated with the following expression:

$$V = \frac{2}{3}[V_M \sin^2(\theta) + V_M \sin^2(\theta - \frac{2\pi}{3}) + V_M \sin^2(\theta + \frac{2\pi}{3})] \tag{3.1}$$

$$= \frac{2}{3}V_M + \frac{2}{3}V_M[\cos(2\omega t) + \cos(2\omega t - \frac{2\pi}{3}) + \cos(2\omega t + \frac{2\pi}{3})] \tag{3.2}$$

Therefore an average value of the maximum value is obtained plus a disturb component at a frequency double than the initial one. The value is then filtered with second order low pass filter with a cut-off frequency of 40 rad/sec. The chosen cut off frequency permits to attenuate the noises although not limiting the control bandwidth, which, for the control detailed in chapter 5 and 6 is far beyond 40 rad/sec as shown in chapter 2.

In Fig. 3.9 it is shown a sampling activity test for a misconfigured PC. The ripple on the filtered voltage is more than 0.4%.

In Fig. 3.10 it is shown a sampling activity test on a well configured PC where the jitter of the scheduling time is very low. The ripple on the filtered voltage is less than 0.02%.

3.5 RTAI applications

Important laboratories in different areas of physics research have tested RTAI. Elettra synchrotron light source in [49] presented their front-end architecture control system based on Linux and on Linux patched with RTAI for those tasks requiring hard real-time capabilities. The main advantages recognized are the possibility to run Linux (and all its services) as low

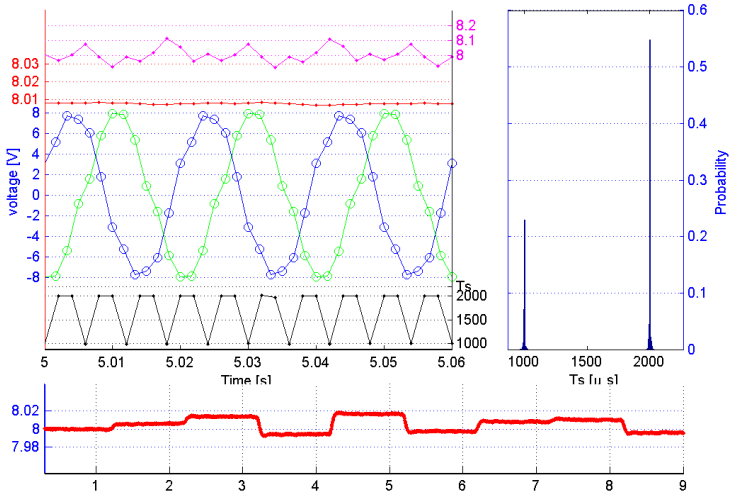


Figure 3.9: Three phase voltages - Sampling of a three phase voltage. In the middle two sinusoids read, bottom the sampling period, upper $v = \frac{2}{3}(v_{rs}^2 + v_{rt}^2 + v_{ts}^2)$. In red the filtered measure. On the right the probability distribution function of the sampling time

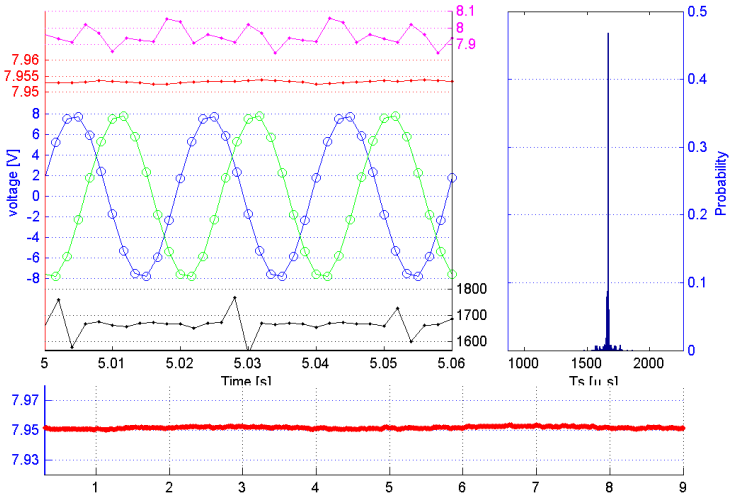


Figure 3.10: Three phase voltages - Sampling of a three phase voltage. In the middle two sinusoids read, bottom the sampling period, upper $v = \frac{2}{3}(v_{rs}^2 + v_{rt}^2 + v_{ts}^2)$. In red the filtered measure. On the right the probability distribution function of the sampling time

priority tasks. Their measures of latency on PowerPC VME boards shows a maximum response time for an interrupt of 24 μs with an average of 9 μs. In [50] it is stressed how the adoption of a GNU/Linux platform for the booster control system opened up the possibility to develop a single code base for different hardware platforms. For some applications, the real-time performance of RTAI are suitable to perform feedback control algorithms with no need of a dedicated Digital Signal Processor (DSP) board [51].

At EFDA-JET (a European joint venture research centre on nuclear fusion) for tokamak real-time systems, the use of i386 platform based on Linux and RTAI have been investigated [52], as an alternative to the existing architecture based on the commercial operating system VxWorks.

Other applications in the motion control field can be found in [53], where the principal author of RTAI shows the main characteristics of RTAI and some application examples. In [54] and [55] the major benefits of RTAI are recognised in the possibility to rapidly develop prototypes of control algorithms for servo-mechanisms.

Reference [56] presents a system to detect, record and transmit electrical and climate data from a photovoltaic field. HRT signal processing is utilized to sample voltage and current waveforms, while the Linux open architecture assures an extremely high flexibility of utilization.

3.6 Controller design with RTAI

A model-based design of a control system includes several phases which have to be repeated a number of times to achieve the performance requested by the controller. From the specification of the whole system and the plant modeling of the system a design of the control is developed. After a successful simulation of the control synthesized, through its implementation, an experimental test can verify the results and eventually restart the process by modifying one or more of the previous activities as sketched in Fig 3.11.

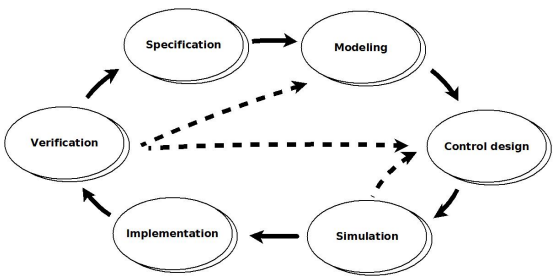


Figure 3.11: Model based design - Control system design methodology.

There are several integrated platforms where users can work in a unique environment and the implementation phase is essentially an automatic generation of code.

Although it is possible to use RTAI without the high level tools (as described in [59]) just taking advantage of its rich programming interface (as described in [57] and in [58]) the cyclic consequentially-linked development process (outlined in Fig 3.11) finds an ideal platform when a Linux RTOS (e.g. RTAI) is used in combination with a commercial Computer-Aided Control System Design (CACSD) software (e.g. Matlab/Simulink or Scilab/Scicos).

The integration of RTAI with two of the main CASCD software (the commercial Matlab/Simulink property of Mathworks Inc. and the open source Scilab/Scicos [60]) is called RTAI-Lab project. RTAI-Lab is composed of some specific blocks and building options which can be used inside the graphical modeler of the CASCD software, and a generic graphical user interface (a GUI called xrtailab), to monitor the execution of the real-time code generated. For the code generation RTAI-Lab relies on the CASCD software (Real Time Workshop in Matlab). While traditionally the controller design and the implementation of the controller are two separated phases in the engineering process of a control system, with RTAI-Lab and RTAI the control engineer can immediately run the final implementation of the designed control.

After modeling the plant and the controller in the simulation modeler software tool, the automatic code generated is compiled on the final platform (Linux patched with RTAI) with the open source gcc compiler [61]. The executable code runs in real-time on x86 CPU (but also other hardware platforms can be considered if needed) and during run-time, the CACSD software used for code generation is no longer needed because the real-time task is statically linked to the needed libraries.

One advantage of automatic code generation is that it avoids errors in programming activities with lower-level languages.

Having chosen one of the diagram modelers and the simulator software, the model of the physical plant to control is obtained. A regulator is then designed and all the logic of the equipment is reported.

The whole model of the power plant as in Fig 3.12, its regulator and state machine are therefore simulated until the requested behavior is obtained as in the design specification.

Planning to generate the code from the model and to run the code on a real-time computer system (e.g. the Linux-RTAI on x86 platform), it is necessary to chose a fixed-step solver to simulate the model.

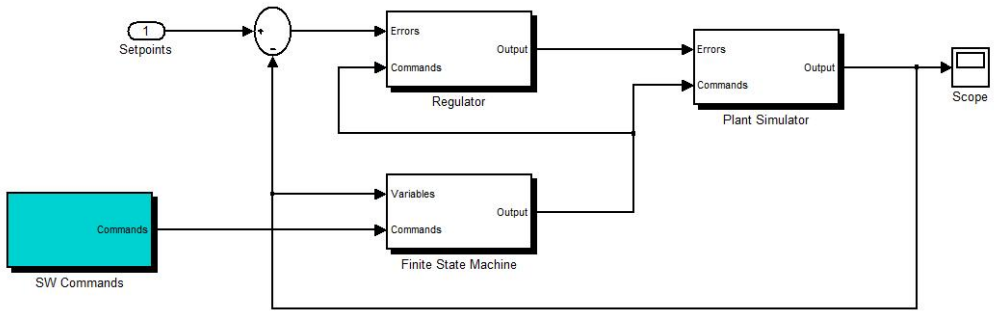


Figure 3.12: Control system model - Control system design simulation.

The I/O blocks have to be added from the RTAI-Lab library and the standard scopes have to be substituted with the RTAI-Lab scopes. Input from the hardware is selected instead of the simulator output and the output from the regulator is routed to the hardware I/O cards as shown in Fig 3.13

Once the code is generated and (eventually) transferred to the final hardware platform it can be run in real-time and experimental results can be compared with the simulations.

The I/O blocks assure that the signal adapting by encoding and scaling properly analog, digital and logical input signals.

3.7 Conclusions

From the literature on RTOSs, performance analysis show that Linux RTAI is comparable with other solutions on the market. Measurements carried on in our laboratories confirm the suitable performance of RTAI; it was shown how the jitter scheduling is dependent on the input output operations and complexity of the control code. For the control code developed and the physical variables sampled and controlled (i.e. electromechanical quantities of synchronous generators) RTAI on x86-64 hardware platform is suitable. The computational power of the hardware platform permits to integrate several embedded software applications on the same CPU. The complete control design methodology has been described. In next chapters the methodology presented will be applied to the development of excitation control systems for synchronous

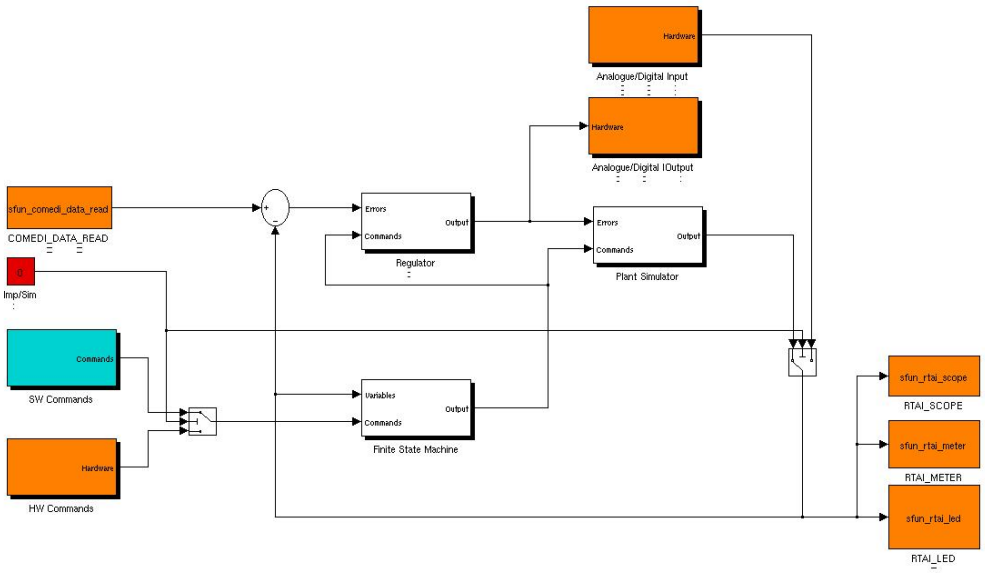


Figure 3.13: Control system design - Control system design simulation.

generators and reactive power regulators for power plant. Running the two control systems on the latest versions of Linux OS makes the devices fully programmable and easy to upgrade with new versions of hardware and software.

4

Communications

4.1 Introduction

The need for communication of the implemented devices is here described. Among all the different existing protocols used in industrial applications, the Ethernet protocols have been chosen . Literature shows that most of the existing industrial protocols converge in using the Ethernet. Ethernet performances are summarized in measurements reported in literature. The communication architecture is shown and its performance is reported. Finally, details on the interfacing with two industrial protocols are shown.

4.2 Communication Capability

A real-time control device should have several different communication capabilities. The real-time device may need to be inserted in an integrated control system such as a Supervisor and Control and Data Acquisition (SCADA) system, or a Distributed Control System (DCS) or to exchange data with other controllers in the system. Interconnecting to a SCADA system normally does not involve real-time communications, being the SCADA system mainly used for Human-Machine Interface (HMI) . Interconnecting to a DCS can be necessary to have real-time performance.

In this work three different applications of communications have been taken into consideration:

- control: real-time communications for the control itself to communicate with peripheral devices;

- protection: real-time communications for auxiliary functions (i.e. redundancy);
- monitoring: HMI communications.

One of the advantages of using a complete operating system like those described in chapter 3 to run a real-time task is the possibility to easily integrate several communication protocols.

For the two devices involved in voltage regulation as described in chapter 2, some examples of the first type of communication are the following:

- the transmission of the UP and DOWN commands from the reactive power regulator to the AVR;
- the voltage and current measures from a peripheral unit.

These types of communication need to be real-time types but have limited constraints about the protocol to be used: they can also be designed from scratch, being both sides of the communication part of the same device and under the same designer.

An example of the communications for auxiliary functions is the communication between a master unit and a slave unit to implement the redundancy of the CPU. The state of the regulator has to be copied to the slave CPU in a consistent way, but the real-time constraints are not too strict.

The communication of data to the HMI does not need real-time. The main difficulty in this kind of communication is the necessity to adequate to industrial standards. This can also be impossible to be directly implemented in the real-time platform used for the control device and there could be the need of some sort of bridge. As technology and industrial standards evolve, different protocols need to be implemented and therefore it is necessary to easily integrate the appropriate software libraries.

4.3 Communication system architectures

Several different communication technologies have been applied in distributed control systems: starting from serial RS-232 wired protocol to radio wireless protocols, thousands of different protocols have been developed and used so far. The convergence of computer systems and communication systems has strongly influenced the way computers interconnect [62] and has leaded to a progressive standardization of protocols.

Most of the networks are built as a stack of layers, each one interfaced with a higher level. The total set of layers and protocols is called the architecture of the network. The International

Standard Organization (OSI) proposed a standard model for network architectures [63] which is composed of seven layers .

A network architecture is the description of the specific implementation of all or some [1] of the layers in that specific architecture.

One of the most widely used network architectures came from the ARPANET and evolved in the Internet. The reference model of this architecture is often called TCP/IP [64] and can be viewed as an OSI model short of some layers as in Fig. 4.1.

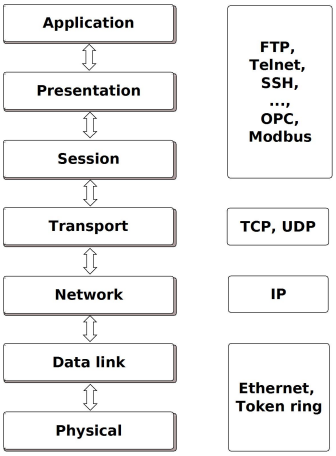


Figure 4.1: TCP/IP and OSI model - Standard OSI model and part of the TCP/IP protocol suite.

4.3.1 Industrial network protocols

Some protocols used for industrial communication were designed years before the OSI model was published, others pertain only some of the layers in the OSI model. Some of them are listed below:

- Token Ring is a standard (known as IEEE 802.5), commercially used by IBM since the seventies and regarding only the physical and data link layers. It is based on a special token which travels around a circular network (the ring), giving real-time characteristics to the communication;
- Profibus is an international standardized field-bus system developed by an international industrial consortium. It has been designed to transmit process data in industrial environments and is based on the presence of a master unit and several slave units and a

[1] In an architecture a layer can also not be used

token ring policy. Communication channels are parametrized, offering the possibility to setup at the configuration of the system;

- Modbus is a serial communication protocol developed for PLCs communications. Being openly published and royalty-free, it has been adopted by several leading companies in industrial automation and has been extensively used in the industrial field;
- CANOpen is a standard specifically developed for automotive industry. It is based on a multi-master architecture and serial communication. The medium access method is original;
- LonWorks was developed by a private company and standardized for control networking by ANSI (ANSI/CEA-709.1-B);
- WorldFIP is a European Standard (EN50170). It is based on a producer-consumer model where each producer transmit data at known time intervals obtaining a timeliness communication;
- P-Net is based on the RS485 standard using a shielded twisted pair cable. It is a multi-master bus where masters send requests to slaves and the right to access the bus is transferred from one master to another by means of a token with a cyclic mechanism based on time;
- InterBus-S is a serial fieldbus based on a cyclic transmission of data between master and slave devices;
- SERCOS (Serial Real-time COmmunication System) is a communication protocol designed for industrial motion controls and digital servo drives in numerically controlled machines and systems. It has been standardized in IEC 61491. The first two versions operated on a fiber optic ring while the latest version (named SERCOS III) is based on Ethernet.

In [65] five different protocols (CAN, FIP, Interbus S, Profibus and SERCOS) are being reviewed according to the specific application to electrical drives control for a steer-by-wire system. Physical characteristics of those protocols have been summarized.

Some of the different protocols developed are mainly used in specific applications and it is not uncommon to notice the presence of several of them in the same industrial plant. Solutions exist to interface devices based of different protocols.

One point in common is that in the last decade most of the network protocols have been interested in initiatives using Ethernet as a field bus, substituting or adding Ethernet to the proprietary and original field bus:

- Ethernet/IP is a built in module in several commercial PLC;
- Modbus/TCP is an evolution of the Modbus protocol carried on Ethernet;
- Powerlink is an implementation of CANOpen over Ethernet;
- PROFINET is an Ethernet based standard defined by the same organization developing, standardizing and maintaining the Profibus standard;
- LonWorks have several possibilities to integrate in IP environment.

The constant fall in prices in the IT market for Ethernet cards and the constant increasing in bandwidth performance are two key points of Ethernet success. Ethernet provides market-proven cost-effective hardware components due to its massive use in local area networks for office purposes. Therefore the use of Ethernet has been expanded to industrial automation and there is a consistent effort to integrate effectively the existing field bus systems with the Ethernet protocol [66].

4.3.2 The Ethernet protocol

One of the most used protocols for the physical layer in the TCP/IP model is the Ethernet protocol. Others exist (e.g Token Ring), but the Ethernet is the one which leads in Local Area Networks (LAN) . Ethernet is a commonly used term that indicates several different protocols and physical media that can be used and have been standardized as IEEE 802.3: it comprises communication over copper wires or coaxial cables as well as fiber optic links.

Two of the first media used for Ethernet were the thick an thin coaxial cable (formally known as 10Base5 and 10 base2). The media was shared among all the transmitters using a scheme named CSMA/CA (Carrier Sense Multiple Access with Collision Detect) . The principle of CSMA/CD technique is that all transmitting stations access simultaneously the media (the cable), each one can try to transmit data and can detect another station transmitting at the same time (a collision) while transmitting. When a collision is detected the transmitting station awaits for a random interval before trying to resend the data.

The presence of a random waiting time leads to a theoretically unlimited delay in transmission, thus it is not possible to calculate a worst case time for transmission and therefore CSMA/CD is not suited for real-time communications.

IEEE 802.3 protocols have evolved from the early Seventies to comprise different media as twisted pair copper cables, fiber optic cables. Also the protocols have changed to include different speeds in transmission (from initial 10 MBit/s to 100 Mbit/s and 10 GBit/s), including full-duplex data flow, extending the frame (the unitary set of data) size. All these improvements and the wide acceptance of the Ethernet technology exhibiting an exponential growth, led to efforts to mitigate the non real-time behavior of the CSMA/CD.

The major improvement towards an industrial use of Ethernet was the introduction of the Switched Ethernet. When twisted copper wires are used as media, the stations are connected through a central device called hub. This is a passive device that repeats whatever is received from an input port to all output ports connected to the stations. In Switched Ethernet the hub is no more a passive device but an active one, which identifies the destination ports and relays the data only to these. This avoids collisions involving traffic from different ports.

In 1997 the full duplex was introduced: each interface is capable of simultaneously transmitting and receiving remote traffic, eliminating the possibility of local collisions.

Ethernet switch and full-duplex transmission mean that data delivery among multiple stations happens without collisions as long as the destinations are different.

4.3.3 Real-time Ethernet

As already shown, the definition of CSMA/DA as Ethernet media access control leads to a non deterministic timing of Ethernet. Ethernet is non-deterministic only if collisions can occur and therefore to implement a deterministic Ethernet all collisions must be avoided. Switched Ethernet along with full-duplex communication and Quality of Service (QoS) to the MAC level work in this direction. Starting from the original standardized Ethernet protocol, several solutions have been developed to add real-time characteristics to Ethernet.

Some of the real-time solutions available to industry today are:

- EtherNet/IP,
- PROFInet, Profinet-SRT (Soft Real Time) is designed to achieve cycle time of 5-10 ms and works only on the software implementation. Profinet-IRT is for hard real-time and achieves 1 ms cycle time with an accuracy of 1 μs

- EtherCAT requires full-duplex, can use copper or fiber optic cables. It is based on a master slave principal: the master fully controls the slaves that do not initiate transmissions.
- ETHERNET Powerlink, also known as EPL, uses standard hardware and can deliver a cycle time of 200 μs with a jitter under 1 μs. It is based on a master slave principal: the slaves are polled in sequence by the master thus avoiding collisions. Non RT Ethernet devices cannot co-exist on the same segment not to compromise real-time.
- IEEE 1588 is a protocol to synchronize independent clocks running in separate nodes. It provides a method to higher protocols to make the Ethernet protocol more deterministic.

An update list that can be found in [67] shows 29 different solutions for real-time extensions of Ethernet.

Efforts have been made to guarantee determinism over off-the-shell Ethernet to work with any Ethernet adapter. An example is Rether [68] which is based on a token passing scheme that regulates the access to the network by passing a control token among the nodes on a Ethernet segment . RTnet [69] is a software framework to provide deterministic Ethernet that was already implemented on RTAI. RTnet is also published as open source under the GNU GPL, it provides a timeslot-based MAC discipline called TDMA (Time Division Multiple Access) and is based on a master slave architecture. RTnet has been extensively tested in [70] where it is used in conjunction with RTAI for distributed controls in plasma fusion devices. It is worth noting that RTnet requires a master station in charge of the network synchronization (i.e. Master station signals the starting of TDMA cycle to all stations, so that each station sends data only in its time slot) and in [71] drawbacks in term of computational effort for the master station are shown.

4.3.4 Ethernet in controls

In [72] a survey of several network protocol (among them Profibus, CAN and Ethernet) applications in motion control systems are presented. Although focused on legacy industrial protocol, it is stated that with the advantages of low cost, high speed and widely support, Ethernet will be the basis for open distributed motion control systems.

Being Profibus widely used for communication between PLCs and othe field devices, its counterpart using Ethernet protocol for the first two layers in the OSI stack called PROFINET, registers an analogue success in industrial automation. Performance tests on PROFINET IO (considered a possible replacement of PROFIBUS DP) to be used for implementation of slow

control systems for physics experiments have been reported in [73]. A cycle of fixed operation of input output is scheduled every 4 ms for each of the two stations involved and a latency of about 7 ms was measured with a considerable jitter of about 7 ms. It is worth noting that PROFINET protocol is based on Ethernet for the physical layer and on IP and UDP for the second and third layers of the OSI model.

In [74] a generic real-time Ethernet schema is proposed and analyzed in terms of implementation costs, compatibility with standard IEEE 802.3, configuration efforts and real-time performance.

In power systems, Ethernet has been already proposed in [77] and [78]. Simulations of the use of Gibabit Ethernet for substation automation are shown in [83].

4.3.5 Performance

Performance analysis of Ethernet is not an easy task. In [75] a low-cost distributed measuring instrument to measure timing characteristics of a real-time Ethernet is presented. To analyze network performance, Network Calculus [79] [80] has been applied to switched Ethernet [81].

Measurements of TCP and UDP data transfer throughputs [82] test how fast data can be sent between two nodes without any delay. This is not of interest in real-time controls where often the data to transmit is limited (e.g. commands to an actuator) and the interest is in timeliness of the transmission rather than in throughput.

Performance of both UDP and TCP protocols are measured in [76]. Two nodes equipped with ARM CPU and Linux OS (both kernel 2.4 and 2.6 have been tested) are connected through Ethernet. Packets are sent and the time spent in the nodes and in the network cables and switch are measured. The total transmitting delay was found of about 270 μs for UDP and of about 380 μs for TCP. As expected UDP protocol has better performance. Experiments show that the network delays is of about 12 μs for a data packet of 132 bytes sent along a cable of 8 meters of length with a network speed of 100 Mbps and therefore is only a minimal part of the total transmission delay. The previous data were measured as an average of thousands samples.

It is worth noting that in real-time the worst case has a central importance. Although often is not a good decision to design the control on the basis of the worst case (bringing to a resource waste), it is important to exactly know the worst case time communication. In [84] a worst case communication delay with a frame size of 144 bits and a switch connecting 24 stations has been calculated in 1.745 ms.

In [85] transmission delay and jitter are measured for non switched, switched and switched with priorities Ethernet. It is also shown the influence of external traffic in all three cases. The switched Ethernet with priorities shows a constant delay (around 100 μs) despite of the increment of traffic and a very low jitter (tens of μs). With low external traffic also switched Ethernet without priorities show the same performance.

The practical effects of both switched and non switched Ethernet delays in a motion control system has been shown in [86]. A delay under 1 ms was observed regardless the amount of traffic in switched Ethernet.

4.4 Communication architecture

Based on the above presented results a test of communication using a standard switched Ethernet (non real-time) was set up. Measurements of the end-to-end delay transmission time and jitter is below presented. "End-to-end", in this context, means between two real-time tasks developed with the methodology presented in chapter 3: a C code automatically generated from the developed Simulink model of the control compiled and executed in user-space. When using non real-time Ethernet one needs an interface between the real-time task and the TCP/IP stack of the operating system (in this case a Linux OS with a real-time kernel patched with RTAI) and therefore the communication architecture results as in Fig. 4.2

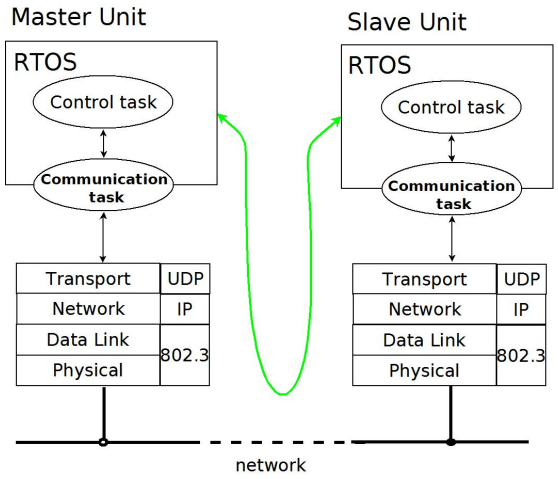


Figure 4.2: Real-time communication - Communication between two real-time tasks.

The network link can be made up of several different media: a cross Ethernet cable for two units, two cables connected to a switch, copper cables and fiber cables with appropriate

interfaces for long distance.

4.4.1 Communication task

The communication described in Fig. 4.2 is implemented through the communication task. The same task is used for most of the communications: between the central unit and the peripheral units, between the two units in a redundancy configuration and to the external logger. Therefore the communication task interfaces the real-time control task with other real-time tasks (as in the communication with the other central unit in case of redundancy and in the communication with the peripheral units) and also with non real-time tasks as the logger. The purposes of the communication task are:

- To receive data from the real-time control task;
- To send data through a socket to the receiving unit;
- To receive data from a socket;
- To send data to the real-time task.

The communication with the real-time task is accomplished through an RTAI mailbox, the data are thus copied into a shared memory which is shared between the real-time thread and the non real-time thread. It is a single-producer single-consumer configuration. The race condition is on a certain number of double variables: from 30 to 160 double values are written by the producer thread and are read by the consumer thread. The critical sections for each thread are listed:

Producer

```
for(i=0; i < n_doubles; i++)
{
   shm_data[i] = msg[i];
}
```

Consumer

```
for(i=0; i < n_doubles; i++)
{
  msg[i] = shm_data[i];
}
```

Executing the two pieces of code asynchronously (i.e. the producer and consumer each work in their own thread and therefore readings can be concurrent with writings) can lead to inconsistent data because reading an writing a double is not an atomic operation under the x86 hardware platform (it can be stated that is not an atomic operation under most of the hardware platforms equipped with moder 32 or 64 bit processors).

A lock-free code for the single-producer single consumer problem can be written using some atomic read-write primitives provided by the hardware. Unfortunately, although all modern CPU provides some atomic data, this is not uniform on the different hardware nor it is uniform on different C compilers. The risk is to write a not portable code or, even worse, an incorrect code.

Other solutions exist in literature to write lock-free codes without using atomic primitives, but often it is difficult to prove the correctness of the code.

Therefore, although it is possible to write a lock-free code to solve the problem, a more traditional solution with a semaphore was adopted. With a semaphore it is easy to implement a mutual exclusion preventing that the two processes use the shared memory at the same time.

A semaphore is created in the main code of the communication task and is used to implement the mutual exclusion for the two critical sections.

Producer

```
rt_sem_wait(sync_sem);
for(i=0; i < n_doubles; i++)
{
   shm_data[i] = msg[i];
}
rt_sem_signal(sync_sem);
```

Consumer

```
rt_sem_wait(sync_sem);
for(i=0; i < n_doubles; i++)
{
  msg[i] = shm_data[i];
}
rt_sem_signal(sync_sem);
```

Moreover lock-based synchronization has its counterindications in priority inversion and deadlocking. Considered that the execution of the critical sections shown above is very fast, the problem of priority inversion can be considered negligible. The problem of a deadlock caused by the death of one of the two threads while holding the semaphore is in any case detected with the interruption of the communication. As will be shown in chapters 5 and 6, this will cause the slave unit or the AVR served by the communication channel in fault going out of service. Every communication channel has its own communication task and therefore it cannot happen that a fault in one task stops another one.

4.4.2 Round-trip measurement

To measure delays of a packet transmission appears necessary to perfectly synchronize the two units. As shown in [85] and [87], to measure the total transmission delay from one real-time task to another, the round-trip principle shown in Fig 4.3 can be used.

In the tests carried out, a round trip time of about 400 μs was measured with a jitter around 100 μs. Having set a control cycle of 1.666 ms, a transmission was able to be completed for

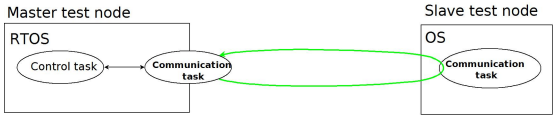


Figure 4.3: Roundtrip measurement - Measuring application level transmission delay.

each cycle. In the distributed SART, which will be considered in detail in chapter 6, several different units can be connected (at the moment the biggest power plant in which a SART system has ever been applied counts six generator units), therefore it was decided to limit the rate transmission to 10 ms. The data pass every control cycle from the control task to the communication tasks but from here, the data are forwarded by UDP packets with a rate that can be set at runtime. The same communication task, set with a lower transmission rate, is also used for other non real-time communications: the UDP packet is sent each second to the SCADA system.

In the communication between master and slave units as they will be described for the SART device, 30 doubles are transmitted from master to slave and 30 doubles from slave to master every 10 ms. It means a transmission rate of less than $0.2Mbs$ for each channel.

The defragmentation of IP packets was avoided with consistent configuration of stations TCP/IP stacks (i.e. avoiding the transmission of data exceeding the standard packet size). A central unit with six peripheral units, each of them transmitting 30 doubles, means receiving 1.2 Mbps, thus quite lower than the Ethernet bandwidth.

4.5 Redundancy in communications

A first grade of redundancy in communications over Ethernet can be implemented through trunking or link aggregation. This gives the control device the ability to survive a cable or network card failure. It was implemented using the bonding or teaming features already presented in the TCP/IP stack in the standard Linux OS. Switches and fiber channels between the switches remain single point of failure. Normally Ethernet Switches furnish a double fiber link, but in case of several peripheral units, the cost to have a double fiber channel link for each one is unaffordable. New solutions can be found on the market to have a full redundancy. In the ring topology, a number of switches connect together to form a ring. The ring network requires that each switch supports a redundancy protocol. The redundancy protocol avoids messages traveling around the ring indefinitely. It is worth noting that industrial solutions exist based on standard Ethernet: this means that the ring topology is transparent to the control.

4.6 Industrial protocols

Interfacing SART device with power plant control systems (e.g. DCS and SCADA systems) required the implementation of higher level protocols. Two different protocols were used: OPC DA and Modbus TCP. Both are standard protocols in industrial applications based on TCP/IP. The implementation of these communications takes great advantage from the used RTOS based on Linux and the possibilities to use commercial and open source software libraries.

4.6.1 OPC-DA

OPC is a collection of open standards for the communications in industrial automation. Originally the name OPC stood for OLE for Process Control, being a standard to access data with the OLE technology (Object Linking and Embedding) using DCOM protocol (Distribuited Component Object Model) from Microsoft. DCOM provides a mechanism for transparently executing function calls across computer systems. Nowadays, although some versions of OPC are still based on DCOM for remote procedure calls, the name OPC refers to Open Productivity and Connectivity and it is no more linked to the DCOM, which was substituted by Microsoft with the .NET framework. Therefore now OPC refers to a wide family of protocols based on open standards (and no more on the proprietary DCOM) called OPC Unified Architecture [88].

Although the new protocol architecture OPC Unified Architecture has already been defined, the most widely used protocol of the OPC family in existing industrial plants is the OPC-DA (Data Access): it deals with the communication of real-time data from production devices like sensors, instruments and PLCs to HMI, DCS and SCADA systems. Every item (e.g. a physical variable measured) transferred under the OPC-DA protocol carries three attributes : a value, the quality of the value and a timestamp. An OPC client makes requests of data to an OPC server: as an example, the SCADA system of the power plant is a client that requests data to the SART system which represents a server.

Several commercial implementations of the OPC-DA exist and several development kits to write an OPC-DA server on Windows OS are available.

The difficulty to implement an OPC-DA interface for the SART system (running on Linux OS) is that the OPC-DA protocol is still based on the DCOM technology and DCOM is a proprietary middleware based on the Windows OS. At least one implementation of DCOM on Linux existed from Software AG but has never been released for production use. An OPC development kit to write OPC-DA servers on Linux used to exist but was dismissed.

The OPC standard comprises also a protocol named OPC XML-DA to access data through an XML protocol and therefore without using the DCOM middleware. Several different commercial implementations of the XML-DA protocol on Linux exist on the market.

For this reason there are several ways to implement an OPC-DA interface for the SART controller. The first one is to develop an XML-DA server on Linux and to connect this to the controller real-time task as in Fig. 4.4

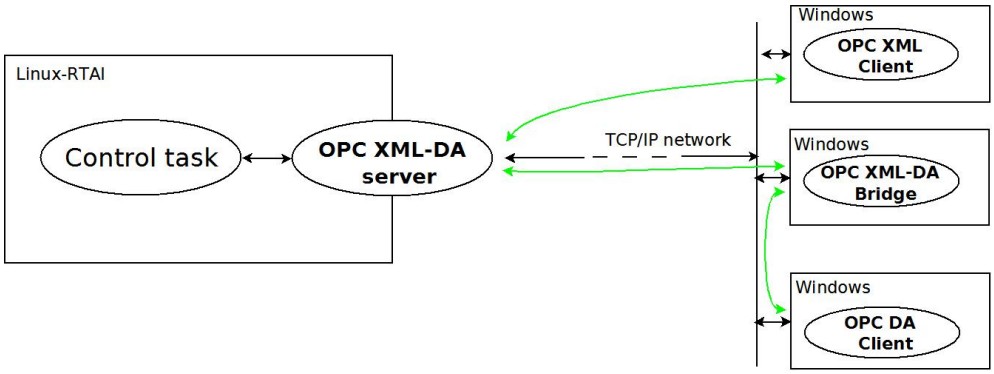


Figure 4.4: XML-DA protocol - OPC interface through XML-DA bridge.

Points of strength are:

- the XML-DA server running on Linux depends only on a library and the code is very easy to maintain;
- OPC XML-DA client can directly connect to the Linux-RTAI controller without other intermediates;
- OPC XML is an open protocol;
- firewalls can be easily configured to secure the communication

Points of weakness :

- the communication is slow (it is better to avoid polling the data with a period shorter than 500 millisecond) although sufficient for SCADA and HMI;
- the XML-DA protocol is not very common in industrial plants mainly because of its poor performance, .

Another implemented solution, was to interface the control task to an OPC-DA server running on Windows. The communication between the OPC-DA server was set up following

the same protocol detailed in section 4.4. The OPC-DA server can be implemented with one of several commercial solutions on the market or using an open source library as Light OPC [89].

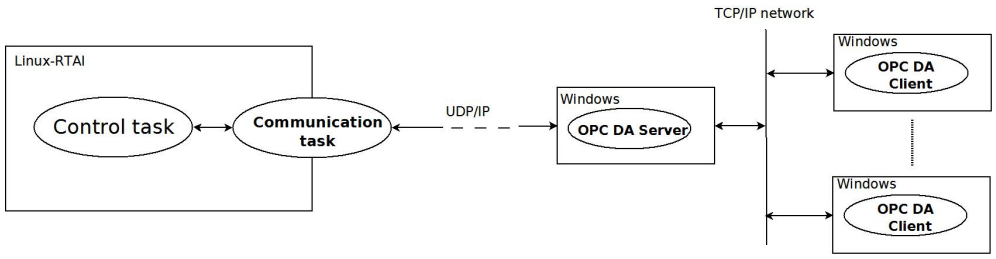


Figure 4.5: OPC DA protocol - OPC interface through OPC-DA server.

In this architecture the communication is faster than the previous one and the internal network is completely separated from the industrial plant network.

4.6.2 Modbus TCP

The communication protocol named Modbus was born in 1979 by Modicon, a company now owned by Schneider Electric, a French global company. Many variants of the Modbus protocol exist. The original version was a serial communication standard over copper lines, which was extended to be used over TCP/IP networks. The main reasons for using Modbus extensively in the industrial environment are the fact that it was openly published, its use is royalty-free and it allows an effective communication while remaining easy to implement and maintain.

The Modbus protocol is based on a master-slave architecture: master devices start the communication and essentially ask for data or send commands to slave devices. Slave devices can be sensors or actuators.

The operations permitted and the data types used by the Modbus protocol are rather simple: setting and reading registers containing integers (8, 16 and 32 bits) and floats (extensions using doubles also exist).

An open source library for Linux was chosen called libmodbus [90].

On the market there are devices available which can measure voltages and currents and can actuate commands (acting on a switch) using the Modbus protocol.

A communication test was carried out and it is described with Fig. 4.6

A digital signal was sent to an oscilloscope through a digital output from a real-time task. The same signal was sent via Modbus protocol (using Ethernet over copper cables and optical fibre cable and appropriate converters) to a Modbus device in which a coil (the digital signal

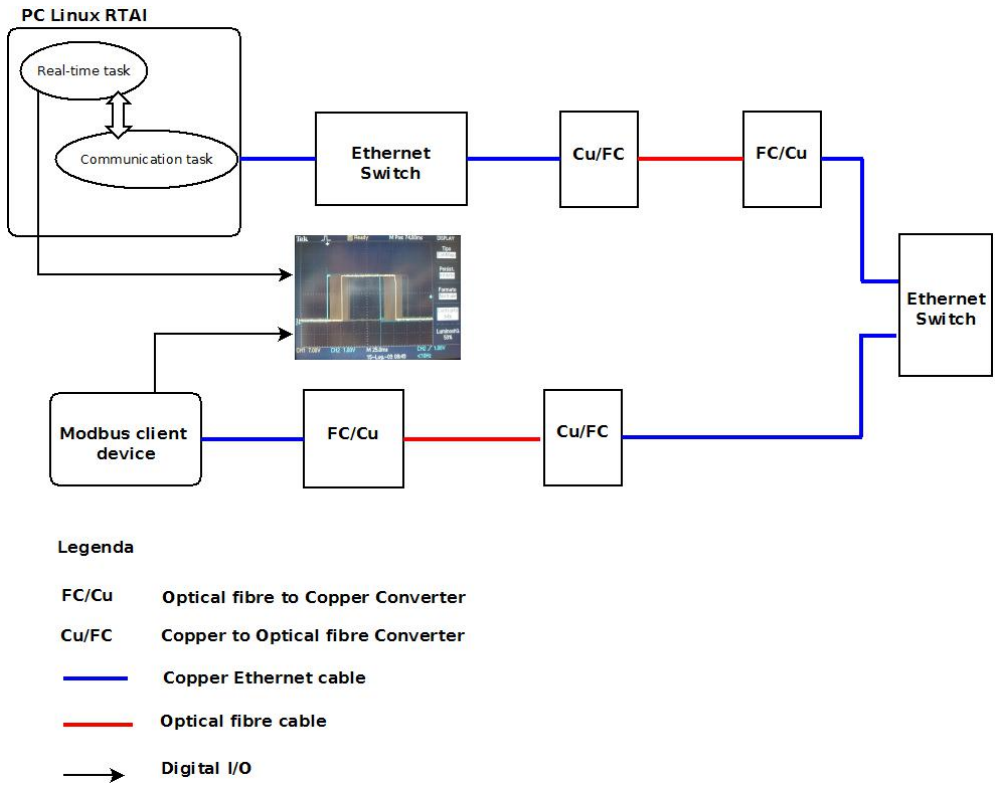


Figure 4.6: Modbus communication - Test bed for Modbus communication.

in the standard Modbus) is commanded. The output from the Modbus device is output to the oscilloscope.

A transmission time of about 25 milliseconds is registered with a maximum jitter of ±20 milliseconds. This is considered adequate to transmit a PWM signal with frequency of 1 Hz (this is the frequency normally adopted for the UP DOWN pulses to the AVRs).

4.7 Data recording

The two control systems implemented have the ability to record various variables. The recording functionality is implemented through the communication task aforementioned. The data logger built has the possibility to send the data through the network or to save the same data in a local file (e.g. on a local usb pen drive). All experimental data shown in chapter 6, were collected using the described software.

4.8 Conclusions

The requirements for the communications of the two control devices to be used in power systems have been shown in detail. A review of technologies and protocols most used in industrial applications have been presented. An increasing interest on using Ethernet was noted. Switched Ethernet along with full duplex communications open to the possibility to use a standard Ethernet for soft real-time communications. The results are that Switched Ethernet can be used in certain cases (i.e. depending on the bandwidth control and on the number of devices to connect) because in such conditions can provide real-time guarantees for message transmission. Examples of interfacing with two of the most used protocols in SCADA systems have been presented: their development has effectively taken advantage from the software platform (a complete Linux system) and the incomparable software libraries available.

5

Excitation control system

5.1 Introduction

The basic task of an Excitation Control System (ECS) is to keep alternator terminals voltage within certain limits to ensure correct voltage ratings under various loads. In addiction an ECS performs other control and protective functions:

- it regulate the working point in such a way that the capability of the exciter and of the generator are not exceeded: field excitation current, terminal voltage, under and over excitation limiters are some commonly implemented functions in an ECS;
- it compensates the load controlling the voltage at a certain point of the system through the compound action;
- it improves the dynamic performance through the damping of system oscillations: this functions is called Power System Stabilizer (PSS);
- it protects the generator and the step-up transformers from damage due to excessive magnetic flux controlling the ratio of per unit voltage to per unit frequency through the V/Hz limiter.

Under different circumstances, alternators absorb or produce reactive power operating respectively in under-excitation or over-excitation mode. This control is called excitation control and contributes to the stability of the individual generator and of the overall transmission or distribution system of the electrical energy [2].

Technical specification for functionalities requested of an ECS can be found in [91] regardless of the technology adopted for the implementation.

An ECS requires HRT signal processing and it was first implemented with analog electronics and dedicated digital processors or microcontrollers. The embedding of digital systems with DSPs to implement algorithms for active and reactive power control of synchronous generators was reported in [92] [93].

Experience on the evolution of microprocessor technologies and their use to implement ECSs has consolidated and has been reviewed in [94].

In all industrial sectors there has been a wide and fast growth of applications based on microprocessor technology. Using digital computers for voltage control is a subject which dates back to the early 1970s but only in the 1980s has became more popular. The trend now is to integrate in one single chip a large number of tasks which in the past were performed by a number of external components often with different technologies to interface. This trend is mainly due to the incremented performance of microprocessors and the growth of open standards both for hardware and software.

The major benefits expected from microprocessors technology applied to ECSs were:

- a wider flexibility;
- reduced number of electronics components (i.e. boards);
- improvements in the user interface;
- enhanced control, alarm and protection functions;
- accurate settings and change of control parameters values;
- easy integration in the supervision power plant system;
- on line monitoring of control variables;
- the possibility to simulate for commissioning and test activities.

Features, functions, benefits and models of digital ECS appear in [95] and [96]. ECSs operating in the industrial production of electrical energy normally need to be integrated into Energy Management Systems (EMSs) or Distribution Management Systems (DMSs) as power station controls, supervisory and automation systems i.e. the DCS, the SCADA, or even into higher level grid-area voltage control systems, i.e. the SVR. Excitation systems of synchronous generators are an integral part of power plant automation systems and belong to the hierarchical voltage control architecture.

These interfacing capabilities can be implemented either into the DSPs or microcontrollers themselves, or adding dedicated hardware (PLCs, interfaces, communication units, etc.).

However, using a complete operating system brings advantages in terms of higher software tools and libraries, i.e. modeling software, windows interfaces and network communications. Moreover, it can integrate all the required functionalities in a more rational way and into a single device.

One emerging development strategy for realizing control systems is to utilize a GPP endowed with an RTOS as presented in chapter 3. A presentation of the implementation of an ECS follows, based on a platform made by a Commercial-Off-The-Shelf GPP, a Linux operating system patched with the Real Time Application Interface (RTAI) and its extension called RTAI-Lab .

5.2 ECS description

The block diagram of Fig 5.1 presents a conventional ECS block scheme: the voltage regulator drives (through the exciter) the generator, whose output voltage is fed-back through a measuring and filtering block (transducer), other functionalities as compound, PSS, under and over excitation limiter are implemented through additional signals feedback.

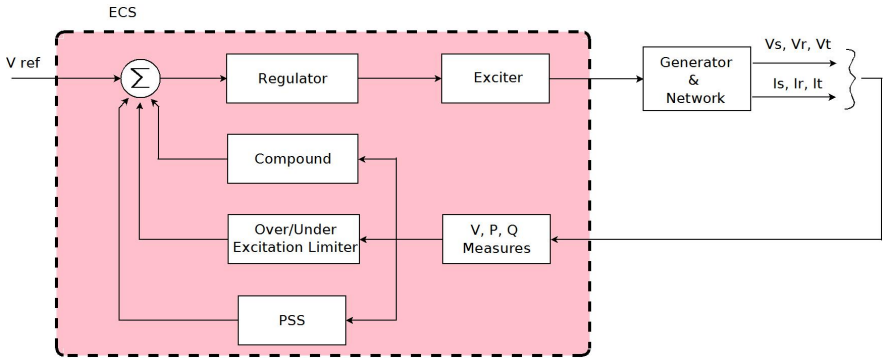


Figure 5.1: ECS scheme - Block scheme of an excitation control system.

In the developed ECS, several additional functionalities are added to the control code of the digital voltage regulator as new software modules, according to the block representation depicted in Fig. 5.2, which is described in the items that follow.

- A simulator of the physical plant (generator/grid), was generated from the mathematical model using a high-level software tool (e.g. Matlab/Simulink or Scilab/Scicos). As

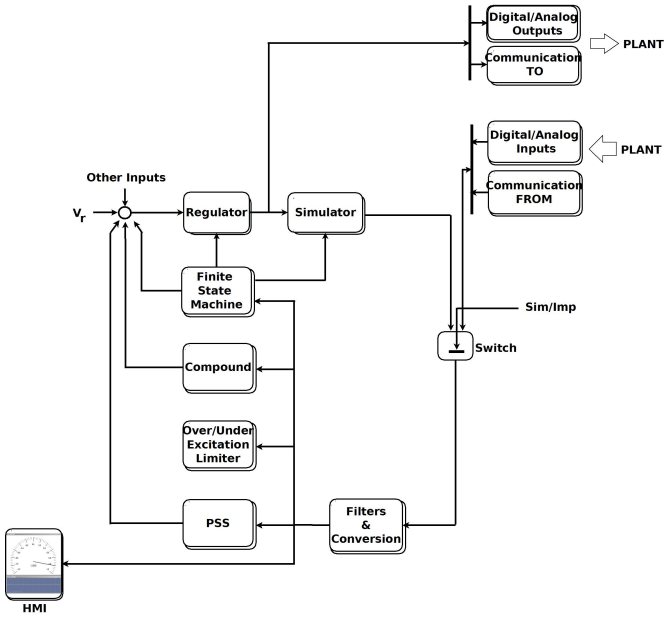


Figure 5.2: ECS functional scheme - Functional scheme of the ECS.

shown in Section 3.6, the control design is constituted of several phases that have to be repeated until the model shows the desired behavior; once the desired performance has been achieved, source files can be generated and an executable code is then compiled to run in the final hardware device. The simulator is never deleted from the control code and runs in parallel with the control algorithm in real-time. It can be used to facilitate factory commissioning, further maintenance or upgrade activities;

- A finite state machine realizes all the logic functions to be handled (start/stop sequences, protection functions, warnings and alarms);
- A voltage regulator is the proper control process and it is essentially implemented as a proportional integral type regulator.

In charge of the regulator and finite state machine blocks there are all the usual functions of an ECS: voltage control, reactive power control, line drop compensation, reactive droop compensation, power system stabilizers. Additional functions as the automatic synchronizer device, virtual instrumentation for real-time monitoring and data-loggers can be embedded, on demand, as software modules as well.

- The HMI, which can be realized using the RTAI-Lab extension or other suitable libraries;

- The I/O activities, which include drivers for both digital/analog I/O cabled signals and communications from/to DCS, SCADA, SVR, and so on. These I/O channels are implemented using digital and analog I/O boards (for cabled signals) or using network boards (for remote communications): as the hardware platform utilized is a PC computer, it is possible to use the widest range of I/O cards. For their importance, the use of remote communication functions is described in chapter 4.

The functional scheme in Fig. 5.2 will be further utilized also in chapter 6 to describe the reactive power control device for a power station. Both devices are implemented with exactly the same hardware and software platform, and they also share the same functional scheme.

5.3 ECS logic scheme

The internal logic scheme of an ECS is shown in Fig. 5.3.

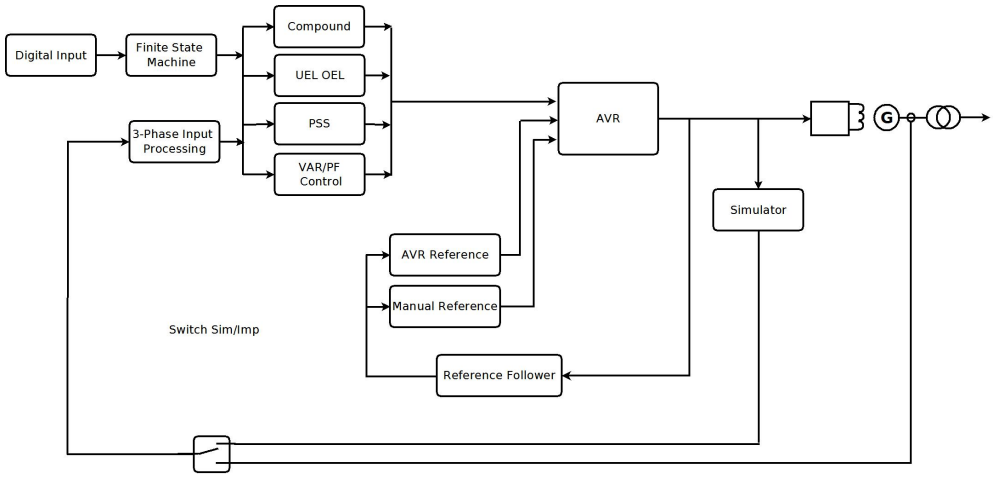


Figure 5.3: ECS description - Logic scheme of the ECS.

5.3.0.1 3-Phase Input Processing

Generator physical variables (currents and voltages) are read by the **3-Phase Input Processing Block** to obtain the quantities needed by the ECS: r.m.s. alternator voltage, active and reactive power. Digital sampling is fixed with a sample period of 0.02/12 seconds that corresponds of 12 samples per period when the frequency grid is 50 Hz.

5.3.0.2 Finite State Machine

The **Finite State Machine** block implements the control logic of the apparatus for the start and stop operations, synchronization with the grid and all protection functions and alarms.

5.3.0.3 Compound

Compound block implements two types of compensation of the generator voltage:

- line drop compensation: as voltage reduces due to the passive elements outside the generator (predominantly line reactance and transformer reactance), to maintain the voltage constant to the load when the reactive load increases, the excitation voltage should be increased. Therefore a signal proportional to the reactive component of the stator current is feedbacked together with the terminal voltage of the generator. The effect is that the terminal voltage increases with the reactive power delivered as in Fig. 5.4

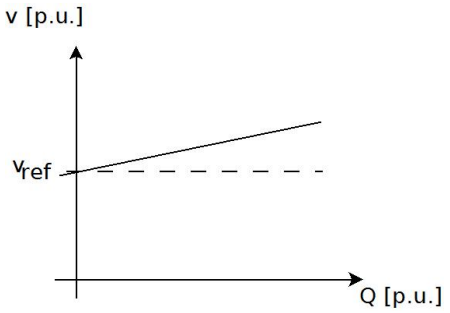


Figure 5.4: Drop compensation - Line drop compensation.

- reactive droop compensation: in power plants with multiple generators connected in parallel with the common MV busbar as in Fig. 5.5, a droop is introduced in voltage-reactive law as in Fig. 5.6

5.3.0.4 PSS

High gain AVR may reduce the damping torque that affect the oscillatory (small signal) stability. To increase the damping torque and therefore to compensate the reduction in damping due to the AVR, a supplementary signal can be provided [97]. An additional signal to the voltage regulator is provided by the Power System Stabilizer **PSS**. This additional signal improve the damping of electromechanical rotor oscillations of the generator. The implemented PSS function is a power-based stabilizer [97]. The power signal is positively feedbacked through

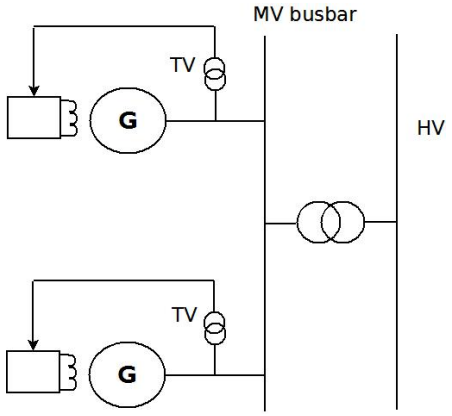


Figure 5.5: Common busbar - Parallel connection to common MV busbar.

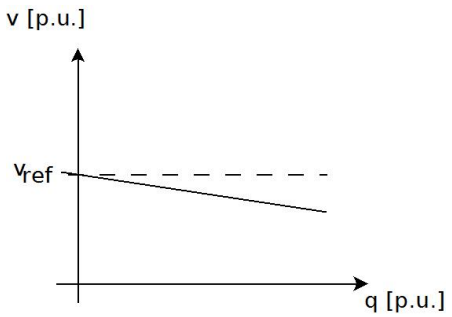


Figure 5.6: Droop compensation - Voltage-reactive power droop.

an high pass filter and a PID transfer function. The PSS module is intended to modulate the generator excitation so as to develop a component of electrical torque in phase with rotor speed deviations.

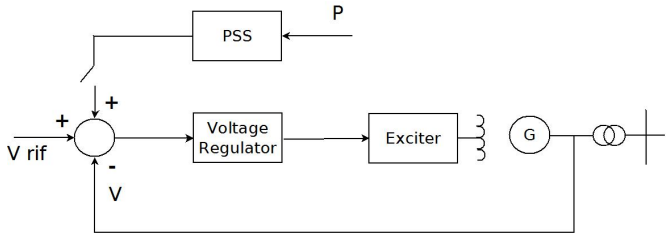


Figure 5.7: PSS - Generator under voltage control with PSS.

The PSS signal is limited to a $+/-0.05$[p.u.].

5.3.0.5 UEL and OEL

The limit value of reactive power is calculated using suitable functions of machine active power and voltage fitting the capability curves of the alternator. **UEL & OEL** block implements Under Excitation Limiter (UEL) and Over Excitation Limiter (OEL) control loops overlapping the voltage control loop. Capability curves are inserted as a set of point that are real-time interpolated as in Fig 5.8

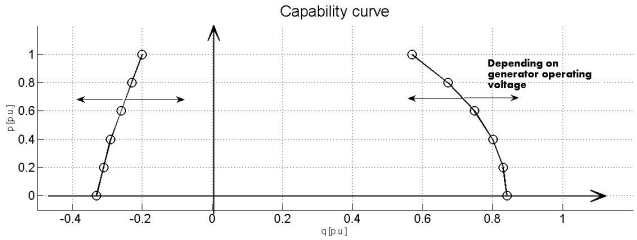


Figure 5.8: Capability curve input - Interpolate capability curve.

5.3.0.6 Var/PF Control

As required in certain applications, the voltage control loop can be overlapped by a **VAR control** loop to perform a reactive power control assuming as a reference a fixed set point or a value of reactive proportional to the active power of the generator (power factor control). VAR Control is also utilized to bring reactive power to zero during stop sequences for reducing alternator voltage transients at switchgear openings. A remote reactive level signal can be received from a remote control to insert the generator in a higher level control.

5.3.0.7 AVR Reference

The **AVR Reference** block outputs the setpoint of the voltage control loop. It receives the raise/lower commands, the grid voltage signal required to realize automatic voltage matching during synchronization and the Reference Follower block output .

5.3.0.8 Manual Reference

The **Manual Reference** block provides the field voltage set point in the manual control mode. This block receives, in addition to raising/lowering commands, the Reference Follower block output.

5.3.0.9 AVR

The **AVR** (Automatic Voltage Regulator) block implements a fast alternator voltage control loop. It is implemented as a discrete PID control algorithm. The PSS, Over- and Underexcitation Limiters and the VAR/Power Factor Control loops overlap the AVR control loop being slower than this.

5.3.0.10 Reference Follower

The **Reference Follower** block, which implements a null-balance between the AVR and Manual Reference outputs, realizes bumpless shifts from automatic to manual voltage control mode and vice versa.

5.3.0.11 Simulator

A **Simulator** of the alternator-grid system is embedded in the code. The simulator provides 3-phase voltages and currents as output and makes it possible to close the excitation control loop on signals generated by the simulator itself instead of real plant ones.

The simulator is a discrete implementation of an 8th-order model. The machine is modeled with a 3-phase stator, one field, an additional d-axis , and two additional q-axis circuits. The state variables result as follows: 2 from d-axis operator functions, two from q-axis operator functions, two from d and q fluxes calculations and two from mechanic equations. Magnetic saturation is included.

Therefore the mathematical model comprises the following equations :

$$c_m - c_e = T_a p \frac{\Omega(t)}{\Omega_n} \tag{5.1}$$

where c_m is the mechanical torque delivered by the prime mover, c_e is the electric torque expressed as

$$c_e = \psi_d i_q - \psi_q i_d \tag{5.2}$$

The stator flux is expressed in its $d-q$ components as:

$$\psi_d = \frac{1+pT_{AA}}{(1+pT_{d0}^{'})(1+pT_{d}^{''})} v_f - x_d \frac{(1+pT_{d}^{'})(1+pT_{d}^{''})}{(1+pT_{d0}^{'})(1+pT_{d0}^{''})} i_d^{'} \tag{5.3}$$

$$-\psi_q = x_q \frac{(1+pT_{q}^{'})(1+pT_{q}^{''})}{(1+pT_{q0}^{'})(1+pT_{q0}^{''})} i_q^{'} \tag{5.4}$$

where $i_d^{'}$ and $i_q^{'}$ are the i_d and i_q corrected to take into account the saturation effects. When the statoric conductor resistance is neglected, the generator voltage can be expressed as:

$$v_d(t) = \frac{1}{\Omega_n} p\Psi_d - \frac{\Omega(t)}{\Omega_n} \Psi_q \tag{5.5}$$

$$v_q(t) = \frac{1}{\Omega_n} p\Psi_q + \frac{\Omega(t)}{\Omega_n} \Psi_d \tag{5.6}$$

5.4 Redundancy

Control systems for generators require to have high integrity and high availability. Several architectures can be adopted to achieve a higher level of dependability. An example applied to an ECS can be found in [98] where a triplex modular redundant architecture is shown. Three channelled subsystems, fully active and with equal authority, are coordinated by a so called median authority unit to derive a single control signal based on a majority principle.

The here presented ECS has been realized with a redundant two-channel structure as in Fig. 5.9.

Two digital control units are here working in parallel, receiving the same signals from the plant. An arbiter logic function sets one of the two controllers as the master and the other as the slave. The two controllers communicate via an Ethernet channel and exchange information with each other: to assure a bumpless transfer between the two controllers, the slave continuously copies the state variables (both numerical and logic) memorized by the master.

The communication channel is implemented as a full-duplex Ethernet communication over a cross Ethernet cable.

From the ECS control task running in the master unit, the state variables are copied into a buffer and from the buffer an UDP datagram is formed and sent to the slave every ten

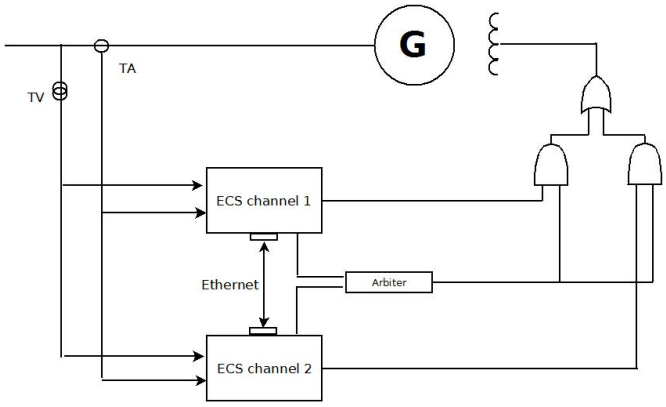


Figure 5.9: Redundancy principle - Principle of redundant ECS.

milliseconds, as shown in Fig. 5.10.

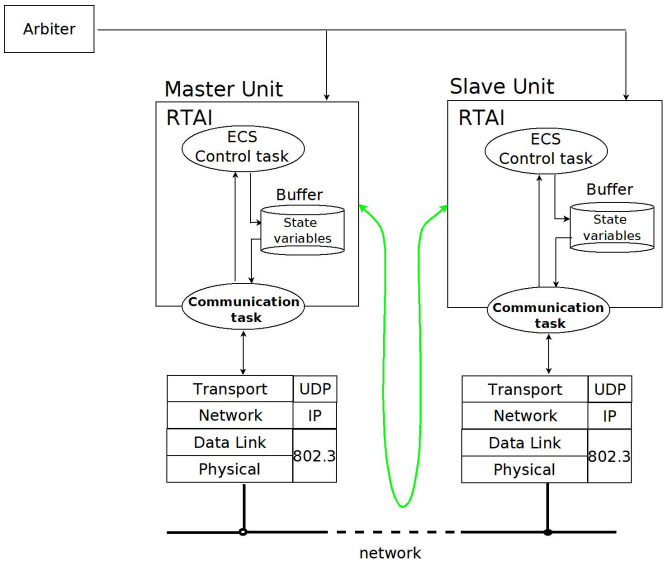


Figure 5.10: Two channel communication system - Communication scheme for control unit redundancy.

As detailed in chapter 4, a non real-time Ethernet was chosen for the communication channel. Therefore it is necessary to decouple the real-time control task from the non real-time communication task where the UDP datagram is formed and sent to the network driver through the TCP/IP stack. A simple buffer in shared memory was chosen.

The transmission of the UDP packet with the state variables is scheduled every 10 ms. This means that state variables are copied every 6 control cycles.

The state variables copied are the state variable of the following control loops: VAR/Power

factor, Over and Under excitation Limiters, AVR.

5.5 Conclusions

The structure of a digital ECS, implemented on the HW/SW platform presented in chapter 3, has been shown. The functional scheme of the ECS is the very similar to that shown for the SART system in chapter 6. Also some of the communication features presented for the ECS have been the basis for the extended communication capabilities of SART. The hardware and software platform is exactly the same for both devices.

6

Automatic voltage and reactive power regulator

6.1 Introduction

Italian grid code forces power stations for the use of an automatic system connected with the national secondary voltage control centers for regulating reactive power and voltage. This control apparatus is called SART (Sistema Automatico di Regolazione della Tensione). The complete new architecture of this device, along with the implementation using Linux-RTAI RTOS is presented. Experimental data of some commissioning tests carried on some power plants are shown.

6.2 Hierarchical voltage control

To improve voltage control, several countries have implemented hierarchical systems to coordinate the management of reactive power resources. The main benefits recognized to coordinated controls of reactive power resources are:

- improvement of the voltage profile of all EHV nodes reducing the variation around the desired values;
- enhancement of system security by increasing the reserves of reactive power available to support the network during emergency conditions;
- increase of the active power transfer capability;

- better utilization of reactive resources and therefore reduced of total losses of the power system [99]

6.3 Coordinated Automatic Voltage Control in Italy

In Italy a coordinated automatic voltage control system was developed, which is now operated by TERNA (the Italian ISO). The national EHV transmission system is subdivided in three regions. Each region is subdivided in areas, and each area is characterized by a pilot node [13] [100] [101]. The system controls pilot node voltages through a hierarchical structure made of three control levels.

The first hierarchical level, referred as Primary Voltage Regulation (PVR), is constituted by the conventional generator voltage control loops that are closed by the Automatic Voltage Regulators(AVRs). The voltage references of the AVRs are controlled by the outputs of the higher level.

The second hierarchical level is referred to as SVR. It includes the reactive power control loops of each power station generator, which are closed by local Voltage and Reactive Power Regulators named SART. In each power plant the SART receives a reactive level from the Regional Voltage Regulators (RVRs) . This is the reactive power requested to each alternator and it is expressed in the percentage of the reactive power limit (as it results from the curves of alternators capability). The SART apparatus actuates the reactive level by generating UP/DOWN commands (pulse-width modulated or pulse-frequency modulated pulses) to the voltage reference calibrators of the AVRs.

The second level is completed by the pilot node voltage control loops, which are closed by the RVRs. A principle scheme representing PVR and SVR is shown in Fig. 6.1.

On the third hierarchical level, a Tertiary Voltage Regulator (TVR) establishes the pilot node voltage references on the basis of the algorithms' results aimed at maximizing the reactive power margins and minimizing the losses of the grid [13][100].

In Fig. 6.1 two regions are shown: region A and region B. Each region is composed of several power plants: some are participating in the SVR other not. At the moment in Italy all power plants with a nominal power higher than 100 MVA have to participate in the SVR and therefore need a SART device [104] connected with the SVR. Every region has several pilot nodes whose voltage is directly controlled by RVR. Each power plant can be composed of several generating

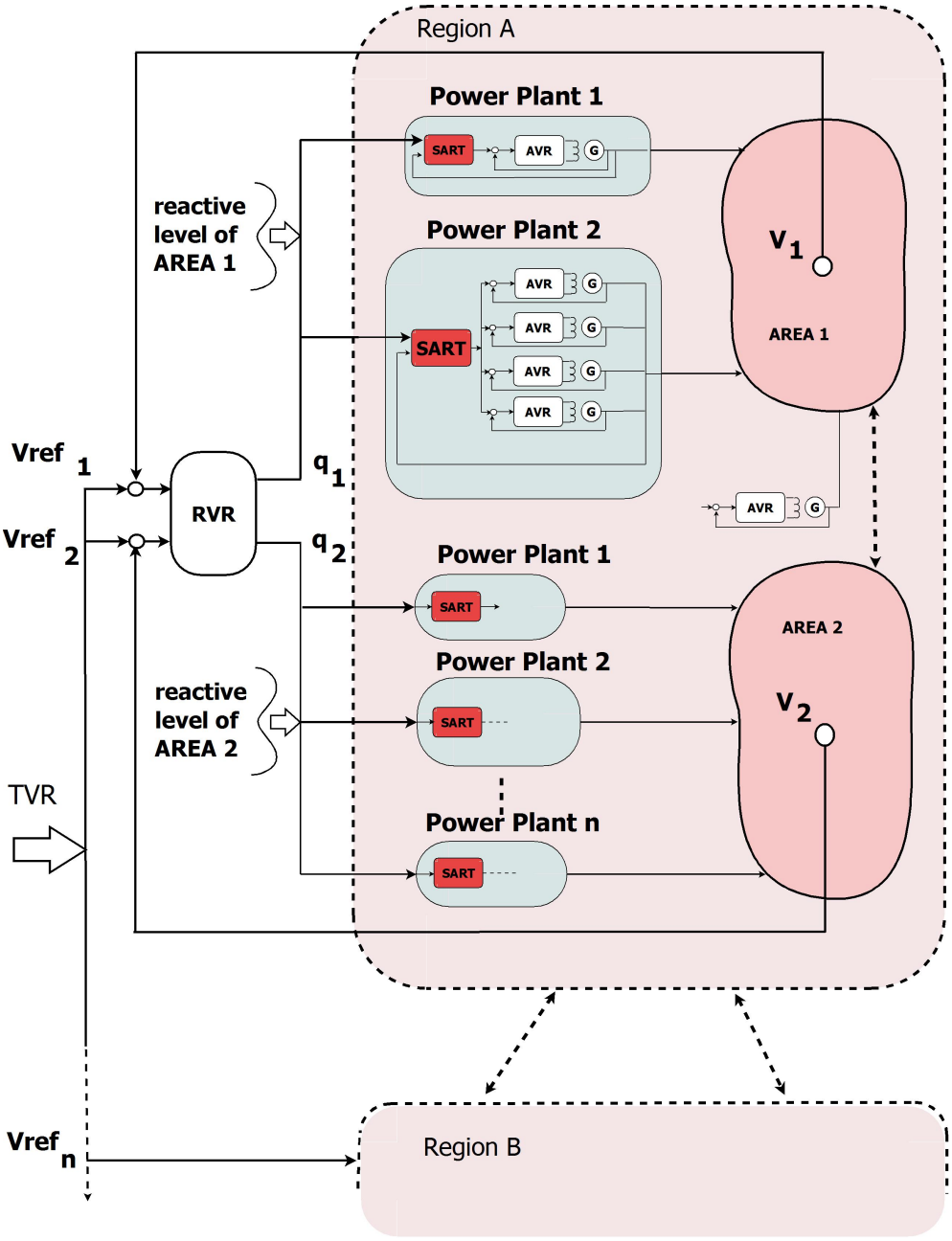


Figure 6.1: SVR - Schematic diagram of the voltage control hierarchical system. SART apparatuses are red colored.

units: the SART device coordinates the reactive power production among all the generators in the power plant.

In Italy the SVR was initially implemented by the Automatica Research Centre (CRA) of the former Italian Electricity Board (ENEL) in the late 1980s. In [13], recognizing the importance to maintain a suitable voltage profile of the transmission network despite of the continuous variations of reactive power requested by loads, the Reactive power Control Project was presented at ENEL (an Italian energy provider, formerly the national vertically-integrated state-owned company). A three level hierarchical control was defined. In [102] several technical details of the application of such distributed control are shown. In the first tests more than 30 power stations were equipped with local Voltage and Reactive Power Regulators, named REPORT, and three regional control centers were endowed with RVRs. These REPORT apparatuses are presented and their functionalities and commissioning tests are discussed in [101]. In November 2005 the code for transmission, dispatching, developing and security of the Italian grid (Grid Code) [106] entered in force, which regulates the relations between TERNA and grid users. Chapter 4 (Dispatching Regulations) of the Grid Code states that each power plant participating to SVR must be equipped with a new generation apparatus named SART, that must comply with specifications given in the annexed document A [104].

6.4 SART Description

During the three years of my PhD project, I have been deeply involved in the development of a new generation of SART apparatus. The device developed, named NewSART [105], presents a distributed architecture composed by the Central Unit (SART-CU) and the Peripheral Units (SART-PU). While the SART-CU is always the same in all the installations, the SART-PU can be substituted with different devices from different vendors: using other peripheral units can be necessary in some plants for customer requests. The dynamic characteristics of those devices (often not adequately reported in the technical specifications) must be checked.

6.4.1 SART Central Unit.

The SART-CU executes the real-time code that realizes all the following functionalities as embedded software modules, according to the functional scheme of 6.2. The main blocks are:

- A Regulator block which implements the main control algorithm: by receiving an input signal representing the reactive power requested by the RVR to the entire power plant, it

calculates the UP/DOWN commands to send to the AVRs of each generating unit of the power plant;

- A Simulator block of the physical plant (power station/grid with numerical outputs of the three-phase AC voltages and currents for each generator) for validation purposes. The simulator runs in parallel with the control algorithm in real-time and it can be used to facilitate factory commissioning and further maintenance or upgrade activities. Although the Simulator block could be eliminated from the control code when the commissioning has been concluded the computational load of this code has no influence on the overall computation and therefore the block is maintained inside the device code;
- A Finite State Machine, which realizes all the logical functions to be handled (start/stop sequences, protection functions, warnings and alarms);
- The HMI, realized using the RTAI-Lab extension or other suitable libraries, which graphically presents the state of the system using suitable virtual instruments (meters, scopes, leds, etc.);
- The I/O activities, which include drivers for both digital/analog I/O cabled signals and communications from/to SART Units, DCS, SCADA, and so on. These I/O channels are implemented using digital and analog I/O boards (for cabled signals) or using network boards (for communications): as the hardware platform utilized is a standard PC, it is possible to use the widest range of I/O cards. These I/O channels can be also utilized to log data from the virtual instruments into external terminals or memory devices.

Each of the above listed elements will be now described in more detail.

6.4.2 Regulator block

The Regulator block implements the core of the control algorithm of the SART device. It comprehends:

- a reactive power control loop for each generator;
- the power station HV busbar voltage control loop.

Fig 6.3 shows the scheme of the SART regulator. The regulator reads its input from the HV busbar or from the Simulator. The command outputs are sent as well to the simulator and to the AVRs of the generators in the power plant. In the normal operation mode the switch

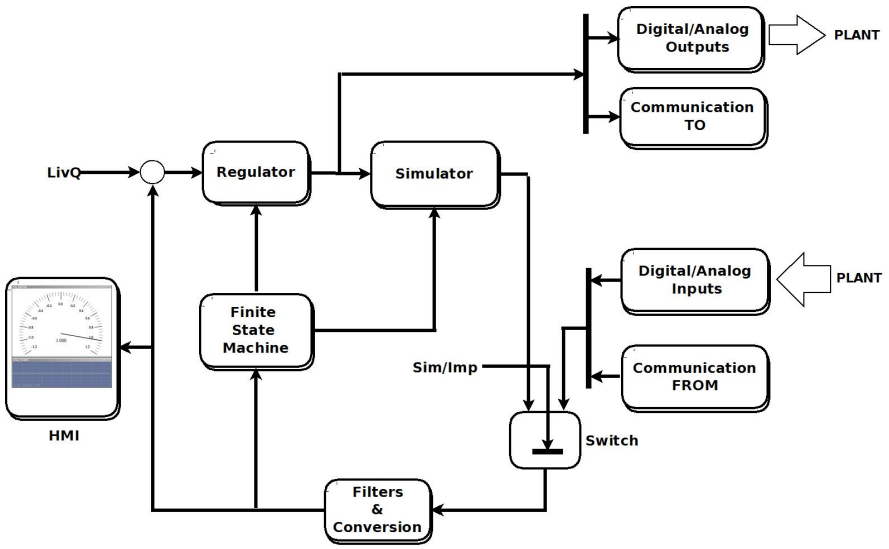


Figure 6.2: SART Central Unit. - Functional scheme of the SART Central Unit.

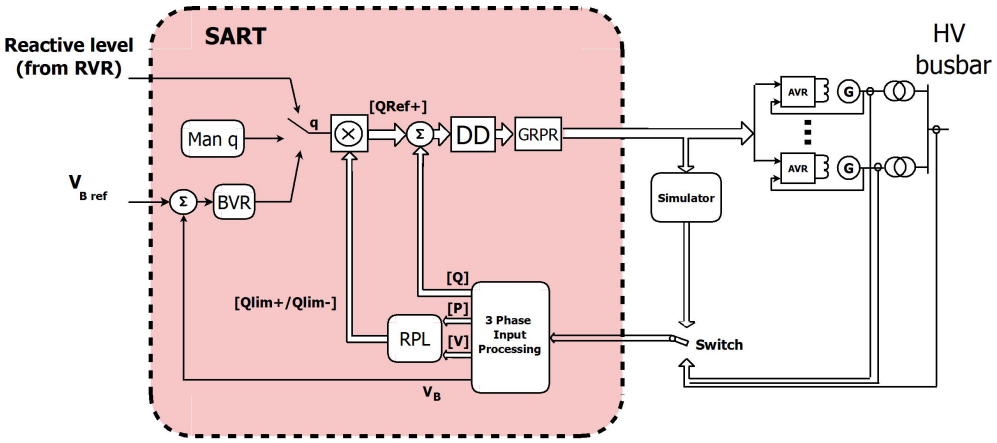


Figure 6.3: Regulator - SART Central Unit Regulator block scheme.

excludes the simulator signals. There are three different inputs of the regulator according to the functional behavior chosen: the regulator receives a voltage control reference when operating as voltage busbar controller, or receives a reactive level signal when operating as reactive controller under the SVR. The third possible input is when the reactive power level of the power plant is manually input: normally this is done only during commissioning activities, it is given to the regulator directly by the operator through the HMI.

The reactive level Liv q received from the RVR is a scalar value comprised between the values -1 and $+1$. The value $+1$ represents a request to the power plant to produce the maximum value of reactive power according to the actual operating point. Similarly, a value of -1 means the maximum reactive power absorption request according to the operating point of all the generators in the power plant. From the Reactive Power Level (RPL) block comes out a value in p.u. for each generator indicating the limit of the generator according to the actual limit curve. Therefore the Liv q value is multiplied for the limit (in p.u.) of each generator.

At a given time each generator delivers a certain P and a certain Q. As shown in Fig 6.4, the working point (represented by a point in a horizontal line with a certain value $\bar{P}$ of active power) sets a limit in the reactive power absorbed or exported by the generator. The maximum reactive power that can be delivered is called Q Lim + and the maximum reactive power that can be absorbed is called Q Lim -.

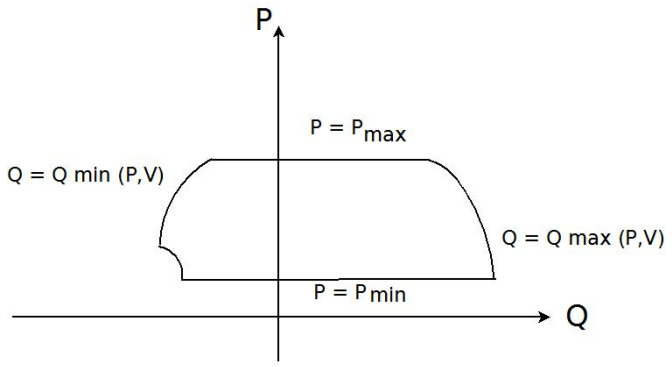


Figure 6.4: Capability curve - Typical capability curve for synchronous generators.

These values are the maximum values the reactive power can reach and they depend on the active power, the voltage and the capability curve. The SART system permits to introduce several capability curves and to chose on the fly which one is active at a certain time. To give an example, for a request of Liv q equal to $+0.7$ the requested reactive power in p.u. for each generator is each *Lim Q +* multiplied by 0.7. This means that each generator has to

deliver a reactive power equal to 70% of its possibility for the active power delivered. This way the reference values of reactive power for each generator are calculated. The actual reactive power generated less this reference gives the error value qerr for the reactive power of each generator. Prior to apply this value to the chosen regulator (traditionally a PI is used), the value is elaborated through the Dynamic decoupling Matrix (DD) with the following equation:

$$[q_{ctrl}] = [DD]\,[q_{err}] \tag{6.1}$$

The DD matrix is the inverse of the non-diagonal matrix which couples the vector of the generator terminal voltages to the vector of the generator reactive powers [107].

From Fig. 6.5 the following relations descend :

$$\Delta Q_i = \frac{\Delta V_i - \Delta V_B}{x_{ti}} \tag{6.2}$$

$$\Delta V_B = \sum_{i=1}^{n} \Delta Q_i x_e \tag{6.3}$$

$$\Delta V_i = \Delta Q_i x_{ti} + \sum_{i=1}^{n} \Delta Q_i x_e \tag{6.4}$$

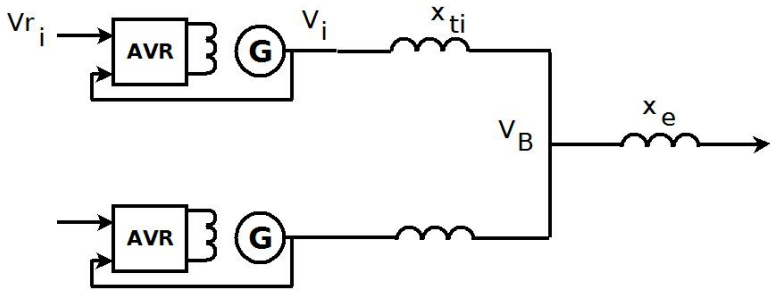


Figure 6.5: Dynamic decoupling matrix - Relation between reactive power variations and voltage variations.

The relation between generator voltage variations and reactive power variations can be expressed with the following matrix expression:

$$\begin{bmatrix} \Delta V_1 \\ ... \\ \Delta V_n \end{bmatrix} = \begin{bmatrix} x_{t1} + x_e & x_e & x_e \\ x_e & x_{ti} + x_e & x_e \\ x_e & x_e & x_{tn} + x_e \end{bmatrix} \begin{bmatrix} \Delta Q_1 \\ ... \\ \Delta Q_n \end{bmatrix} \tag{6.5}$$

SART actuates the reactive level requested modifying the voltage reference of each AVR. Therefore the imposed variations of reactive power for each generator (i.e. the vector $[q_{err1}, ..., q_{errn}]$)

are composed with the decoupling matrix $[DD]$ whose elements are:

$$(d_{i,j}) = \begin{cases} x_{ti} & \text{if } i \neq j \\ x_{ti} + x_e & \text{if } i = j \end{cases} \tag{6.6}$$

The qCtrl values are finally used to generate AVRs voltage references by means of UP/DOWN commands. The SART device is designed to work with two different modulation for the UP/DOWN commands: pulse-frequency modulation (PFM) and pulse-width modulation (PWM) With PWM, when qCtrl is positive an UP pulse is generated and remains UP till the value qCtrl remains positive. With PFM, a pulse of a specified length is generated.

An example of logical circuit generating the UP pulses in PWM is shown in Fig 6.7

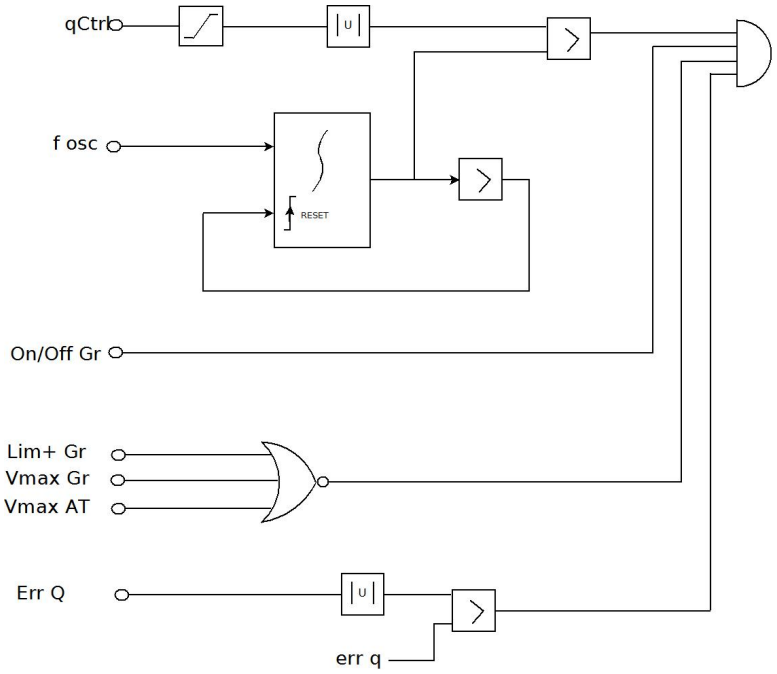


Figure 6.6: - Generation of UP PWM pulses.

A ramp signal at the frequency of the pulses to be generated with amplitude between 0 and 1 is compared with the absolute of the qCtrl signal and it generates the PWM pulse. The UP pulses are enabled only if all the following conditions are true:

- the generator is under control of SART: signal On/Off Gr is true;
- the generator has not reached its upper reactive limit: signal Lim+ Gr is false;
- the generator has not reached its upper voltage limit: signal Vmax Gr is false;

- the AT busbar of the power plant has not reached its upper voltage limit: signal Vmax AT is false;

- the difference between the reactive power injected by the generator and the reference reactive power is lower than a set insensitivity value: Err Q is lower than err q.

A similar scheme can be drawn for the DOWN pulses considering symmetrical signals for lower limits in reactive power and voltage. The pulse would be an UP if qctrl is positive or a DOWN pulse if qctrl is negative.

Fig. 6.7 show a possible implementation in an high level language (i.e. Simulink).

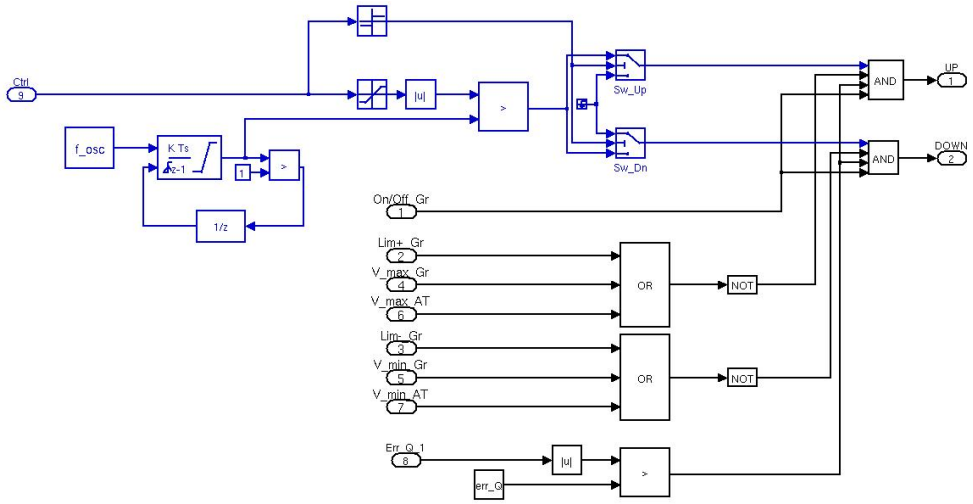


Figure 6.7: - Generation of UP PWM pulses.

The reactive power control is based on the matrix (diagonal) of the Generator Reactive Power Regulators (GRPRs) .

6.4.2.1 Busbar voltage control mode

As shown in Fig. 6.3 the SART can be utilized also for power station stand-alone control (i.e. out of SVR). This can be done either by locally setting the reactive level signal (manually in Man_q mode, as in Fig 6.3), or by overlapping the reactive power control loop with the power station HV busbar voltage control loop, through the Busbar Voltage Regulator (BVR) . Under BVR, daily memorized profiles of HV busbar voltage can be stored and actuated.

6.4.3 Simulator block

The simulator block is a mathematical model of the power plant and the network. It takes as input the UP/DOWN commands calculated for every generator, it has the active power of each generator, the total reactance between each generator and the network, the voltage of the network as defined parameters. Each generator is considered as regulated by an AVR with defined constant time of the value 0.5 s. Thus the power plant and network model, for N generators, is the scheme in Fig 6.8.

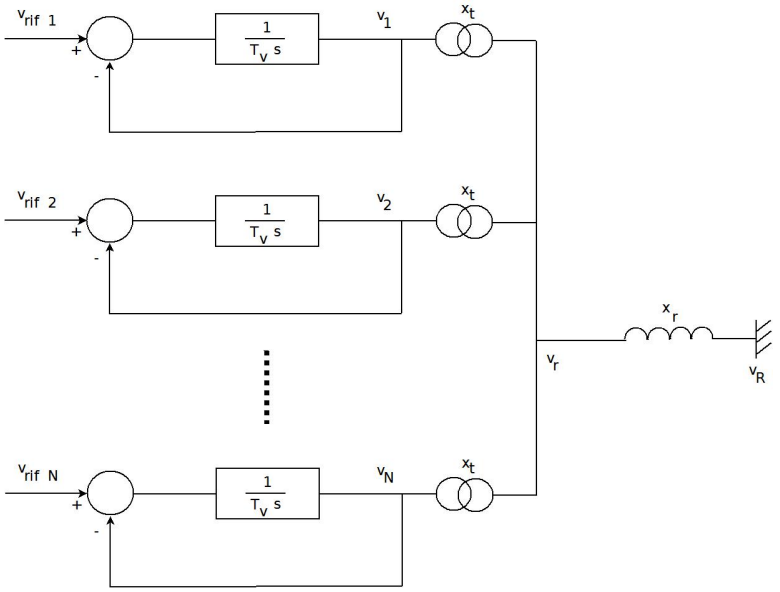


Figure 6.8: Network model - Power plant and network model.

The reactive power absorbed or delivered by each generator will be:

$$q_i = \frac{v_i(v_i - v_r)}{x_t} \tag{6.7}$$

where v_r is:

$$v_r = \frac{\frac{v_1}{x_t} + \frac{v_2}{x_t} + ... + \frac{v_R}{x_t}}{\frac{1}{x_1} + \frac{1}{x_2} + \frac{1}{x_N}} \tag{6.8}$$

Although it should be possible to deeply model every generator with its AVR, the proposed first order model for AVR and generator is sufficient to simulate the behavior of SART. Decoupling between the inner voltage loop of each generator and the reactive outer loop is based on the difference on the time constant of the two loops. Therefore the inner voltage loop is fixed at 0.5 seconds when the outer reactive power loop is set at 5 seconds.

6.4.4 Finite state machine block

The Finite state machine block is part of the SART device and is implemented together (inside the same processor unit) with the regulation, simulation and I/O signal processing functions. A different implementation choice could have been to implement the SART logic into a dedicated CPU as for example a programmable logic control (PLC) device.

A SART device can be in one of the following three functional modes:

1. SART controlling the reactive power level set by the remote Liv q signal;
2. SART controlling the reactive power level by a local manually generated Liv q signal;
3. SART controlling the busbar voltage level by a local voltage reference signal.

The logical functions implemented are:

- The switching between different operational modes: from manual reactive control, to remote reactive control and to voltage busbar control;
- The insertion and exclusion of single generator groups in SART control loops;
- The alarm management. A list of the alarms managed by the finite state machine is:
  - Fault in the remote reactive signal received;
  - Fault in generator busbar voltage measures;
  - Faults in peripheral units;
  - Faults in SCADA or DCS communications;
  - Communication faults with peripheral units.

All the logical functions have been modelled with combinational logic and sequential logic. They have been respectively implemented by boolean circuits and by flip-flops.

6.4.5 Human Machine Interface

Several levels of HMI have been designed for SART device. The first level runs directly on the CPU where all the control tasks run. The xrtailab application [57] [58] has been used and shows the following plant variables:

- Reactive power of each generator unit displayed together on an oscilloscope;

- Voltage of each generator unit displayed each on a separate meter;
- Active power of each generator unit displayed each on a separate meter;
- Q_Lim of each generator unit displayed each on a separate meter.

A panel comprising all alarms is also displayed and a second panel with the state of SART is shown.

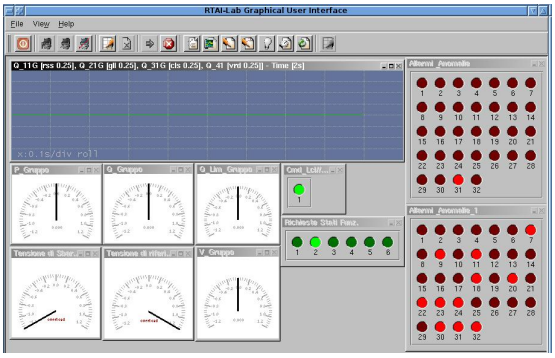


Figure 6.9: HMI - On board interface with xrtailab application.

The interface built with xrtailab (Fig. 6.9) is directly connected with the control task running in real-time. The communication between the control task and xrtailab is implemented through the mailbox communication feature implemented in RTAI.

A second level of interface is often implemented with a commercial SCADA system. The chosen commercial tool is normally decided by the customer and integrates the SART system in the whole power plant SCADA system.

6.4.6 Input - output block

The I/O activities include three main different kinds of communications:

- Cabled I/O analog and digital signals;
- SCADA and DCS communications;
- Internal communications of the SART system.

6.4.6.1 Cabled I/O

Analog and digital signals are implemented using digital and analog boards connected to the PCI bus.

Digital input/output is performed by an adequate number of PCI digital I/O boards (PCIe-DIO96H from Measurement Computing) mounted on a SART system. Each board can be used for a total of 96 digital values each one programmable as input or output. From RTAI such boards work under the 8255 comedi driver.

Analogue input is performed by PCI-Das1002 which provides either 16 single-ended or eight differential analog inputs. DAS1002 is driven by cb_pcidas comedi driver.

Analogue output is carried out by NI-6704 board from National Instruments, which provides 16 analog outputs. The comedi driver used for this board is the ni_670x.

The comedi drivers assure that each operation is performed without loosing real-time. The control task performs several input output operations. As an example, a SART system controlling three generator units of a combined gas power plant needs approximately 50 logical inputs and 50 logical outputs, 20 analog outputs and 20 analog inputs. All these variables must be read an written in each control loop avoiding the use of buffers. Comedi drivers implement I/O operation respecting real-time.

6.4.6.2 Internal communications

Redundancy The SART-CU can be duplicated into a redundant dual-unit to provide the apparatus with a high degree of availability. Two PCs are employed in this case and they run as Master and Slave and share via communications all the numerical and logic state variables. An independent arbiter device commutates Slave PC to Master in case of a fault. Each unit communicates its state to the other unit every 10 ms. The values that are exchanged between the two units are:

- On/Off status for each generating unit: every generating unit, although present and working, can be excluded from the SART control;
- General On and Off status;
- Functional status of SART: one of the three operational modes (busbar voltage control, reactive level control, manual reactive level control);
- References of the voltage and reactive power calibrators;

- Islanded condition.

Peripheral units SART control systems receive measures from the power plant through several peripheral units:

- from the generating unit it receives measures of active power, reactive power, busbar voltage;
- from each AVR it receive a signal indicating the availability of the AVR, active capability curve;
- from the high voltage busbar unit it receives the voltage measure.

SART also sends some control signals to peripheral: the most important are the Up and Down signal to the AVRs.

All these ways to communicate with the peripheral units are performed every 10 milliseconds as shown in chapter 4

6.4.6.3 SCADA and DCS communications

A SART control system is normally inserted in the SCADA system of the entire power station. The protocol used depends on the requests of the power plant manager. One of the most common choice is the use of one of the OPC series of standard. In this case a bridge is implemented on a Windows machine.

Fig 6.10 depicts the general structure of all the communications of a SART system. Every SART-CU has three network cards:

- One connecting the CU to the internal network composed by the peripheral units;
- One connecting the two CU one with each other: the simpler connection can be implemented with a cross Ethernet cable;
- One connecting the CU to the external network (the power plant SCADA network).

The SART rack contains two Ethernet switches: one for the internal network and one for the connection with the power plant network. The internal and external networks are therefore physically separated. The IP packets forwarding is always disabled. The communication with the external network is implemented with a software bridge that manages also the logic of the

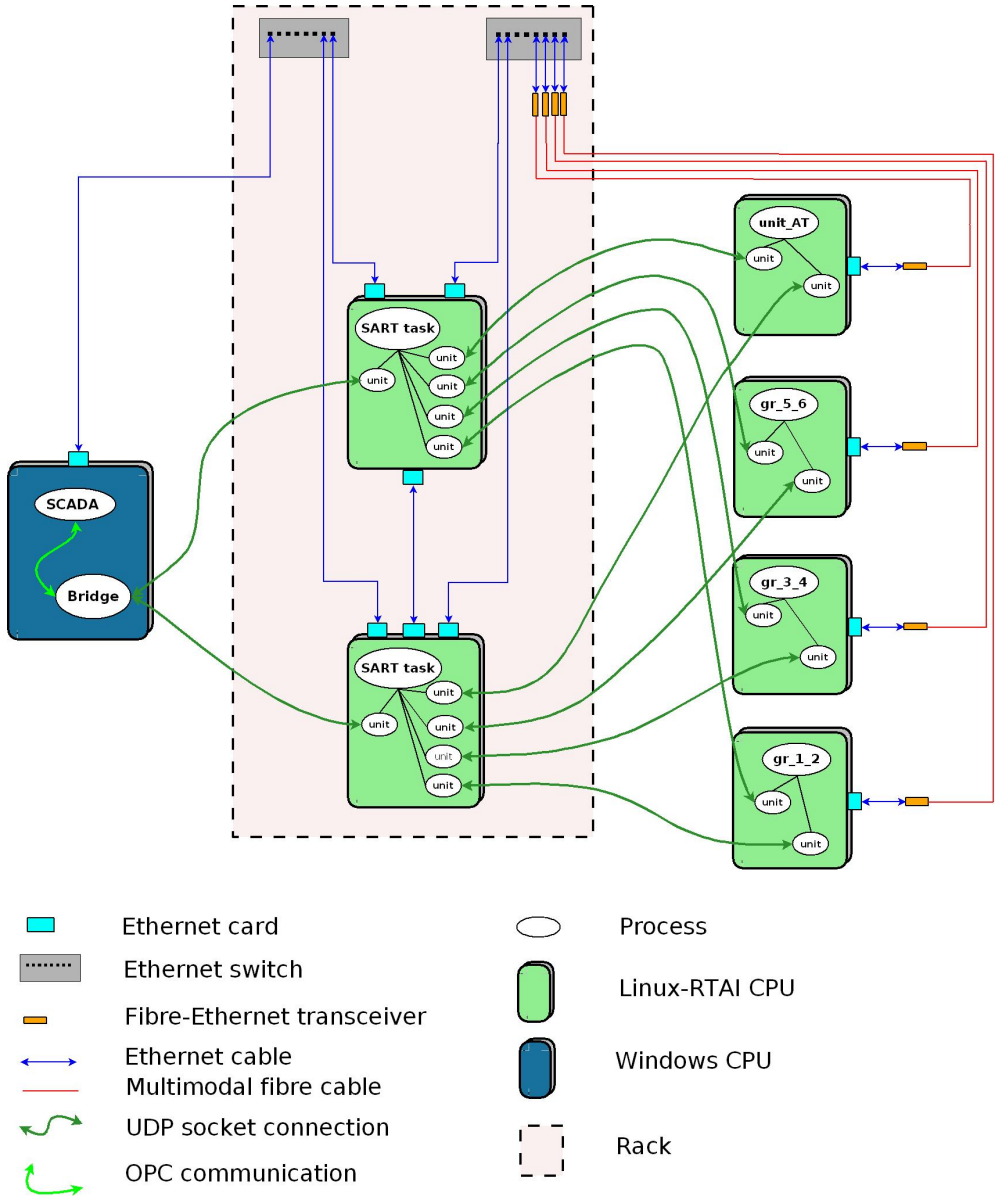


Figure 6.10: Communications - General communication diagram of SART

redundancy in the communication with the two SART-CUs, presenting a unique device to the SCADA system.

From the internal switch to the peripheral units the communication is on optical fibre: the peripheral units are normally located several hundred meters from the central unit. Therefore all communications are implemented at the physical layer level of the standard networking model with the IEEE 802.3 family. A physical switched channel is dedicated to every logical communication channel to avoid Ethernet collisions.

Above the physical layer, for the transport layer IP protocols have been used: UDP for internal communications and TCP to connect to the external network. A process denoted unit in Fig. 6.10 is the interface between the real-time control task and the non real-time communication tasks and it is described in chapter 4.

Therefore, SCADA and DCS along with internal communications are all performed with network cards through software IP protocols. They are treated deeply in chapter 4.

6.5 Experimental data

Experimental data of four different power stations will be presented.

The SART system has been applied to different power stations connected to the italian transmission system at 400 kV.

Data were registered during commissioning operations with Italian TSO TERNA. The data are sent from the SART apparatus through the Ethernet with a simple protocol using UDP/IP as described in chapter 4. An external laptop is connected to the SART local area network and collect all the data into files that can be elaborated on line or used for further elaborations. Data are collected at a frequency of 100 Hz (i.e. the sampling time is 10 ms).

6.5.1 Case 1

The first case is a gas combined power station. The power station is composed of two 323 MVA gas turbine generators and one 360 MVA steam turbine generator.

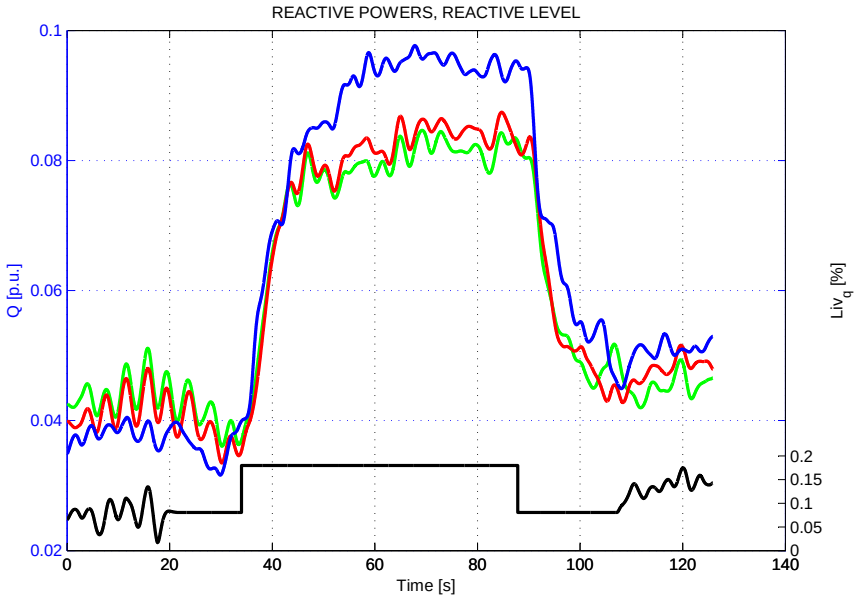


Figure 6.11: Case 1 - Step 1 - Reactive power response to a step in Liv_q signal.

In Fig. 1 it is shown the reactive power response of the three groups: in blue the 360 MVA steam generator, in red and green the two 323 MVA gas turbine generators. At time 20 sec

the power station move from RTS (where the voltage of the high voltage busbar is controlled) to a Liv_q mode (where the reactive powers follow the signal received from the TSO). At time 34 sec (circa) the signal Liv_q is commanded with a step of +10%. Every group changes its reactive power generated according to its capability curve and its active power generated (not shown). The three generators are commanded with a series of digital pulses modulated in duration (PWM).

In Fig. 6.12 and Fig. 6.13 the voltage profiles of group 1 and 3 with the UP and DOWN commands sent from the SART to the excitation system are shown. The pulses are width modulated.

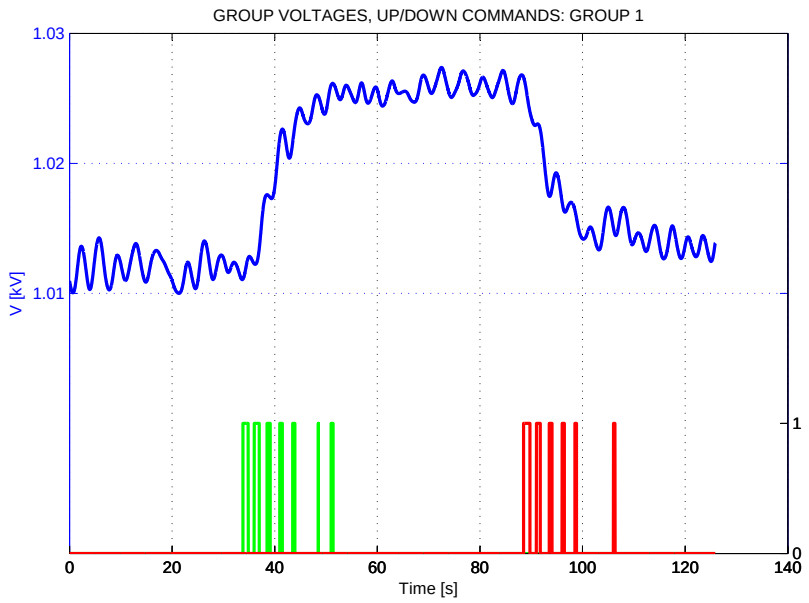


Figure 6.12: Case 1 - Voltage GR1 - Voltage of group 1 with the up and down command sent.

In Fig. 6.14 a step of 20% (from + 0.05 to +0.25) is shown. It is easy to see the different level of the reactive power reached by Group 3 (the blue line): this depends on the different size of group three (363 MVA) in respect of the two twin gas generators. The SART system reactive requests are proportional to the reactive power capability of each generator.

In Fig. 6.15 are reported two steps of 25% of reactive level signal. Last graph of Fig 6.15 shows the voltage of the busbar (Vr drawn in black) together with the Vrif signal (Vrif drawn

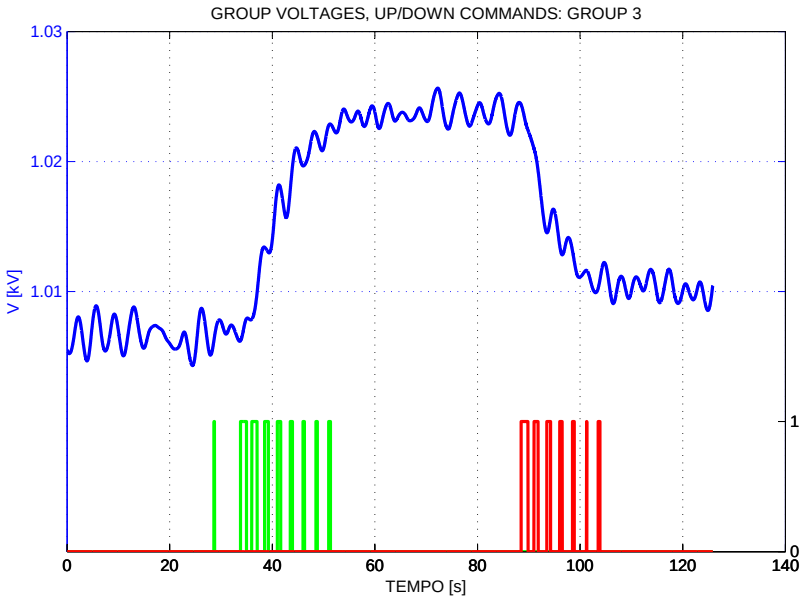


Figure 6.13: Case 1 - Voltage GR3 - Voltage of group 3 with the up and down command sent.

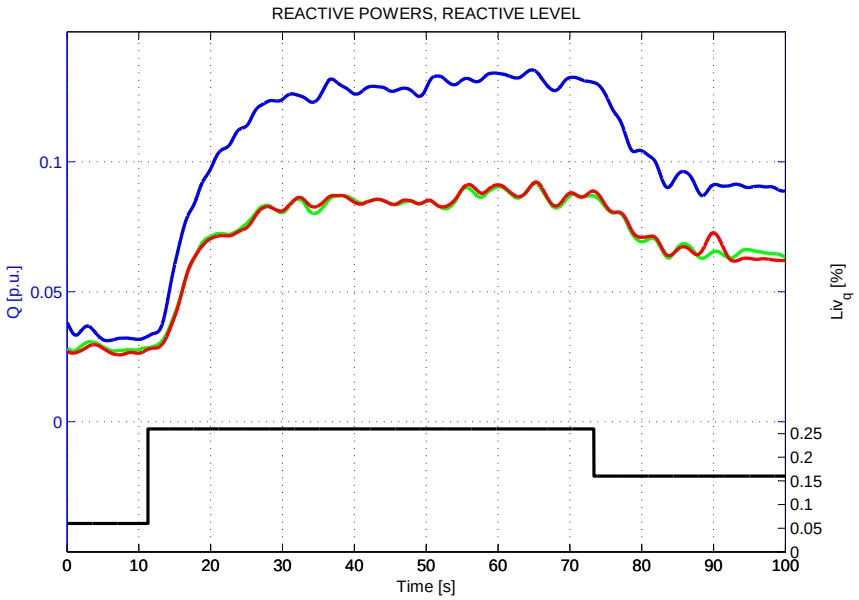


Figure 6.14: Case 1 - Step 2 - Reactive level step of +20%

in blue): being the SART in the Liv_q mode, the Vrif signal simply follow the actual Vr level in such a way to prepare for a dumpless switch to RTS mode.

Fig 6.16 shows three steps of Liv_q from 0 level to 30%.

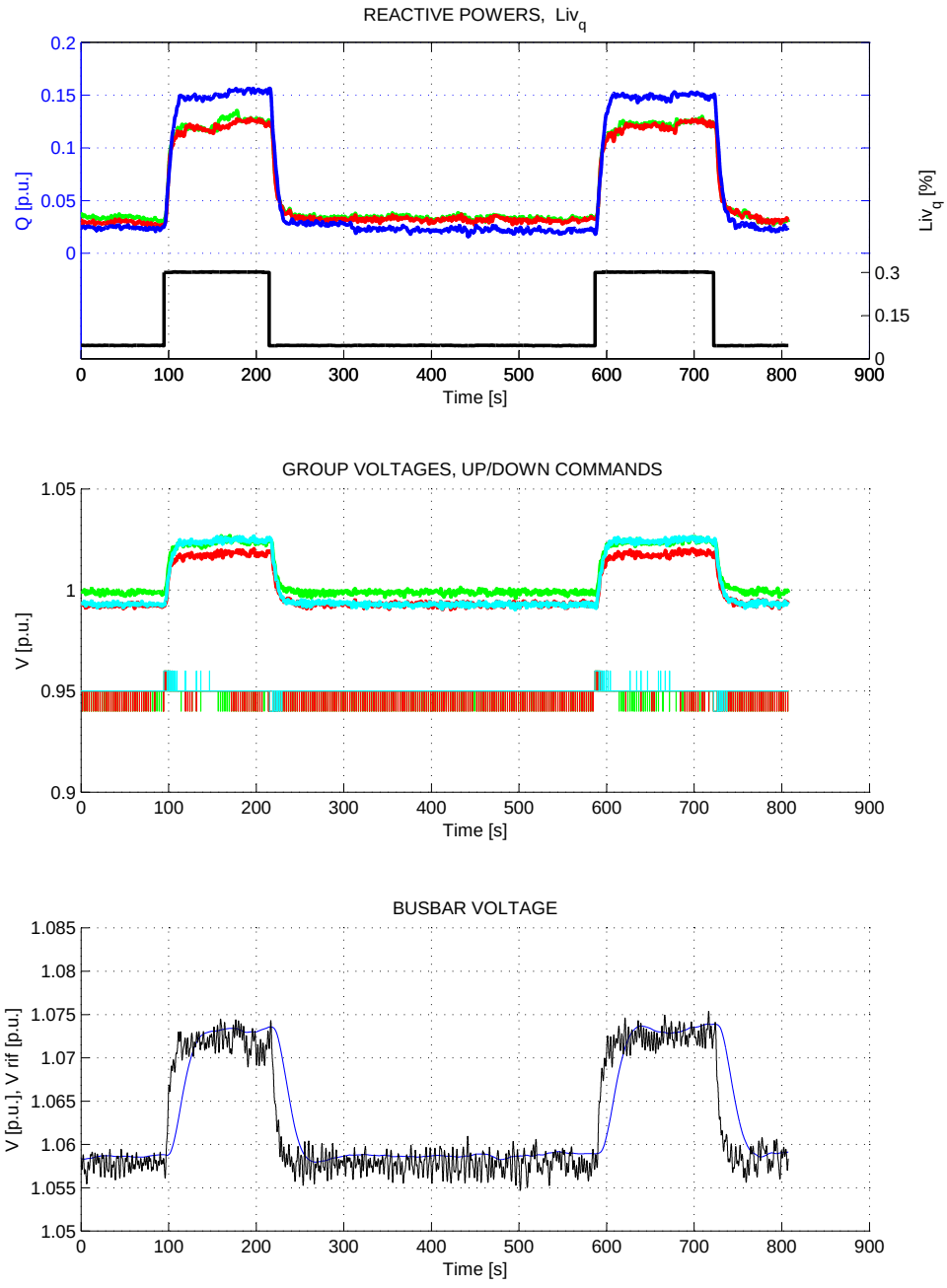


Figure 6.15: Case 1 - Two Steps - Two steps in Liv_q of 25%.

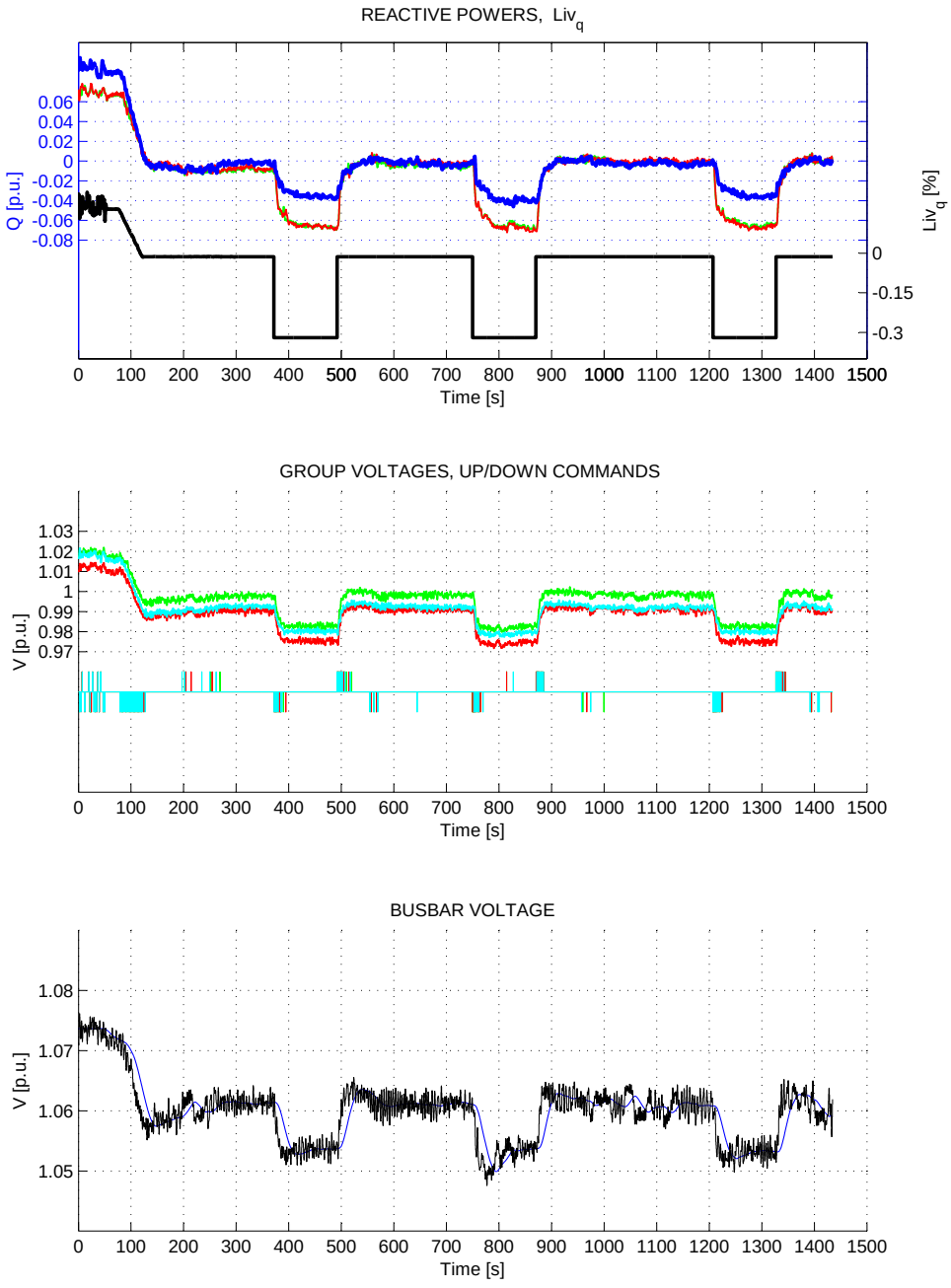


Figure 6.16: Case 1 - Three Steps - Three steps of Liv_q from 0 to 30%

6.5.2 Case 2

The second case consists of the experimental results of the application of the SART in a 1410 MVA power station (3 identical 300 MVA gas turbine and 3 identical 170 MVA steam turbine generators) connected to the 400 kV italian transmission grid. The testing session has been carried out with the power plant fully operating (6 generators on duty) under SART control and receiving the reactive level from the RVR.

In Fig. 6.17 a step of Liv_q of an amplitude of 20% is shown

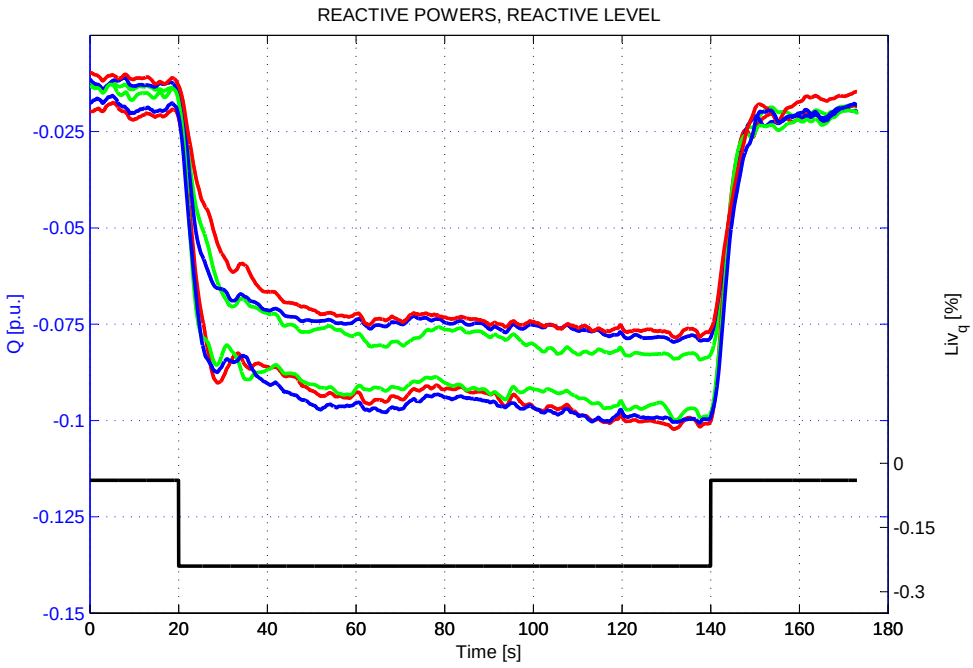


Figure 6.17: Case2 - Step -20 - Six groups power station: reactive power response for a 20% Liv_q step.

In Fig. 6.17 the two different groups of generators (three 300 MVA gas turbines and three 170 steam turbines generators) can be identified.

For the same Liv_q step shown above, the voltage of one steam generator and the pulses sent to its excitation system are shown in Fig. 6.18. In Fig. 6.19 voltage of one gas generator with pulses sent to its excitation system are shown.

In Fig. 6.20 a switch of the SART from Liv_q mode (where the reactive power of the power

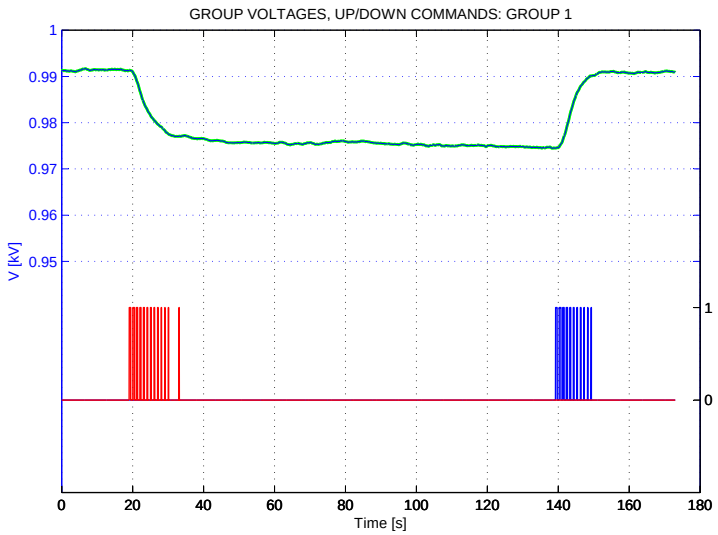


Figure 6.18: Case2 - Step -0.2 Group 1 - Voltage profile and Up/Down commands for group 1. In red color Down commands, in blue Up Commands

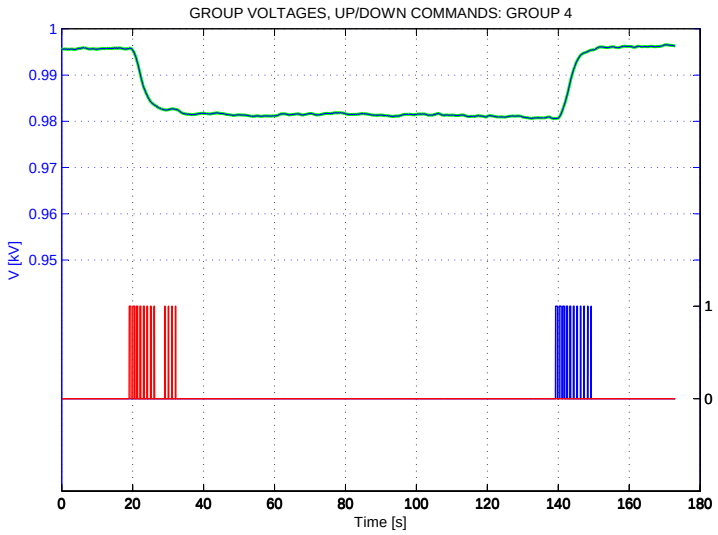


Figure 6.19: Case2 - Step -0.2 Group 4 - Voltage profile and Up/Down commands for groups 4. In red color Down commands, in blue Up commands

station is conditioned with the Liv_q signal) to an RTS mode (where the busbuar voltage is controlled from the power station itself) is shown. At time zero the power station is controlled with a Liv_q signal with a negative ramp. At time 90 the Liv_q is setted constant at level 0.15: in the voltage picture is possible to recognise the V_rif signal following the Vr value. At time 754 sec the SART is switched in RTS mode: the Vr value is controlled with the Vrif signal and the Liv_q follows the reactive power generated by the power station preparing for a possible bumpless switch.

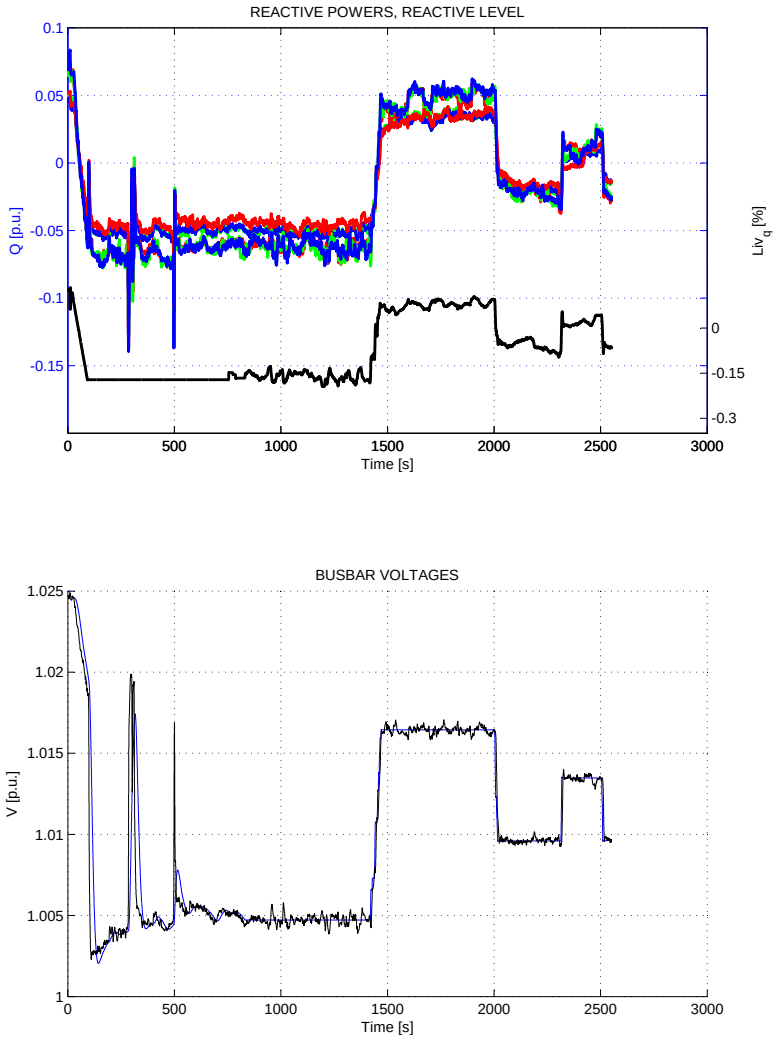


Figure 6.20: Case2 - Livq RTS transition - Bumpless switch from Liv_q mode to RTS mode.

6.5.3 Case 3

The power station under examination is a coal thermoelectric plant composed of three steam groups each of them with the nominal power of 750 MVA.

In Fig. 6.21 the reactive power response for a step in Liv q signal of 30%.

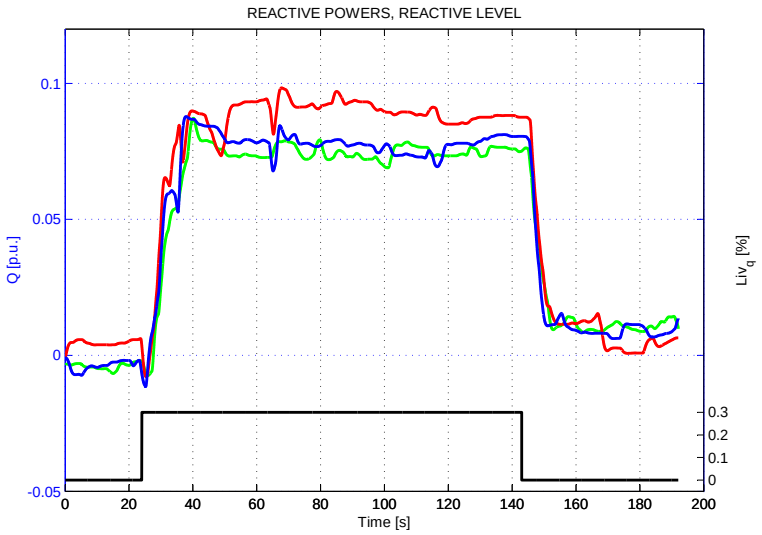


Figure 6.21: Case3 - Reactive power response - Reactive power response to a step of 30% in Liv_q.

In Fig. 6.22, 6.23 and 6.24 the voltages of the three generators along with Up/Down commands for each one are shown.

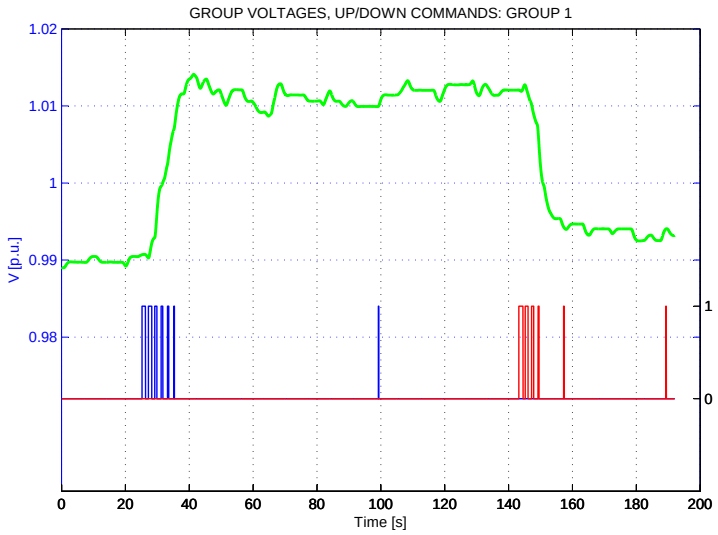


Figure 6.22: Case3 - Voltage GR1 - Voltage and Up Down commands for GR1.

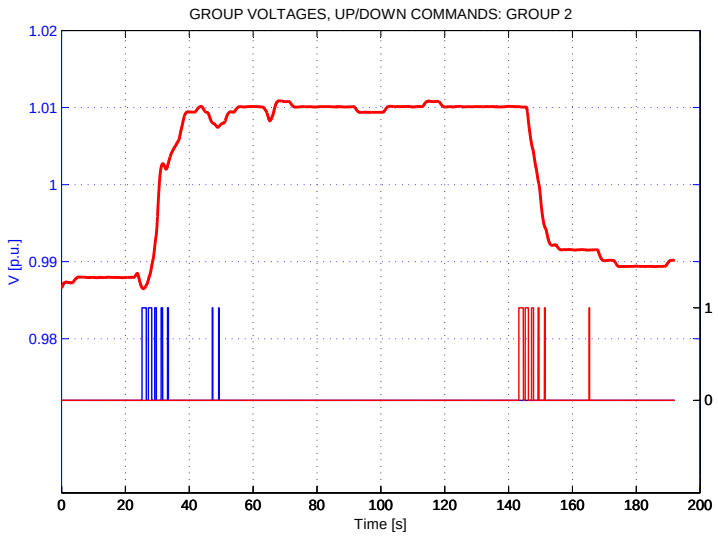


Figure 6.23: Case3 - Voltage GR2 - Voltage and Up Down commands for GR2.

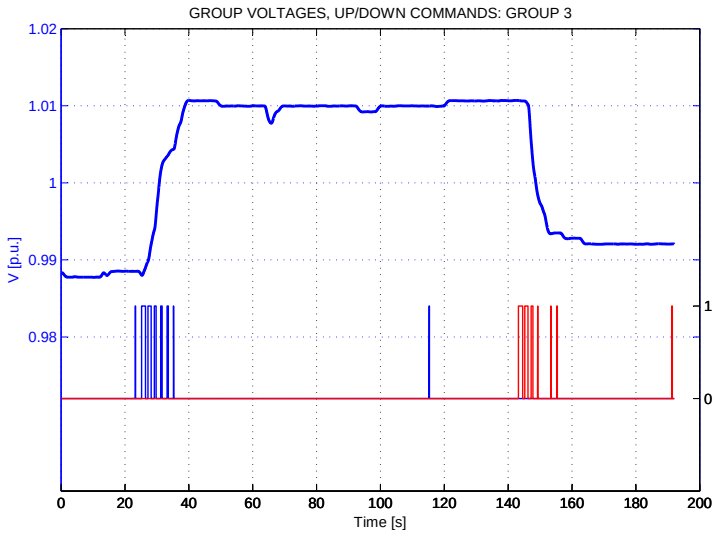


Figure 6.24: Case3 - Voltage GR3 - Voltage and Up Down commands for GR3.

6.5.4 Case 4

The plant is a combined-cycle power station composed of two identical groups. Each of the two groups is composed of a gas turbine connected with a synchronous generator of 300 MVA and steam turbine connected to a synchronous generator of 170 MVA. The power station is connected to the Italian 400 kV transmission grid.

Fig 6.25 shows a step in Liv q from value 0.35 to value 0.05.

In Fig. 6.26 are shown Down pulses and voltage for Gr1 gas turbine generator for the falling edge of Liv q shown in Fig above 6.25.

Up pulses for generator Gr2 (stem turbine generator) are shown In Fig. 6.27

Finally in Fig 6.28 the busbar voltage is shown.

6.6 Conclusions

A new SART architecture has been implemented. It is based on an open source real-time OS (i.e. Linux RTAI) and on Switched Ethernet. Detailed description of the implementation adopted has been reported. Experimental tests carried out at different power plant stations have confirmed the effectiveness of the solution proposed.

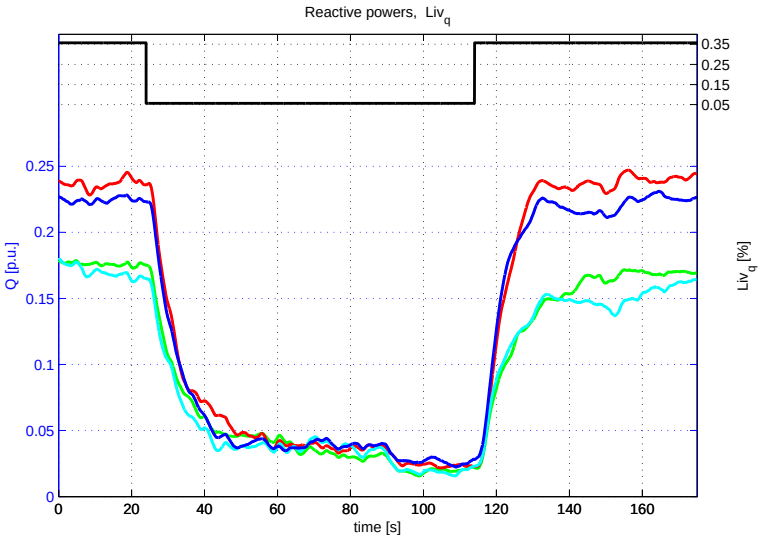


Figure 6.25: Case4 - Reactive power response - Reactive power response to a step of minus 0.3 in Liv_q. Lines Red and Blue refer to the steam turbine generators while lines Green and Cyan refer to the gas turbine generators.

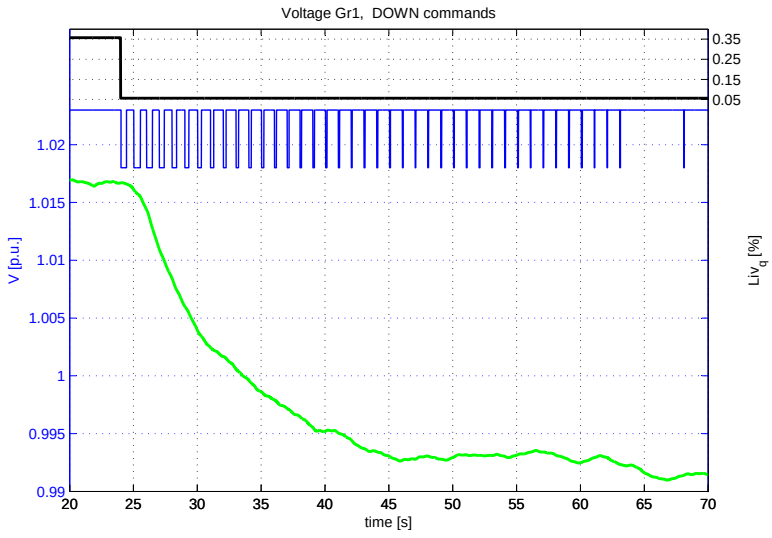


Figure 6.26: Case4 - Voltage GR1 - Generator Gr1 voltage and DOWN pulses

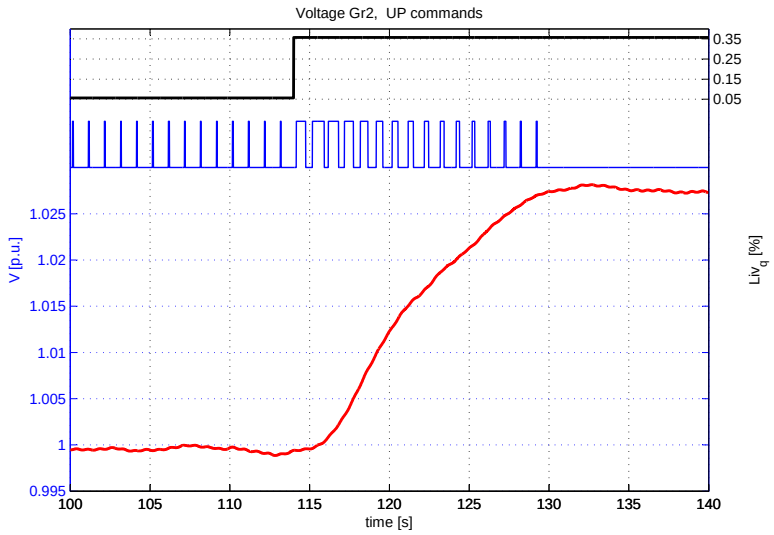


Figure 6.27: Case4 - Voltage GR2 - Generator Gr2 voltage and UP pulses

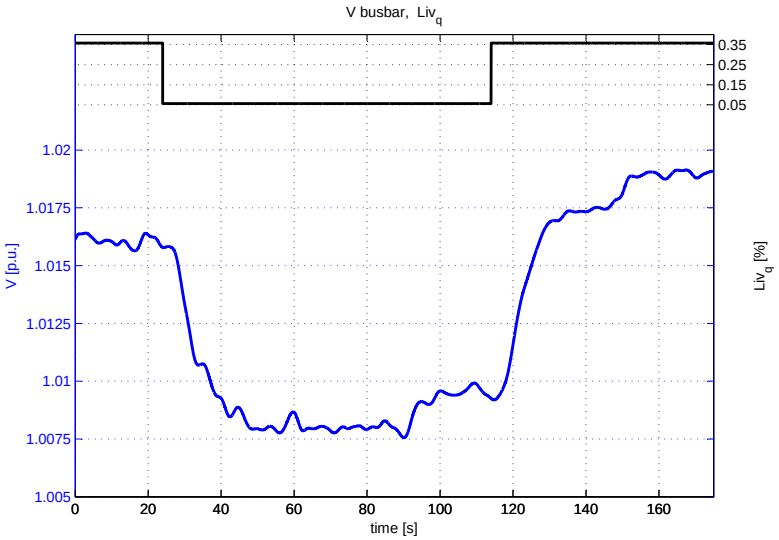


Figure 6.28: Case4 - Busbar voltage - Power station busbar voltage during the Liv_q step

7

Distributed Generation

7.1 Introduction

As distributed generation increases, new control problems arise. Among them the voltage rise problem is presented along with a new control strategy. Simulations on test networks are presented. It is believed that the hardware and software platform detailed in the previous chapters can be a powerful instrument to implement the voltage rise mitigation technique presented.

7.2 Distributed energy resources

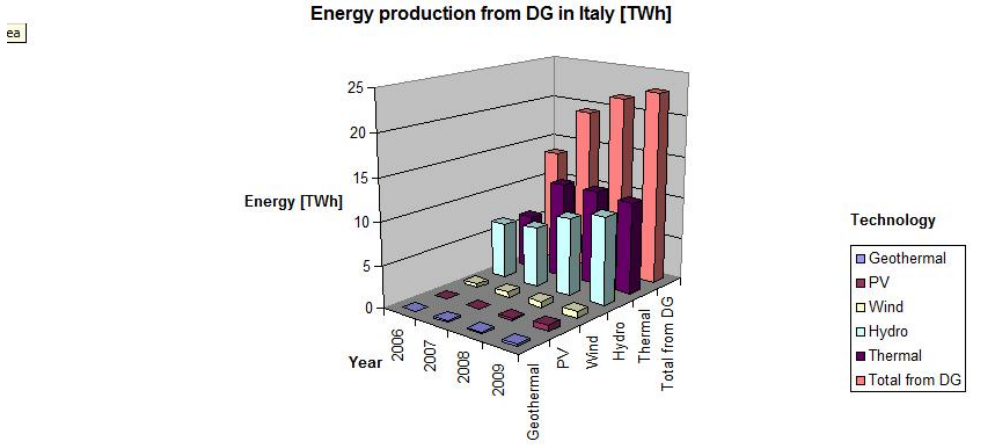
According to several authors the term of DG is used to depict the production of electrical energy with generators of the size from some kW to several MW. Depending on the connection rules adopted by any national Grid Code, the upper limit for considering a generator as belonging to the DG can be from some kVA to 100 MVA. In Italy the AEEG directive n. 160/2006 [108] defines as DG, generators of a nominal power lower than 10 MVA connected to the distribution network [1]. Although some definitions of DG do not include the rating of generators [109], normally the size of a generator determines where it can be connected to the grid and this depends on the capacity and voltage level of each network. Therefore the size of a generator normally determines if a generator belongs to the distribution grid or not and can be consistently different in different countries [110][111]. As well, there are exceptions where bigger generators have been connected to the distribution grid for technical reasons.

[1] TICA document (Integrated Text for Active Connections) published by AEEG in 2010 asserts that producing plants injecting power lower than 6000 kW have to be connected to medium voltage grid.

The technology used for DG is not relevant but some generation technology categories (e.g. renewable technologies and combined production of heat and power) cover the majority of DG installed. A brief list of DG technologies available contains:

- Hydro power systems;
- Wind turbines;
- Photovoltaic systems;
- Fuel cells;
- Microturbines;
- Internal combustion engines;
- Stirling engines.

The situation of energy production growth with DG in Italy in the last years is depicted in Fig. 7.1 [112] [113] [114]



	2006	2007	2008	2009
Geothermal	0	0,2	0,2	0,2
PV	0,0021	0,04	0,2	0,7
Wind	0,45	0,7	0,7	0,8
Hydro	6,6	7,1	9,2	10,4
Thermal	6,4	11,3	11,3	10,9
Total from DG	13,5	19,3	21,6	22,9

Figure 7.1: - Energy production with DG in Italy in TWh.

Several factors have lead to an increase in the DG [115] [116]. Among them the most important are:

- The liberalization of electricity markets (as for example in several European countries where the vertical national electricity companies have been substituted by private companies partecipating in a wide base of competing suppliers market) augments the possibility for investments in the production of electrical energy also with small capitals and therefore small size generators;
- Development in technology offers a wide range of solutions in the generation of electrical energy, especially in the low range power size and is often related to a better utilization of energy sources (i.e. combined generators for residential and commercial utilization) or renewable energy sources;
- The climate change problem and the various protocols and directives issued by governments, boost for the utilization of renewable sources or for a better utilization of fossil fuel based sources. In both cases this leads to an increment of little size generators that are normally connected to the distribution network for economical and practical reasons.

Several technical issues must be considered about connecting small generators into an already existing distribution network (that normally has been designed to work as a passive network). For the distribution networks, many studies [117][118] consider the impact of DG penetration in terms of short circuit currents, conductor thermal limits, voltage variations and fault protections. A brief list of the technical issues arising when introducing dispersed generation in distribution networks can include:

- Thermal rating of equipment;
- System faults levels;
- Stability;
- Reverse power flow;
- Steady state voltage rise;
- Power quality;
- Protection systems.

One of the most impacting phenomenon is the steady-state voltage rise resulting from the connection of distributed generators [119].

7.3 Voltage rise

Actual distribution networks have been designed as passive networks in which voltage decreases along the feeders due to conductors voltage drop. In order to face voltage drops, power is distributed keeping the voltage at the primary substation higher than the voltage at customers connection points. To keep voltage at connection points within permitted limits, On-Line Tap Changers (OLTC) are commonly employed at primary substations [120][121] and eventually cascaded in a number of levels. Voltage drop between two nodes 1 and 2 when power P1 and Q1 are injected as in Fig. 7.2, can be calculated according to equation 7.2.

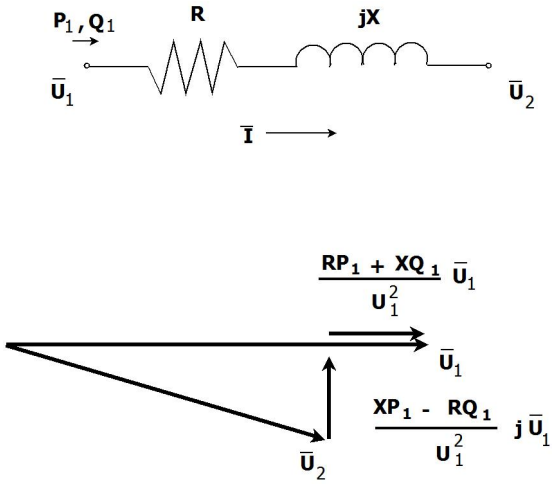


Figure 7.2: Voltage drop - Voltage drop between two nodes.

Therefore it results:

$$\bar{U_1} - \bar{U_2} = \frac{(R + jX)(P_1 - jQ_1)}{U_1^2}\bar{U_1} \tag{7.1}$$

$$U_1 - U_2 \approx \frac{RP_1 + XQ_1}{U_1} \tag{7.2}$$

where:

- U_1, U_2 are the voltages at the ends of the line;
- R and X are the resistance and reactance of the line;
- P_1 and Q_1 are active and reactive power injected at node 1.

Therefore voltages in connecting nodes depend on network configuration, load conditions and both active and reactive power produced by generators.

The voltage drop of a distribution line with DG as shown in Fig. 7.3

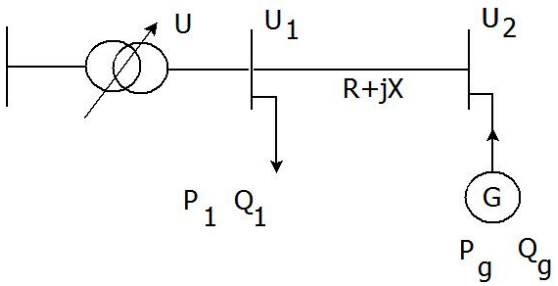


Figure 7.3: Voltage rise - Voltage rise with distributed generation.

can be approximated with the following expression:

$$U_2 - U_1 \approx \frac{RP_g + XQ_g}{U_2} \tag{7.3}$$

This leads to an increased voltage in the feeder due to a generator injecting active power into the network.

Therefore, while in passive distribution networks the voltage profile of a feeder is a descending curve, with the highest voltage near the primary substation and the lower voltages at the end of the feeder (assuming as it normally happens that the distribution network is radial type) with the presence of DG, the voltage profile tends to rise at the generator point of connection. As an example, the voltage profile for an example network that will be further discussed is shown. In Fig. 7.4 the effects of augmenting loads is shown for a passive network. In Fig. 7.5 for the same network the loads have been considered constant while the effects of the increase of active power injection on the voltage profile are shown.

Traditional voltage controls of distribution networks make use of OLTCs. A review of the existing voltage control of OLTCs, which are used to regulate the voltage level, can be found in [122]. The effect of OLTC regulation is to move the curve of voltage profile parallel to itself as shown in 7.6

To mitigate voltage rise and keep voltage within a permissible range, several approaches are possible [119]:

- Reduce the primary substation voltage;
- Allow the distributed generators to exchange reactive power, to reduce the term RP+XQ;

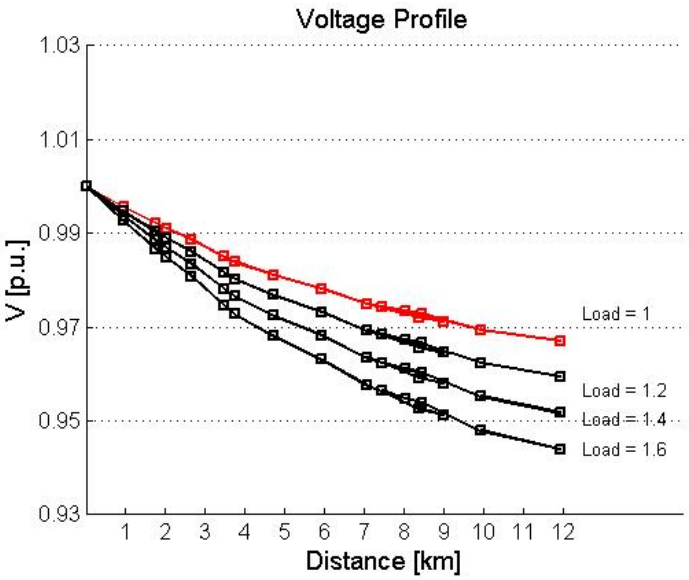


Figure 7.4: Voltage drop - Effects of loads on voltage profile.

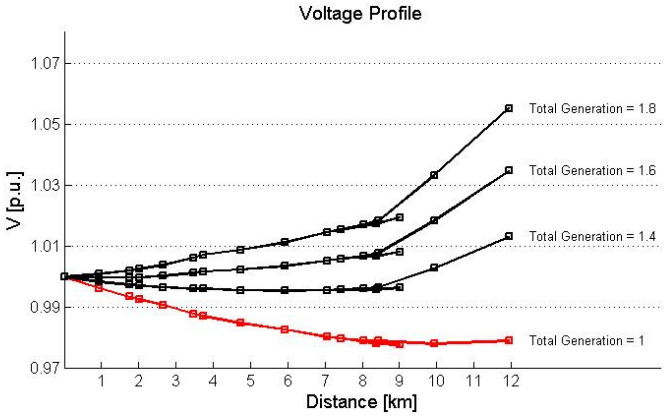


Figure 7.5: Voltage rise - Effects of generators on voltage profile.

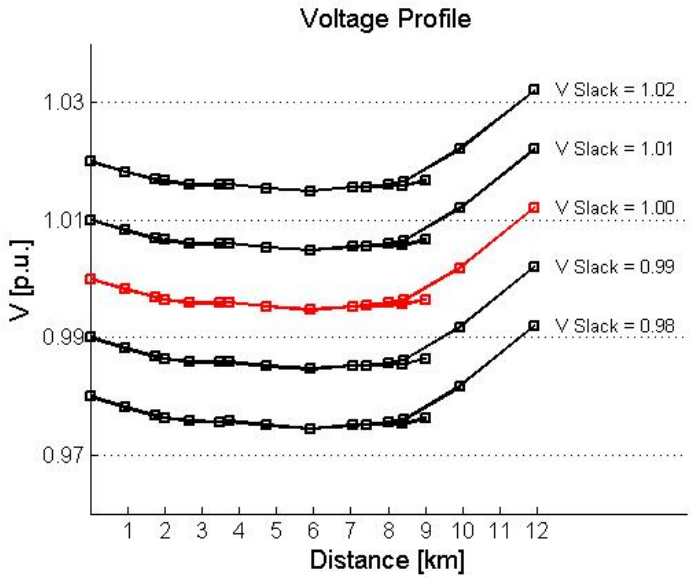


Figure 7.6: Voltage profile with OLTC - Effects of OLTC regulation on voltage profile.

- Employ OLTCs;
- Increase conductor size (reducing the resistance);
- Limiting the active power production of the distributed generators;
- A combination of the above.

The voltage profile in a distribution network can be more effectively controlled if also the reactive power exchanged between the network and the generators is used. In this case generators do not work anymore at unity power factor. In literature, proposed strategies for voltage control acting on reactive power generation can be divided into two categories: coordinated controls and local controls. Coordinated voltage control occurs when a central Power Control Unit (PCU) coordinates the reactive power injected by the generators into a feeder [123] [124]; voltages in the connecting points and power produced by distributed generators are measured as in Fig. 7.7, where an example of four buses network is shown.

In local control each generator controls its reactive power production only on the basis of local measurements, as in Fig. 7.8.

The coordinated strategy implies a communication system throughout the feeder and this communication system needs to be reliable and robust. The central PCU then elaborates all the data needed for calculating an optimized solution. An example of coordinated controls

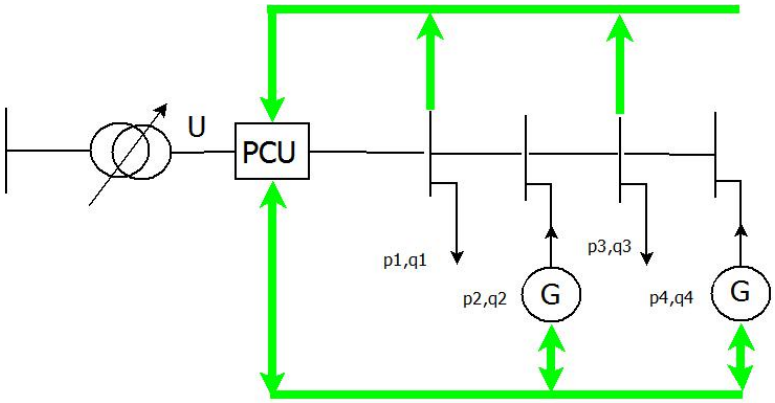


Figure 7.7: Coordinated control - Coordinated reactive power generation control.

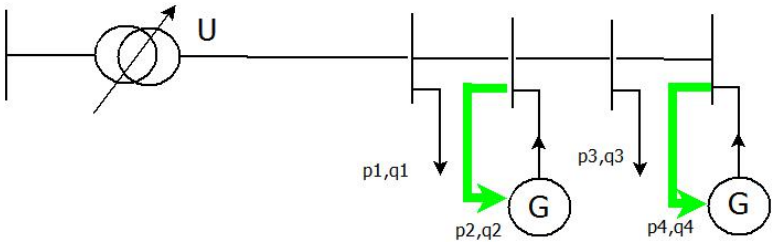


Figure 7.8: Local control - Local reactive power generation control.

based on sensitivity theory has been presented in [125] [126] [127], other algorithms take into consideration also the presence of OLTCs [128] [129] and try to optimize a cost function [130]. Among those that present local controls, one based on sensitivity theory is [131]. Work [132] presents an algorithm that minimizes the reactive power requested from the transmission network. Other solutions can be applied either to a centralized or decentralized architecture as in [133].

7.4 Voltage rise mitigation based on sensitivity matrices

The transient response of generators and their primary controls are assumed instantaneous in relation to the slow time scale of the control and therefore only steady state load flow equations are considered. Loads are modeled as constant power devices. The proposed strategy is a simple reactive control approach based on the two sensitivity matrices defined by the following

expression:

$$[\Delta u_m] = \begin{bmatrix} \frac{\partial u}{\partial p} & 0 \\ 0 & \frac{\partial u}{\partial q} \end{bmatrix} \begin{bmatrix} \Delta p \\ \Delta q \end{bmatrix} = [B][\Delta p] + [C][\Delta q] \tag{7.4}$$

When a subset of network buses of cardinality M (it can be also viewed as M voltage observable nodes) is chosen, the voltage variations at these buses (the vector called $[\Delta u_M]$) can be expressed as linear combination of the active and reactive power injected by the generators into the network.

$$[\Delta u_M] = [B][\Delta p] + [C][\Delta q] \tag{7.5}$$

where:

- $[\Delta u_M]$ is the vector $(M \times 1)$ of the voltage variations at chosen buses with respect to voltage values in absence of distributed generators;
- $[\Delta p]$ is the vector $(N_g \times 1)$ of the active power variations injected by N_g distributed generators;
- $[\Delta p]$ is the vector $(N_g \times 1)$ of the reactive power variations injected by N_g distributed generators.

This equation represents a linearization of the network around the operating point where both reactive and active power generated by dispersed generators are equal to zero. In other words it is a linearization of the network behaviour in absence of distributed generation. Voltage variations due to loads and disturbances on the transmission network are not considered, as the proposed control is only aimed at minimizing variations provoked by distributed generators. The two sensitivity matrices $[B]$ and $[C]$ $(M \times N_g)$ are defined by the equation itself.

The objective of the studied voltage control is to minimize variations $[\Delta u_M]$ controlling the reactive power generated. The control law of reactive power for the N_g is expressed in equation (7.6)

$$[\Delta q] = [A][\Delta p] \tag{7.6}$$

where A is a matrix $(N_g \times N_g)$. This way, the problem becomes to find an [A] matrix, which minimizes voltage variations.

There are several physical variables available to control the variables represented by the vector $[\Delta u_M]$ of voltage variations: voltages, currents, phase angles between voltages, active powers injected, reactive powers injected. Among them the large impact of the power flow injected by the generator on the voltage profile has been shown in [134]. In [135], it is proposed to control voltage injecting reactive power together with the active power according on the voltage of the feeder near the inverter. It is also shown how this control low is equivalent to an injection of reactive power proportional to the active power injected by the generator.

A simplification can be introduced: the number of buses where the voltage variations are minimized is equal to the generators actively involved in the control: $M = N_g$.

With this simplification two different possibilities have been studied: to find a full $[A]$ matrix or to find a diagonal $[A]$ matrix.

A full $[A]$ matrix means that the reactive power produced by one generator depends on the active power of all other active powers produced by the other generators in the feeder. This entails the necessity of a communication channel among all the generators.

With a diagonal $[A]$ matrix every generator decides the reactive power to absorb or inject only on its active power generated. If the coefficients of $[A]$ are fixed, there is no need for communication at all. The coefficients of $[A]$ depend on the topology of the network, the physical characteristics of the cables (resistance and inductance) and the working point (the non-linear system representing the network is linearized around the working point to calculate the sensitivity matrices) and therefore they can be fixed when the network is fixed.

7.4.1 Case full matrix $[A]$

In the equation defining the sensitivity matrices:

$$[\Delta u_m] = [B][\Delta p] + [C][\Delta q] \tag{7.7}$$

where all the matrices are squared matrices $N_g \times N_g$. The analytical solution to eliminate voltage variations ($[\Delta u_M]$) is:

$$[A] = [C]^{-1}[B] \tag{7.8}$$

From a mathematical point of view the solution needs the [C] matrix to be invertible (i.e.

non singular). The C matrix is a squared matrix:

$$\begin{bmatrix} \Delta u_1 \\ \vdots \\ \vdots \\ \Delta u_{N_g} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & \dots & C_{1,N_g} \\ & C_{i,j} & & \\ & & \ddots & \\ & & & C_{N_g,N_g} \end{bmatrix} \begin{bmatrix} \Delta q_1 \\ \vdots \\ \vdots \\ \Delta q_{N_g} \end{bmatrix} \tag{7.9}$$

where the elements can be defined with the following expression:

$$C_{ij} = \Delta u_i | \begin{array}{ll} q_j = 1 & \\ q_k = 0 & \forall k \neq j \end{array} \tag{7.10}$$

Element (i,j) is the variation of the voltage of bus i when the reactive power injected by generator j is 1 and all other generators do not inject any reactive power (the operating point is fixed by the rest of active power that has to be considered constant). The sensitivity coefficients can be estimated by a series of load flow calculations each performed for a small variation of a reactive power control variable. When the load flow calculation is carried out by using Newton-Raphson based methods, the voltage sensitivity coefficients can be derived directly from the Jacobian matrix.

7.4.2 Case diagonal matrix $[A]$

When considering a diagonal matrix $[A]$, the vector of voltage variations becomes function of the N_g elements of $[A]$. The problem can be rewritten as minimum:

$$min \quad u_m = ([B] + [C][A])[\Delta p] \tag{7.11}$$

$$A, B, C \in \mathbb{R}^{N_G x N_G} \tag{7.12}$$

the following functional of the elements of [A] can be considered for minimization:

$$f(\cdot) = [P]^T [B + CA]^T [B + CA][P] \tag{7.13}$$

where

$$A = \begin{bmatrix} a_1 & 0 & ... & 0 \\ 0 & a_2 & ... & 0 \\ ... & & & \\ 0 & ... & 0 & a_n \end{bmatrix} \tag{7.14}$$

The minimum value for the function can be found solving the following:

$$\frac{\partial f}{\partial a_i} = 0 \qquad \forall i \in 1, ..., n_g \tag{7.15}$$

The complete calculation of this minimum now follows.

From equation 7.13:

$$f(A) = P^T(B + CA)^T(B + CA)P \tag{7.16}$$

using the known relations:

$$(AB)^T = B^T A^T \tag{7.17}$$

$$(A + B)^T = A^T + B^T \tag{7.18}$$

$$A^T = A \qquad \text{in case of A diagonal} \tag{7.19}$$

becomes:

$$f(A) = P^T B^T BP + P^T AC^T BP + P^T B^T CAP + P^T AC^T CAP \tag{7.20}$$

which has to be differentiated with respect to the terms $a_1, \ldots, a_n$.

Term $P^T B^T BP$ does not contain any $a_1, \ldots, a_n$ and therefore can be eliminated. Terms $P^T AC^T BP$ and $P^T B^T CAP$ contain only terms of $a_1, \ldots, a_n$ of first grade and therefore will remain as a constant. Term $P^T AC^T CAP$ is a second grade term and therefore will remain, after differentiation, as a first grade in $a_1, \ldots, a_n$. At the end a linear system in $a_1, \ldots, a_n$ is expected.

7.4.2.1 Term $P^T AC^T BP$

It is easy to write term $C^T B$: it is a $N \times N$ matrix whose (i, j) term is

$$(C^T B)_{ij} = \sum_{l=1}^{n} c_{l,i} b_{l,j} \tag{7.21}$$

AC^TB is a $N_g \times N_g$ matrix, the same as B^TC but each row i is multiplied by a_i:

$$[A(C^TB)] = \begin{bmatrix} a_1 \sum_{l=1}^{m} c_{l1}b_{l1} & a_1 \sum_{l=1}^{m} c_{l1}b_{l2} & ... \\ a_2 \sum_{l=1}^{m} c_{l2}b_{l1} & a_2 \sum_{l=1}^{m} c_{l2}b_{l2} & ... \\ ... & & \\ a_n \sum_{l=1}^{m} c_{ln}b_{l1} & a_n \sum_{l=1}^{m} c_{ln}b_{l2} & ... \end{bmatrix} \tag{7.22}$$

The component to $\frac{\partial f()}{\partial a_i}$ of P^TAC^TBP is:

$$\frac{\partial}{\partial a_i} P^TAC^TBP = p_i \sum_{j=1}^{n} p_j \sum_{l=1}^{m} c_{l1}b_{lj} \tag{7.23}$$

7.4.2.2 Term P^TB^TCAP

Similarly to the previous case, the component to $\frac{\partial f()}{\partial a_i}$ of P^TB^TCAP is:

$$\frac{\partial}{\partial a_i} P^TB^TCAP = p_i \sum_{j=1}^{n} p_j \sum_{l=1}^{m} c_{li}b_{lj} \tag{7.24}$$

7.4.3 Term P^TAC^TCAP

Given $C \in R^{m \times n}$, matrix C^TC is in $R^{n \times n}$:

$$(C^TC)_{ij} = \sum_{l=1}^{m} c_{li}c_{lj} \qquad i,j = 1,...,n$$

This is pre and post multiplied for the diagonal matrix A:

$$A(C^TC)A = \begin{bmatrix} a_1a_1 \sum_{l=1}^{m} c_{l1}c_{l1} & a_1a_2 \sum_{l=1}^{m} c_{l1}c_{l2} & ... & a_1a_n \sum_{l=1}^{m} c_{l1}c_{ln} \\ a_2a_1 \sum_{l=1}^{m} c_{l2}c_{l1} & a_2a_2 \sum_{l=1}^{m} c_{l2}c_{l2} & ... & a_2a_n \sum_{l=1}^{m} c_{l2}c_{ln} \\ ... & & & \\ a_na_1 \sum_{l=1}^{m} c_{ln}c_{l1} & a_na_2 \sum_{l=1}^{m} c_{ln}c_{l2} & ... & a_na_n \sum_{l=1}^{m} c_{ln}c_{ln} \end{bmatrix}$$

This matrix is pre-multiplied by raw vector P^T and post-multiplied by column vector P and therefore $P^TA(C^TC)AP$ is a term in R given by the sum of all elements. The differentiation of this $P^TA(C^TC)AP$ with respect of a_i is :

$$\frac{\partial}{\partial a_i} P^TA(C^TC)AP = 2p_i \sum_{i=1}^{n} p_j a_j \sum_{l=1}^{m} c_{li}c_{lj} \tag{7.25}$$

Putting together equations 7.23, 7.24 and 7.25:

$$\frac{\partial}{\partial a_i} f(A) = 2p_i \sum_{i=1}^{n} p_j a_j \sum_{l=1}^{m} c_{li}c_{lj} + 2p_i \sum_{j=1}^{n} p_j \sum_{l=1}^{m} c_{lh}b_{lj} \tag{7.26}$$

In matricial form, it can be written as:

$$\frac{\partial}{\partial a_i} f(A) = \begin{bmatrix} & L_{i,j} & \end{bmatrix} \begin{bmatrix} a_1 \\ a_i \\ a_n \end{bmatrix} + \begin{bmatrix} M_i \end{bmatrix} \tag{7.27}$$

where:

$$(L)_{ij} = p_j \sum_{l=1}^{m} c_{li} c_{lj} \qquad i,j = 1,...,n$$
$$(M)_i = -\sum_{j=1}^{n} p_j \sum_{l=1}^{m} c_{li} b_{lj} \qquad i = 1,...,n$$

And therefore the n_g coefficients of $[A]$ matrix that minimize vector $[\Delta u_m]$ are:

$$[a] = [L]^{-1}[M] \tag{7.28}$$

7.5 Simulations

7.5.1 Simulation software

When there is distributed generation in a distribution network the P-Q decoupling techniques cannot be used due to the high ratio of R/X [136] and therefore the traditional Newton-Raphson method has to be used to solve the load flow . A software tool to implement the proposed algorithm was chosen. The requirements are the capability to compute a power flow on a network and the possibility to integrate the computation in scripts. PSAT (Power System Analysis Toolbox) is an open source software package for analysis and design of electric power systems [137] [138]. It is based on Matlab and GNU/Octave. This means that it has been developed using Matlab and all its methods can be called from a script inside Matlab or GNU/Octave. Differently from major commercial software programs which are closed and do not permit to change the source code or to add functionalities, PSAT is open source and therefore all algorithms implemented can be read in source code (mainly Matlab code), eventually modified and new algorithms can be added. Being PSAT developed inside Matlab, one of the more popular high level scientific languages, it is very flexible and it is possible to prototype algorithms

as extensions of the ones furnished with the software. Although PSAT includes power flow, continuation power flow, optimal power flow, small signal stability analysis and time domain simulation, only the power flow algorithm was used to implement the proposed voltage control for distribution networks with dispersed generation. A feature offered by PSAT is the capability to draw electrical schemes by means of pictorial blocks. It is possible to draw the electrical scheme to analyze, inside Simulink using the PSAT-Simulink library: all common items useful to represent an electric power systems are offered .

7.5.2 Network test

To test the developed approach a test MV network was used [139] [140]. Fig. 7.9 shows the topology of the network.

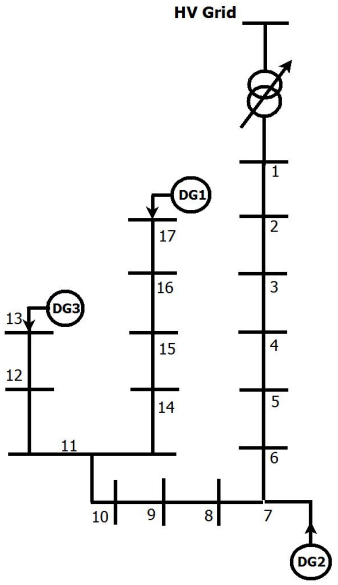


Figure 7.9: Network test - MV industrial test network.

The network was chosen as a typical industrial network. Although most of the Italian Medium voltage (MV) and Low Voltage (LV) are built meshed, connecting different primary or secondary substations, they are operated in radial configuration. The main feeder starts from one end of the substation and ends on the same unit substation on a different busbar but the network is operated in open loop configuration with an automatic line sectionalizer in the middle of the feeder. The schema in Fig. 7.9 represents only one of the feeders downstream of the HV/MV substation: the primary substation is considered a slack bus of infinite power and

therefore no other parallel feeders which emanates from the substation are taken into account. The primary substation is endowed with a transformer of the nominal power of 40 MVA. The MV distribution feeder has 17 buses for an extension of 12 km. At each bus there is a brunch with laterals and sub-feeders: no further detailed representation of the low voltage distribution network was taken into account and therefore at each bus a load or a generator were modeled. From bus 1 to bus 11 the backbone line length is 7.4 km. From bus 11 the feeder is divided into two sub-feeders, the first to bus 17 of length 2.9 km and the second to bus 13 of length 1.6 km. 70% of the line is underground cable (aluminium with a section area from 150 mm^2 to 240 mm^2). 30% of the line is overhead (aerial) copper line with a cross-section of 35 mm^2. The percentage between underground and overhead distribution lines respects the situation of the Italian MV distribution network as presented in [141] (e.g. relatively high power loads and short lines length as it is typical for an industrial network). From bus 7 to bus 9 the cable cross section passes from 150 mm^2 to 35 mm^2 representing a bottleneck. Table 7.1 presents test network lines data

Lines	L[km]	**r** $[\Omega/km]$	**l** $[mH/km]$
1-2	0.942	0.125	0.493
2-3	0.810	0.125	0.493
3-4	0.266	0.125	0.493
4-5	0.642	0.125	0.493
5-6	0.809	0.206	0.608
6-7	0.266	0.206	0.608
7-8	1.000	0.125	0.493
8-9	1.200	0.125	0.493
9-10	1.126	0.206	0.608
10-11	0.378	0.125	0.493
11-12	0.935	0.519	1.957
12-13	0.595	0.519	1.957
11-14	0.640	0.206	0.608
14-15	0.400	0.206	0.608
15-16	1.500	0.519	1.957
16-17	2.000	0.519	1.957

Table 7.1: MV test network lines data.

All loads were modeled as constant PQ loads with value 400 kW with an inductive power factor of 0.85: several different assumption on the loads can be done, but this simplification does not invalidate the results on voltage profile.

Three generators are modeled in the network: being the network of industrial type the hypothesis on the size of the generators is from 2 to 5 MW:

- At bus 7 a power plant with diesel engine motors coupled with synchronous generators for a total size of 2.2 MW;
- At bus 13 a power plant with micro-turbines connected to the grid with static converters for a total of 2 MW;
- At bus 17 a power plant for a total of 5MW composed of gas turbines coupled with synchronous generators.

DG	unit Node	Active power [MW]
DG1	17	5
DG2	7	2.2
DG3	13	2

Table 7.2: Table MV test network generator data..

It is worth nothing that the study concerns only the steady state voltage variations of a distribution feeder with dispersed generation: no dynamic or thermal analysis was carried out.

The test network was modeled in PSAT. As an example a picture of the Simulink model used to introduce the data is shown in Fig 7.10.

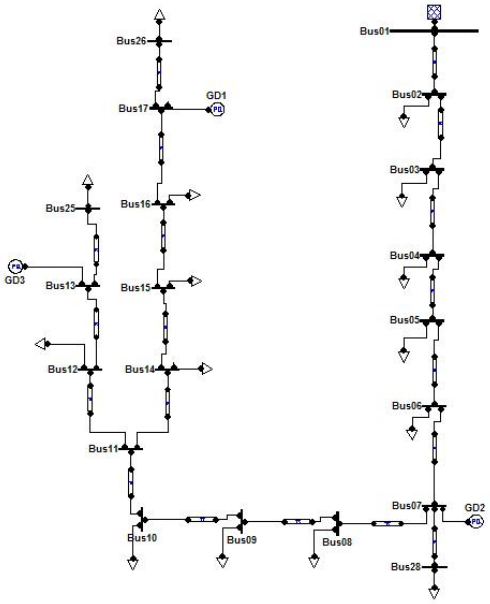


Figure 7.10: Network model - Simulink PSAT model of the test distribution network.

With PSAT is therefore possible to calculate the voltage at each node once both the active power injected in the network by the generators and active and reactive power absorbed from

the network by the loads have been defined. In Fig. 7.11 the voltage profile was calculated in four different situations:

- Red line: all generators inject the nominal active power at unitary power factor (i.e. zero reactive power). It is clearly visible the voltage rise effect;

- Blue line: the feeder is completely passive (i.e. active and reactive power is zero for all three generators);

- Green line: the algorithm described was applied. The three generators (injecting their active nominal power) absorb reactive power following the law (expressed in p.u.):

$$[\Delta q] = [A][\Delta p] = \begin{bmatrix} -0.432 & 0 & 0 \\ -0.009 & -0.437 & -0.010 \\ 0.014 & 0 & -0.430 \end{bmatrix} \begin{bmatrix} 0.125 \\ 0.055 \\ 0.050 \end{bmatrix} = \begin{bmatrix} -0.054 \\ -0.025 \\ -0.021 \end{bmatrix}$$

  In physical units the three generators have the following operating point:

DG unit	**Active power[MW]**	**Reactive power[MVAR]**	$\cos\phi$
DG1	5	-2.16	0.92
DG2	2.2	-1.00	0.91
DG3	2	-0.84	0.92

Table 7.3: Active and reactive power with the proposed control.

- Cyan line: represents the worst case. This happens when the distributed generation is at the nominal value and the load is at minimal value (in the graph the load has been set to zero). The algorithm was applied and therefore the impact of the DG is limited: the reactive power compensate the voltage rise due to the active power generation and therefore the voltage profile is very near to the ideal case (the nominal voltage of the feeder).

The three points circled represent the subset of the buses of the network of cardinality 3 that was chosen: bus 7, bus 11 and bus 17.

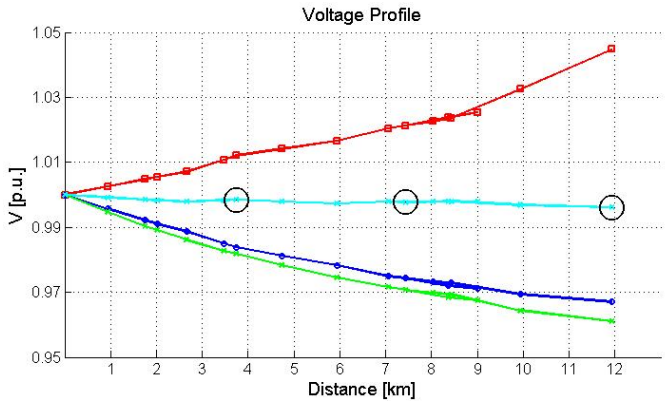


Figure 7.11: Voltage profile - Voltage profile.

7.5.2.1 Diagonal solution

The same network and data is used to find a solution with a diagonal matrix $[A]$. following the matrix $[A]$ and the reactive powers imposed to the three generators:

$$[\Delta q] = [A][\Delta p] = \begin{bmatrix} -0.4321 & 0 & 0 \\ 0 & -0.4673 & 0 \\ 0 & 0 & -0.3934 \end{bmatrix} \begin{bmatrix} 0.125 \\ 0.055 \\ 0.050 \end{bmatrix}$$
$$= \begin{bmatrix} -0.054 \\ -0.026 \\ -0.020 \end{bmatrix}$$

In physical units the three generators have the following operating point:

DG unit	**Active power[MW]**	**Reactive power[MVAR]**	$\cos\phi$
DG1	5	-2.16	0.92
DG2	2.2	-1.03	0.91
DG3	2	-0.79	0.93

Table 7.4: Active and reactive power with the proposed control and diagonal solution.

In Fig. 7.12 the voltage profile for the diagonal $[A]$ solution is shown.

Interestingly, there is a minimal difference in the calculated reactive powers, passing from the full to the diagonal $[A]$ matrix solution. Therefore the adoption of $[A]$ diagonal with the local setup shown in Fig. 7.8 represents the most effective solution, as it can be applied even in case no communication between generators is available.

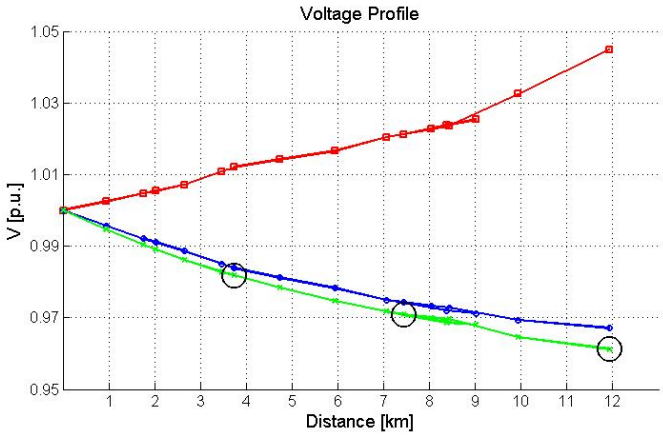


Figure 7.12: - Voltage profile choosing node 7, 11 and 17 with diagonal A.

7.5.3 Choosing the pilot nodes

The subset of network nodes of cardinality M, where the minimization of the voltage rise is acted through the reactive power of the generators, has a similar role of the pilot nodes in the SVR of the transmission grid. The chosen nodes have to be controlled by the actuators, represented here by the distributed generators. Further, the voltage control has to be as inexpensive as possible in terms of reactive power used to control their voltage level. Thus a good number representing the attitude of a node i to be controlled by a given generator j is its sensitivity $\partial V_i/\partial Q_j$. At the same time it is important that the chosen nodes are representative of the voltage rise problem in the feeder (e.g. choosing a node near to the substation that does not suffer from voltage rise effect is useless). It is therefore possible to choose among those nodes presenting the highest voltage rise effects, i.e. for each generator j choosing the node i with the highest sensitivity $\partial V_i/\partial P_j$. The two presented strategies give the same nodes and those nodes are the most impacted by the over-voltage effect.

In the previous examples a more trivial selection of the pilot nodes was done: for each generator a node near the generator was chosen.

The sensitivity of each node to each active power generator injection can be calculated and is presented in table 7.5:

For the first generator the node 17 is chosen having the highest sensitivity value, for the second generator the same node 17 has the highest sensitivity and since it is already in the M set, the second highest is chosen: node 16. For the third generator the node with the highest sensitivity is node 13. Finally the set of controlled nodes is $V_B = 17, 16, 13$.

Bus	$\frac{\partial V_i}{\partial P_1}$	$\frac{\partial V_i}{\partial P_2}$	$\frac{\partial V_i}{\partial P_3}$
1	0.0180	0.0275	0.0244
2	0.0337	0.0514	0.0457
3	0.0389	0.0592	0.0527
4	0.0516	0.0784	0.0698
5	0.0823	0.1189	0.1072
6	0.0924	0.1323	0.1195
7	0.1132	0.1321	0.1471
8	0.1385	0.1318	0.1807
9	0.1829	0.1313	0.2343
10	0.1911	0.1312	0.2451
11	0.1907	0.1309	0.3596
12	0.1902	0.1305	0.4386
13	0.2150	0.1310	0.2447
14	0.2310	0.1308	0.2444
15	0.3803	0.1289	0.2407
16	0.5964	0.1257	0.2349
17	0.1902	0.1306	0.4387

Table 7.5: Sensitivity of nodes to generators active power injection.

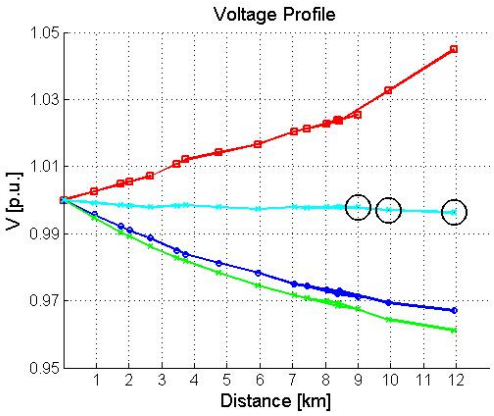


Figure 7.13: - Voltage profile choosing node 17, 16 and 13.

The $[A]$ matrix resulting from the chosen set of nodes is:

$$[A] = \begin{bmatrix} -0.430 & 0 & 0 \\ -0.004 & -0.437 & -0.015 \\ 0.005 & 0 & -0.426 \end{bmatrix}$$

Giving a little difference in the reactive power production:

$$[\Delta q] = [A][\Delta p] = \begin{bmatrix} -0.430 & 0 & 0 \\ -0.004 & -0.437 & -0.015 \\ 0.005 & 0 & -0.426 \end{bmatrix} \begin{bmatrix} 0.125 \\ 0.055 \\ 0.050 \end{bmatrix} = \begin{bmatrix} -0.054 \\ -0.023 \\ -0.023 \end{bmatrix}$$

7.5.4 IEEE-37 bus test network

The proposed strategy has been tested in the IEEE-37 bus MV test network [142]. Fig. 7.14 shows the topology of the network.

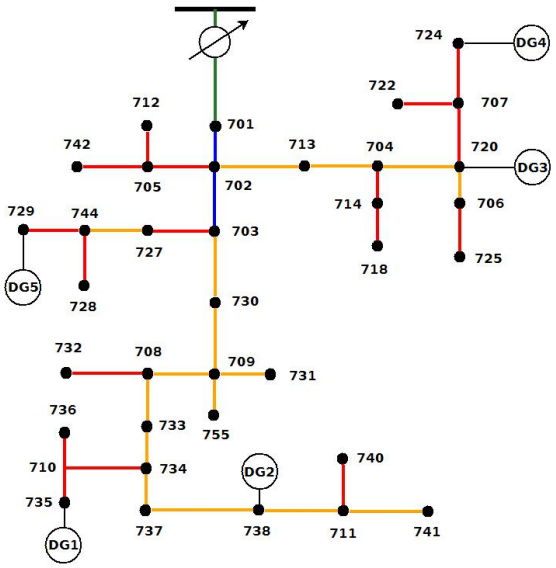


Figure 7.14: IEEE 37 nodes - IEEE 37 bus MV test network.

This test network presents a high R/X ratio of some of the line conductors, which is particularly unfavorable. IEEE 37-bus network comprises four types of cables, colored differently in Fig. 7.14 whose data are reported according to [143] in Table 7.6. Inductances are calculated as in section 2.3 on page 9.

The high R/X ratio makes some bus voltages strongly dependent from active power flows. DGs have been connected to selected buses according to an example presented in [144] and DGs data (all generators are assumed to operate at their nominal active power) are in Table 7.7 (in

Lines	L[km]	**r** $[\Omega/km]$	**l** $[mH/km]$	**x** $[\Omega/km]$	R/X
799-701	0.564	0.065	1.41	0.443	0.147
701-702	0.293	0.129	1.35	0.424	0.304
702-705	0.122	0.480	1.22	0.383	1.253
702-713	0.810	0.480	1.22	0.383	1.253
702-703	0.402	0.129	1.35	0.424	0.304
703-727	0.073	0.606	1.15	0.361	1.679
703-730	0.183	0.480	1.22	0.383	1.253
704-714	0.024	0.606	1.15	0.361	1.679
704-720	0.244	0.480	1.22	0.383	1.253
705-742	0.098	0.606	1.15	0.361	1.679
705-712	0.073	0.606	1.15	0.361	1.679
706-725	0.085	0.606	1.15	0.361	1.679
707-724	0.232	0.606	1.15	0.361	1.679
707-722	0.037	0.606	1.15	0.361	1.679
708-733	0.098	0.480	1.22	0.383	1.253
708-732	0.098	0.606	1.15	0.361	1.679
709-731	0.183	0.480	1.22	0.383	1.253
709-708	0.098	0.480	1.22	0.383	1.253
710-735	0.061	0.606	1.15	0.361	1.679
710-736	0.390	0.606	1.15	0.361	1.679
711-741	0.122	0.480	1.22	0.383	1.253
711-740	0.061	0.606	1.15	0.361	1.679
713-704	0.158	0.480	1.22	0.383	1.253
714-718	0.158	0.606	1.15	0.361	1.679
720-707	0.280	0.606	1.15	0.361	1.679
720-706	0.183	0.480	1.22	0.383	1.253
727-744	0.085	0.480	1.22	0.383	1.253
730-709	0.061	0.480	1.22	0.383	1.253
733-734	0.171	0.480	1.22	0.383	1.253
734-737	0.195	0.480	1.22	0.383	1.253
734-710	0.158	0.606	1.15	0.361	1.679
737-738	0.122	0.480	1.22	0.383	1.253
738-711	0.122	0.480	1.22	0.383	1.253
744-728	0.061	0.606	1.15	0.361	1.679
744-729	0.085	0.606	1.15	0.361	1.679

Table 7.6: MV test network lines data.

the original IEEE description of the network no DG was considered).

DG	**bus Node**	**Active power [MW]**
DG1	735	0.70
DG2	738	1.40
DG3	720	0.60
DG4	724	1.00
DG5	729	1.40

Table 7.7: Table IEEE 37 nodes MV test network generator data.

Network loads are those of the original IEEE document [142] and are summarized in Table 7.8.

Bus	P[kW]	Q [kVar]
701	630	315
712	85	40
713	85	40
714	38	18
718	85	40
720	85	40
722	161	80
724	42	21
725	42	21
727	42	21
728	126	63
729	42	21
730	85	40
731	85	40
732	42	21
733	85	40
734	42	21
735	85	40
736	42	21
737	140	70
738	126	62
740	85	40
741	42	21
742	93	44
744	42	21

Table 7.8: MV IEEE 37 bus test network load data.

The proposed algorithm has been applied to the described network in the case $N_g = M = 5$. Voltage is controlled in five buses chosen according to paragraph 7.5.3 among those buses that presents the highest value of sensitivity on reactive powers injected by generators: 735,740,720, 724, 729.

The full and diagonal $[A]$ matrices are the following:

$$[A] = \begin{bmatrix} -1.1665 & 0.0883 & 0.0452 & 0.0454 & 0.1119 \\ 0.1495 & -1.0740 & 0.0327 & 0.0328 & 0.0808 \\ 0.1351 & 0.1297 & -0.8052 & 0.5638 & 0.1502 \\ -0.0000 & -0.0000 & -0.0000 & -1.3728 & -0.0000 \\ 0.5039 & 0.4795 & 0.2314 & 0.2320 & -0.7210 \end{bmatrix} \tag{7.29}$$

$$[A] = \begin{bmatrix} -0.6604 & 0 & 0 & 0 & 0 \\ 0 & -0.8781 & 0 & 0 & 0 \\ 0 & 0 & 0.9434 & 0 & 0 \\ 0 & 0 & 0 & -1.3689 & 0 \\ 0 & 0 & 0 & 0 & 0.2790 \end{bmatrix} \tag{7.30}$$

It can be seen that all reactive powers calculated would certainly exceed the capability limits of the DGs (being them either synchronous generators or inverter based). Therefore, assuming an average capability limit equal to $|LimQ| = 0.4 * p$ for each DG, a correction on the calculated reactive powers has been introduced according to the following statements:

$$if \quad q > LimQ_+ * (p) \quad then \quad q = 0.4 * p;$$

$$if \quad q < LimQ_- * (p) \quad then \quad q = -0.4 * p;$$

The reactive powers imposed by the algorithm along wit the corrected values are reported in Table 7.9 for the diagonal solution and in Fig. 7.10 for the full A matrix.

DG	**Active power [MW]**	**Reactive power calculated[MVar]**	**Reactive power limited[MVar]**
DG1	0.70	-0.1057	-0.0640
DG2	1.40	-0.2810	-0.1280
DG3	0.60	0.1321	0.0560
DG4	1.00	-0.3285	-0.0960
DG5	1.40	0.0893	0.0893

Table 7.9: Table IEEE 37 nodes MV test network reactive powers imposed with diagonal [A].

DG	**Active power [MW]**	**Reactive power calculated[MVar]**	**Reactive power limited[MVar]**
DG1	0.70	-0.1054	-0.0640
DG2	1.40	-0.2815	-0.1280
DG3	0.60	0.1338	0.0560
DG4	1.00	-0.3295	-0.0960
DG5	1.40	0.0914	0.0914

Table 7.10: Table IEEE 37 nodes MV test network reactive powers imposed with full [A].

With such assumption, voltage profiles of the feeder have been calculated, running a load flow algorithm in PSAT. Results are shown in Fig.5: the blue line is the voltage profile of the feeder with no connected DGs; the red line is the voltage profile with five connected DGs and no mitigation; finally, the green line is the voltage profile with five connected DGs operated according to the mitigation technique. Circled in black are the M=5 chosen buses.

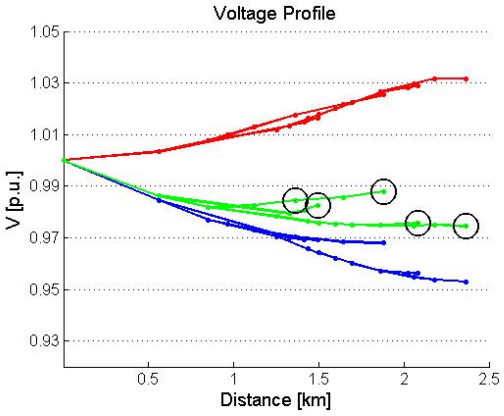


Figure 7.15: - Voltage profile with full [A] matrix.

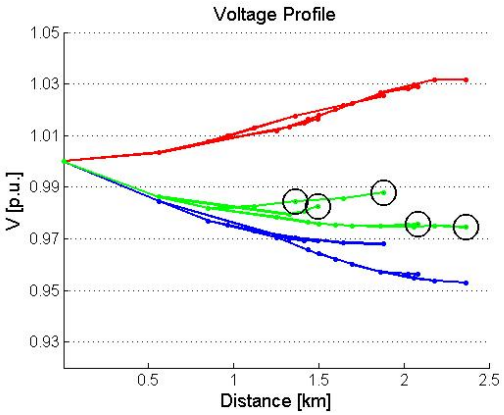


Figure 7.16: - Voltage profile with diagonal [A] matrix.

As in previous test case the diagonal solution is very closed to the full one.

7.6 Voltage Control Systems

The HW/SW platform presented in previous chapters is suitable for implementing coordinated or local reactive power controls directly into the Voltage Control Systems (VCSs) that equip

generators (i.e. ECSs described in chapter 5 for synchronous generators) or inverter voltage controls (for inverter based generators). All functionalities presented in the case of the ECS and of the SART, can be implemented into an inverter based generator endowed with a similar control device as well.

Therefore the proposed proposed platform can be considered as a smart VCS provided with embedded ICT capabilities so that it can operate in the grid as an intelligent electronic device. It take full advantage from ICTs [145] [146] [147]. As shown in chapter 4, communications with SCADA or DCS systems have been already implemented and tested using common software protocols based on TCP and UDP over IP.

7.7 Conclusions

The voltage rise problem in distribution networks when in presence of distributed generation has been presented. A simple algorithm, that can be applied to different communications architectures, has been detailed. For synchronous generators this algorithm can be implemented using Smart ECS embedding control as those shown in chapter 5 and their communication capabilities. Simulations on test MV networks have been carried out

8

Conclusion

The electric power system is a very complex and huge system with several active devices and for years it has been considered the most complex system ever made by humans. In the last three decades the development of the Internet has lead to the building of another very complex system.

Even though the two systems are different, several technologies from the ICT world are introduced into the electrical systems:

- computation equipment born for personal use becomes suitable for control device development;
- operating systems introduced for general purpose use become real-time operating systems;
- network protocols designed for office local area networks are ported to industrial environment.

The introduction of these new elements opens up new possibilities.

In this thesis a work resulting from a collaboration between the University of Trieste and an Italian firm involved into the development of voltage control devices is presented: excitation control systems for synchronous generators and automatic voltage control systems for power plants were developed.

Both devices were firstly developed as analogue devices, then migrated with digital technology implemented on dedicated hardware and now are developed on general computing systems.

The major motivations of this late migration are economical aspects, but the introduction of this new elements brings also new design methodologies.

In this work, one of these new methodologies with its development tools was introduced. The aim was to show the concrete possibility to implement control devices useful to power systems using RTAI and its extension called RTAI-Lab. A Linux OS extended with RTAI can operate as a RTOS keeping latencies bounded within tens of microseconds, thus becoming feasible for real-time applications, as excitation control systems and reactive power regulators. Therefore, using RTAI, it is possible to utilize cost-saving GPPs and data acquisition boards for HRT applications. Furthermore, the employment of an OS that can run on personal, industrial, miniaturized or even embedded computers, makes it possible to scale the hardware solution to very different needs without changing the architecture and the software platform.

Control algorithms can be designed and written using high-level programming language tools, provided with automatic code generation.

Development procedure consists in creating the control system model in MATLAB/Simulink or Scilab/Scicos, incorporating a model of the controlled plant for validation purposes. Once validated through simulation, the control system model is compiled using the code generator for the RTAI target and a C compiler.

The adoption of COTS PCs endowed with Linux RTAI, together with the above stated development procedure, brings to the user relevant advantages.

The distributed SART architecture shown, stresses on the communication facilities offered by the chosen platform: software libraries, protocols and development tools give the control designer the appropriate tools to effectively interface the device with the power plant control system.

New applications are arising in the distribution network as it is changing from a passive network to an active one, with the emerging production of energy into the multitude of little generators.

The presented platform, with its communication capabilities and development tools can be used in the distributed control architecture of the future Smart Grid. The specifications for the communication system underlying the future power distribution network, has not been yet completed because of the need to support a great variety of applications, many of which have not yet been designed. It is commonly believed that all future communications for power system control will use the IP family to allow interfacing all the control devices over multiple media and both public and private networks.

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