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DOTTORATO DI RICERCA IN INGEGNERIA DELL'INFORMAZIONE

DESIGN OF HIGH-PERFORMANCE, APPLICATION-SPECIFIC ANALOG-TO-DIGITAL CONVERTERS

DOCTORAL THESIS

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This thesis is dedicated to my family, my friends and whoever, even only with a small talk, has contributed to this work.

I don’t always design amplifiers...
but when I do they make great oscillators.

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Summary

FROM the birth of the first digital computers, Analog-to-Digital Converters (ADCs) have gained more and more importance in every fields of electronics. From very high-speed digitizers required for wireless and wired data link, to very high-resolution converters for environmental sensor interfacing, ADCs with very high performances must be designed. It is possible to divide the world of the Analog-to-Digital Converters according to requirements of the target applications, basically high-speed and high-resolution. Different architectures have been developed and different parameters are used to evaluate their performances, depending on the specific fields of interest. From the examples that will be described, it will look evident how general-purpose solutions cannot fulfil so different design spaces in an efficient way. Data acquisition systems for sensor interfacing, as requested in wireless sensor networks for environmental monitoring, must be very accurate, keeping low power and area consumptions. The ADC is one of the most pivotal blocks in the acquisition chain. Its presence is essential due to the need to process, storage or transmit the information: all operations that can be realized very efficiently only in the digital world. The design of electronics for sensor nodes powered by energy harvesters or for wearable devices can be even more challenging, due to the need to keep the power consumption as low as possible, often working with supply voltage domain of few hundreds of millivolts. Extreme environments as dilution fridges, where physical experiments on qubits for quantum computing applications, can also host classical electronics, so that specific design techniques must be employed for the design of analog-mixed electronics, including analog-to-digital converters.

In this work of thesis, a full description of the design of three different Analog-to-Digital Converters will be presented. The different target specifications will require different architectures and specific solutions that will be deeply analysed. First, a Delta-Sigma (Δ-Σ) Analog-to-Digital Converter optimized for low-frequency signals has been developed. A complete description of the high-level and transistor-level design allows a full comprehension of the complex challenges for the fulfilment of high-accuracy and high-resolution specifications, as typically required for sensor interfacing. In particular, offset and low-frequency noise could be especially detrimental due to the

bandwidth of interest of the input signals, in the range from the dc to few kilohertz. A system-level chopper stabilization technique has been fully analysed and implemented. Thanks to this technique, it has been possible to reach an offset on the order of few microvolts and a rms noise voltage of tens of microvolts.

Looking at the high demanding of low-power and low-voltage electronics for wireless sensor networks, possibly powered by energy harvesting devices, a Δ-Σ converter capable of working with supply voltage as low as 200 mV has been realized. Typical issues of low amplifier dc-gain and low-headroom for MOSFET devices are faced by means of a novel switched-capacitor, inverter-based integrator. The ultra-low power and ultra-low voltage converter has been simulated, showing good performances, as summarised by the figure-of-merit of 42.4 fJ/conv with $V_{dd} = 0.3V$. To prove the effectiveness of the proposed inverter-based integrator, a simple single-order Δ-Σ modulator has been designed with the 0.18 μm CMOS process. Measurements on a test chip show the functionality of the converter with supply voltage as low as 0.2 V, with very low power consumptions.

Finally, the design of an high-speed Successive Approximation Register (SAR) converter for extreme environment applications is proposed. It has been optimized for quantum computing application, more precisely for radio-frequency reflectometry interface for spin qubit readout. A new challenge in the design of classical electronics for quantum computing is the compatibility with cryogenic temperatures (4 K), in order to improve the scalability of the actual quantum computers. A ping-pong SAR converter with a maximum sampling frequency of 1 GHz and a resolution of 6 has been developed. Additional programmability allowed the increasing of the converter resolution up to 9 bit, at the cost of some speed penalties. Novel techniques in the converter topology and in the switching algorithm scheme have been developed in order to face the changing of MOSFET behaviour at cryogenic temperatures.

List of publications

International Journals

1. Piotto, M., Catania, A., Nannini, A. and Bruschi, P. (2020). Thermal noise boosting effects in hot-wire based micro sensors. *Journal Of Sensors*.

2. Bruschi, P., Catania, A., Del Cesta, S. and Piotto, M. (2019, 3). A two-stage switched-capacitor integrator for high gain inverter-like architectures. *IEEE Transactions on Circuits and Systems II: Express Briefs (TCASII)*. IEEE.

International Conferences/Workshops with Peer Review

1. Benvenuti L., Catania A., Cicalini M., Ria A., Piotto M. and Bruschi P. (2019,7). A 0.3 V 15 nW 69 dB SNDR Inverter-Based Δ-Σ Modulator in 0.18 μm CMOS. *15th Conference on Ph. D Research in Microelectronics and Electronics (PRIME)*. IEEE.

2. Ria A., Catania, A. Cicalini, M. Benvenuti L., Piotto M. and Bruschi P. (2019,7). A Sub-1V CMOS Switched Capacitor Voltage Reference with high output current capability. *15th Conference on Ph. D Research in Microelectronics and Electronics (PRIME)*. IEEE.

3. A. Catania, A. Ria, S. Del Cesta, M. Piotto, P. Bruschi, (2018,7). Analysis and simulation of chopper stabilization techniques applied to Delta-Sigma converters. *15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*. IEEE.

4. A. Ria, S. Del Cesta, A. Catania, M. Piotto, P. Bruschi, (2018,7). Improved class-AB output stage for Sub-1 V fully-differential operational amplifiers. *14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*. IEEE.

5. S. Del Cesta, A. Catania, M. Piotto, P. Bruschi, (2017,9). A compact sub-1V class AB operational amplifier for low-voltage switched-capacitor circuits. *European Conference on Circuit Theory and Design (ECCTD)*. IEEE.

6. A. Catania, S. Del Cesta, M. Piotto, P. Bruschi, (2017,6). Design of current feedback instrumentation amplifiers with rail-to-rail input-output ranges. *13th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*. IEEE.

List of Abbreviations

Symbols

FoM_S	Schreier Figure of Merit. 19, 20
FoM_W	Walden Figure of Merit. 5, 14, 19, 90
Δ-Σ	Delta-Sigma. V, IX, XI, XII, 10, 16–20, 22, 24–39, 41, 43–51, 53, 55, 57, 59, 66, 68, 83–85, 87–91, 93, 126, 130

A

ADC	Analog-to-Digital Converter. V, 1–3, 5–7, 10, 11, 14–17, 66, 69, 93, 136
AFE	Analog Front-End. 1
ASIC	Application-Specific Integrated-Circuit. 2

B

BER	Bit Error Rate. 6, 11

C

CDS	Correlated Double Sampling. 16
CHS	CHopper-Stabilization. 24, 35, 37
CIC	Cascaded Integrator-Comb. 31, 42
CMFB	Common-Mode FeedBack. 38

D

DAC	Digital-to-Analog Converter. 1, 12
DEM	Dynamic Element Matching. 16
DNL	Differential Non-Linearity. 7
DUT	Device Under Test. 47, 48

E

EIS	Electrochemical Impedance Spectroscopy. 47

ENOB Effective Number Of Bits. 5
ERBW Effective Resolution BandWidth. 5

F
FD Fully-Differential. 37
FIR Finite-Impulse Response. 29

I
INL Integral Non-Linearity. 7
IOT Internet Of Things. 2, 15

L
LSB Least Significant Bit. 3

M
MASH Multi-stAge noise-SHaping. 32

N
NTF Noise Transfer Function. 25

O
OSR OverSampling Ratio. 9

P
PSD Power Spectral Density. 3, 9, 10

S
SAR Successive Approximation Register. V, 12, 13
SC Switched-Capacitor. 16
SFDR Spurious Free Dynamic-Range. 5
SINAD SIgnal-to-Noise And Distortion ratio. 5
SIP System-In-a-Package. 2
SNDR Signal-to-Noise and Distortion Ratio. 5
SNR Signal-to-Noise Ratio. 4, 5, 10, 30
SOC System-On-a-Chip. 2
SQNR Signal-to-Quantization Noise Ratio. 5
STF Signal Transfer Function. 25

T
THD Total Harmonic Distortion. 5

Contents

Introduction

Exploring the whole world of Analog-to-Digital Converters in a PhD thesis is practically impossible, due to the extent of the subject. This work focuses on the design of two different kinds of converters: Δ-Σ and SAR ADCs. Discrete-time Δ-Σ modulators lead in the design space of high-resolution data converters. Furthermore, the inverter-like approach applied to switched-capacitor integrators allows a large scaling of the supply voltage and of the power consumption, and consequently it opens the way to ultra-low voltage and ultra-low power Δ-Σ modulators. SAR converters, on the other hand, can reach very high sampling frequencies with high energy efficiencies, compared to other high-speed architectures as pipeline or full-flash converters. Moreover, the SAR converter is one of the architectures that takes the most advantage from technology scaling, thanks to its high number of digital operations. For the same reason, its functionality is also compatible with harsh environments as cryogenic temperatures.

From here on out, the outline of this PhD thesis will be provided.

In Chapter 1, a general introduction about analog-to-digital converters will put the basis for the following discussions. A brief overview about the main parameters which describe the Analog-to-Digital converter performances and the most diffused architectures (classified for high-speed and high-resolution applications) are described. A final survey about the actual state-of-the-art of scientific and commercial ADCs will end this introductive chapter.

In Chapter 2, an initial description of Delta-Sigma converters is provided. The design of a high-resolution converter optimized for the digitalization of low-frequency signals (as the ones from sensor acquisition systems) is described in details, focusing on the implementation of two dynamic offset cancellation techniques and an energy-efficient slew-rate enhancement circuit. Measurements on a silicon prototype will show the actual performances of the proposed converter.

In Chapter 3, the design of an ultra-low voltage (ULV) Delta-Sigma converter is described, after an initial overview about ULV CMOS design techniques. The ultra-low voltage operations are allowed by means of an innovative switched-capacitor, inverter-like integrator, that will be fully described. Measurements on the ASIC will confirm the functionality of the converter for supply voltage down to 0.2 V.

Chapter 4 describes the design of a cryo-CMOS, high-speed Successive Approxima-

tion Register converter for quantum computing applications. A brief dissertation about quantum computing technology and cryo-CMOS design will contextualize the work and the main challenges related to this new branch of engineering. A full description of the proposed converter is provided, focusing on the challenges related to cryo-CMOS design. This work has been developed during the six months of research stay at Applied QUantum Architecture (AQUA) department at TU Delft, in The Netherlands.

Appendix A will provide some analytical derivations for switched-capacitor circuits, applied in particular to switched-capacitor integrators. Important non-idealities as amplifier finite dc gain, offset and noise will be also taken into account.

CHAPTER 1

Overview of Analog-to-Digital Converters

1.1 Introduction

In this first chapter, a brief overview on the Analog-to-Digital Converters (ADCs) is provided. An ADC is the electronic circuit able to convert the information from the analog to the digital domain. The inverse operation (from the digital domain back to the analog one) is implemented by the Digital-to-Analog Converter (DAC).

Every physical quantity present in the environment is representable through an analog signal. An analog signal is a time-varying, continuous signal, that can assume every values inside a certain range. Some examples of physical quantities that can be described by analog signals are the atmospheric pressure, the temperature in a room, or the concentration of a specific gas in the air. All these signals can be acquired by an appropriate sensor, in order to obtain useful information on the surrounding environment. Once the sensor's transducer has converted the physical quantity in an electrical quantity (usually a voltage, a current or a charge), the analog electrical signal must be properly elaborated by an Analog Front-End (AFE) and then converted in the digital domain, by means of an ADC.

The digital conversion is almost always mandatory, in order to storage the useful information, effectuate more elaborate signal processing and transmit the data to other devices. These operations are much more efficient when effectuated in the digital domain, compared to the operations allowed in the analog domain. For this reason, the signal processing of the AFE is typically limited to few essential operations, such as amplification and filtering.

The above mentioned application is just one of the many where analog-to-digital conversion is pivotal. It is hard to find electronic fields where the ADCs are not employed. Conversion of audio or video signals for signal processing and storage on disk; conversion of high frequency signals in RF receivers; low-power digitalization

of signals from bio-sensors for wearable electronics; multiple-channel ADCs for microcontrollers; very high-performance converters for electronics test bench. These are only some of the all the possible systems where specific converters are required.

It is easy to guess how so different fields demand very different (often contrasting) specifications for the electronics. A unique ADC architecture can not fulfil all the different requirements. The main characteristics of data converters are: i) speed (i.e. the capability of digitalize high frequency signals, usually expressed in terms of converted samples per second, or SPS), ii) power consumption, iii) resolution, that is a measure of the capability of not spoiling the signal fidelity during the conversion.

Electronic data converters appeared for the first time in the 50s [1], and from the first example of commercial product, gigantic steps were made. The first commercial ADC is believed to be introduced in 1954 by Epsco Engineering. It was an 11-bit, 50 kSPS successive-approximation converter based on vacuum-tube. The power dissipation was around 500 watts, with considerable dimensions (19" × 15" × 26") and price ($8000 to $9000).

A part from the outstanding improvements of the technological processes (especially CMOS processes), with consequent benefits in terms of costs, performances, and dimensions, new ADC architectures have been introduced. Research on this field has been very fertile in the last decades and it does not show signs to slow down, due to the high demanding of more and more efficient solutions. Also actual commercial ADCs present on the market explore the whole design space and reach very high performances: sampling rates up to tens of GSPS [2], resolutions up to 32 bit[1] [3] and power consumptions down to 900 nW [4].

However, discrete components can not be employed everywhere, especially in highly specific applications where only Application-Specific Integrated-Circuit (ASIC) solutions are allowed. In sensor readout interface, for example, System-On-a-Chip (SOC) or System-In-a-Package (SIP) are usually employed. Typical SOC solutions for Internet Of Things (IOT), for example, includes the whole embedded system of data acquisition, from the sensor device to the digital communication protocol in a single chip. The design of low-power and very compact electronic circuits is the key to achieve successful products. In the last years, more and more interest has grown around wireless sensor network and wearable electronics, together with the research on energy harvesting devices [5] and implantable sensors [6].

In this work, the design of three different Analog-to-Digital Converters for highly specific applications will be presented. Before going into details of the design strategies, the transistor-level choices and the novel techniques implemented to achieve the target performances, the definition of the most important parameters for Analog-to-Digital Converter will be provided. Then, a brief overview on the most popular data converter architectures will be presented, classifying them in two great groups: high-speed and high-resolution. At the end of this chapter, the trends of research and commercial data converters will be summarized.

[1] Nominal resolution, not effective resolution. See 1.2.1 section for more details.

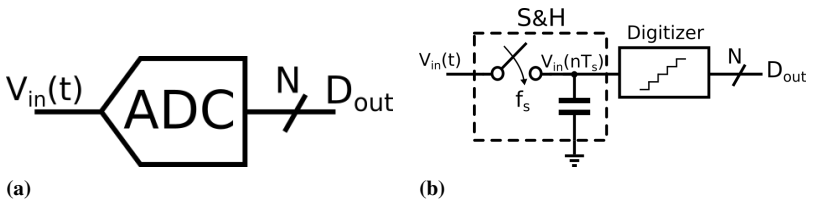

Figure 1.1: *(a) Symbol of the ADC. (b) Ideal view of an ADC.*

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1.2 ADC parameters

Every Analog-to-Digital Converter can be represented as the cascade of a sample-and-hold and a digitizer (Fig.1.1). The sample-and-hold (in the simplest case implemented by a switch, controlled by a proper clock signal, and a capacitor), is the circuit responsible for the sampling of the input signal. The clock signal that drives the switch, called sampling signal (with a certain frequency f_S), is strictly related to the speed of the converter. In order to properly sample the input signal, according to the Nyquist–Shannon sampling theorem, f_S must be at least two times the bandwidth of the input signal, or higher. The presence of spurs outside the frequency range $[0, f_S/2]$ will cause signal distortion, through aliasing. Aliasing is the down-conversion of frequency components placed outside $[0, f_S/2]$ to the signal bandwidth [7], due to the sampling operation. Low-pass filters, also called anti-alias filters, are typically placed before the ADC. Depending on the sampling frequency or the required accuracy, the design of the anti-alias filter could be very critical. Electrical noise will suffer of aliasing phenomenon as well, known also as noise-foldover. Noise foldover will cause an increase of the noise Power Spectral Density (PSD) in the signal bandwidth. More hints about noise foldover operating principle will be given in paragraph 1.3.

The digitizer (or quantizer), instead, is the block that converts the analog sampled signal in a digital code, expressed with a word of N bits. N is called the nominal resolution (sometimes only resolution) of the ADC, and it is related to how the ADC output is "alike" to the input signal. The smallest variation of the input signal that can be recognized is the quantity that generates a variation of one Least Significant Bit (LSB) in the output code. As it can easily foreseen, the higher is N (i.e. the number of quantized levels on the output) and the better is the fidelity of the output signal compared to the input one. Apart from the specific converter architecture complexity, already the operations of sampling and quantization involve several implications that it is worth highlighting. As already mentioned, the sampling operation introduces aliasing and noise fold-over. The quantization of the input signal, on the other hand, will introduce an error due to the limited number of quantized levels, compared to the infinite levels assumed by an analog signal. Other non-idealities, such as electrical noise and harmonic distortions, will further penalise the converter performances. In order to evaluate and compare different ADCs, several parameters have been defined.

First, we will see the definition of some important parameters related to the dynamic performances of the converter. Dynamic parameters characterize the ADC performances with respect of an input tone with a frequency inside the converter bandwidth. Finally, static parameters, concerning the presence of dc input signal, will be

defined.

1.2.1 Dynamic Parameters

The operation of quantization introduced by the digitizer consists in the representation of the sampled signal with a quantized number of levels 2^N. The input signal is generally included in a certain range $[0, V_{FS}]$ or $[-V_{FS}/2, -V_{FS}/2]$ (depending if the converter is unipolar or bipolar), where V_{FS} is called the full-scale range of the converter.

In the previous paragraph, it was already mentioned the fact that quantization introduces an error, called quantization error, that affects the output signal. The higher is the number of quantized level (i.e. the converter resolution N), the lower is this error on the output code. The shape of the quantization error is strictly related to the input signal and the number of quantization levels, as it looks evident from Fig.1.2. Quantization error (ϵ_q) is evaluated as the subtraction of the input signal and the converter output code (multiplied for the full-scale range). Trivially, if the converter input is a dc signal, the quantization noise will be constant and its spectrum will have only a dc component. If the converter resolution is high enough, the input signal is fast enough (compared to the sampling frequency) and it has an amplitude large enough (compared to the full-scale range) as the sinusoid in Fig.1.2, then it is reasonable to consider the quantization error as random and independent from the input signal.

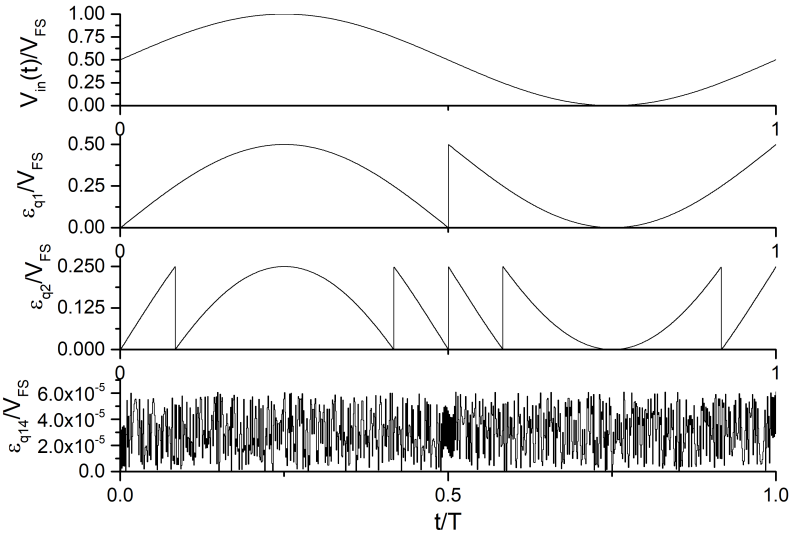

Figure 1.2: *Quantization errors of 1 bit, 2 bit and 14 bit perfect ADCs, with a full-scale sinusoidal input (graph on top).*

Under certain conditions of the input signal and the resolution N, it is reasonable to consider the distribution of the quantization error (also called, erroneously but in an universally accepted way, quantization noise) with an equal occurrence probability, i.e. with a white spectrum. Considering this assumption, it is demonstrable that the quantization noise has a power spectral density uniformly distributed between 0 and $f_s/2$, with a power of $\Delta^2/12$, where Δ is the quantization step, defines as: $\Delta = V_{FS}/2^N$.

It is already possible to evaluate the Signal-to-Noise Ratio (SNR) of an ideal ADC where only quantization noise is present. In these conditions, the SNR is also called SQNR (Signal-to-Quantization Noise Ratio). For these calculations, a full-scale sinusoidal tone is considered as input signal.

$$SQNR = \frac{V_{FS}^2/8}{\Delta^2/12} = \frac{V_{FS}^2/8}{V_{FS}^2/(2^{2N}12)} = \frac{3}{2}2^{2N} \tag{1.1}$$

The SQNR is usually expressed in dB as:

$$SQNR|_{dB} = 6.02N - 1.76 \tag{1.2}$$

Eq.1.2 is a fundamental expression for Analog-to-Digital Converters, because it easily relates the resolution of the converter N with the SNR.

In a real ADC, other noise sources, such as electrical noise and jitter, will reduce the value of SNR compared to the ideal value of SQNR. Moreover, non-linearities introduced by the converter, will further worsen the ADC performances. Typically, the SIgnal-to-Noise And Distortion ratio (SINAD, also called SNDR) is used, taking into account all the non-idealities affecting the converter.

$$SINAD = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{1.3}$$

P_{noise} will be the sum of the powers of quantization noise and of the other noise sources, in the converter bandwidth B_W (that in several converters coincides with the Nyquist frequency, i.e. half of the sampling frequency f_S). Starting from 1.2 and replacing SQNR with SINAD, it is possible to extrapolate the information on the effective resolution of the converter, expressed in Effective Number Of Bits (ENOB).

$$ENOB = \frac{SINAD|_{dB} - 1.76}{6.02} \tag{1.4}$$

The difference between the nominal resolution and the effective resolution is a measure of the degradation of the performances due to the additional errors introduced by the converter besides quantization noise, that is intrinsically present.

The SNR and the SINAD are typically function of the input signal frequency, for a certain sampling frequency. The frequency such that the SNR is 3 dB lower compared to the SNR peak is called Effective Resolution BandWidth (ERBW). If the ERBW is higher than half of the sampling frequency, the ADC is a Nyquist converter, in the sense that it is able to guarantee proper conversions in the whole Nyquist bandwidth.

Only considering the definition of effective resolution, it is possible to provide a first figure of merit, called Walden Figure of Merit (FoM_W)[2] [8]. FoM_W evaluates the ADC performances in terms of power consumption, speed (i.e. sampling frequency) and resolution:

$$FoM_W = \frac{P_D}{2^{ENOB} f_S} \tag{1.5}$$

[2] Actually, the original FoM in [8] is defined as the inverse of the one universally accepted.

In order to evaluate the converter linearity, two main parameters are used: the Total Harmonic Distortion (THD) and the Spurious Free Dynamic-Range (SFDR), respectively defined as:

$$THD = \frac{P_{distortion}}{P_{signal}} = \frac{\sum_{i=2}^{M} P_i}{P_1} \tag{1.6}$$

$$SFDR = P_{signal} - P_{spur} \tag{1.7}$$

Where P_1 is the power of the fundamental (i.e. of the signal), P_i is the power of the i-th harmonic and P_{spur} is the power of the largest spur introduced by the converter inside the signal bandwidth.

Other parameters are used to evaluate the converter performances, depending on the specific applications.

- Bit Error Rate (BER) is typically used for high-speed data converters. BER is the ratio of the number of wrong bits observed to the total number of bits in a bit stream. A typical cause of BER increase is due to comparator metastability, as deeply analysed for different architectures in [9–11]. Depending on the kind of application, more or less strict BER requirements are present. In Bluetooth communications, BER should be lower than 10^{-4}, while in UWB communications or in Serial Link, a BER lower than 10^{-12} is required.

- Settling time of an ADC is the time occurring from a variation of the input signal to the settling of the output code (within a certain range) at the final value. This parameter can be relevant when a single ADC is used to convert signals coming from different channels, in time-division multiplexing fashion. Usually, the converter settling time is related to the converter latency, that is the delay between the sampling of the input and the appearance of the relative output code.

- The aperture time is the delay between the ideal sampling instant and the actual moment when the sample-and-hold starts holding the input signal. Due to skew or time jitter, the moment when the input signal is sampled could have a systematic delay (clock skew) or a random uncertainty (clock jitter) different from period to period. Time jitter reduces the signal-to-noise ratio and it may be detrimental in high-speed converter [7]. Time skew, besides introducing an additional phase shift between the input signal and the sampled signal, is critical in time-interleaving ADCs, where different skews in the different channels introduce additional spurs in the output spectrum [12].

1.2.2 Static Parameters

The evaluation of ADC static parameters start from the dc input-output characteristic. Sweeping the converter full-scale range with a dc input signal, the converter input-output characteristic results in a staircase, as shown in Fig. 1.3. The ideal ADC is the perfect sample-and-hold, i.e. a converter with infinite resolution. The perfect ADC is a converter with resolution N, and no errors. The following definitions are taken from [13].

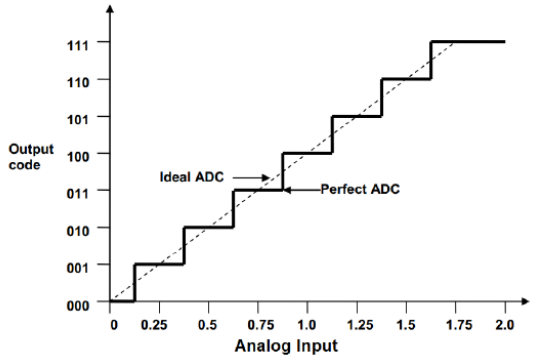

Figure 1.3: *Characteristics of an ideal ADC and a perfect 3-bit ADC. Graph taken from [13].*

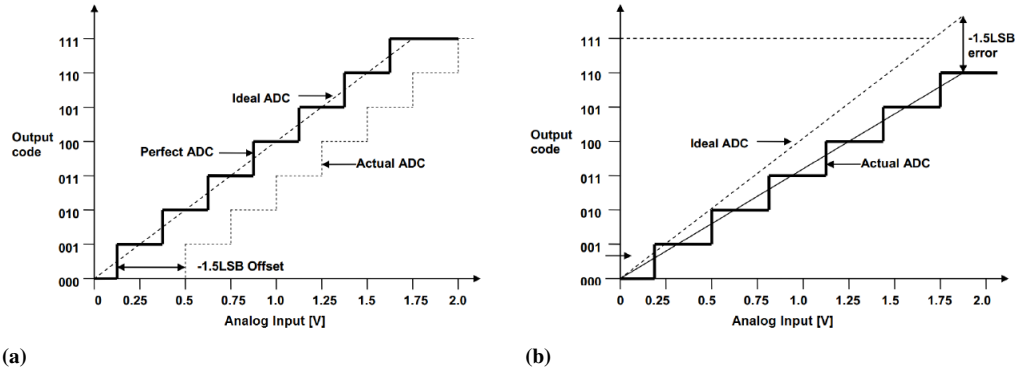

Figure 1.4: *(a) Offset error. (b) Gain error. Graphs taken from [13].*

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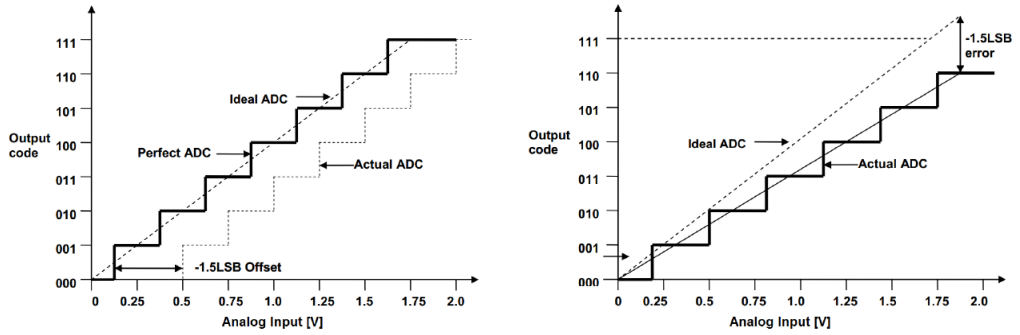
The offset error is defined as the difference between the actual ADC characteristic and the perfect ADC characteristic, evaluated at the zero transition (Fig.1.5-a). It is usually expressed in LSB, or as a voltage, multiplying the code for the value of the quantization step Δ. The gain error is the difference between the last step midpoint of the actual ADC and the last step midpoint of the ideal ADC, after the compensation of the offset error (Fig.1.5-b). The presence of a gain error causes the deviation of characteristic slope from the unity slope of an ideal converter.

After the compensation of offset and gain erros, the converter characteristic should be the same as the one of a perfect ADC. Additional deviations of the actual characteristic are measured through the parameters Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). DNL is the difference in the step width between the actual characteristic and the perfect one. Presence of DNL errors are reflected in quantization steps of varying widths (Fig.1.6-a). Often with the term DNL, the maximum DNL is hinted, expressed as a function of the LSB. If the ADC has a DNL lower than the LSB, no missing codes are present. INL is the vertical difference between the actual input-output characteristic and the ideal one (Fig.1.6-b). INL gives a useful information on the kind of non-linearities which affect the converter. The behaviour of INL respect to the input voltage is a sort of "signature" of the kind of converter architecture. As for the DNL, with INL is often expressed its maximum value (as a function of the LSB).



(a) (b)

Figure 1.5: *(a) Offset error. (b) Gain error. Pictures taken from [13].*

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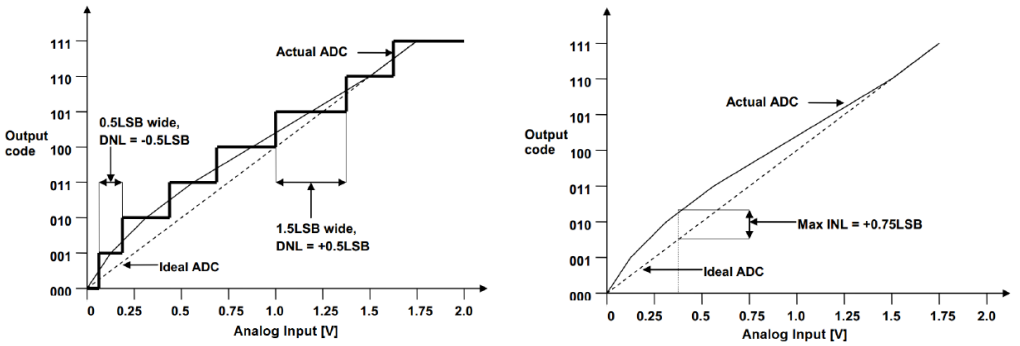

(a) (b)

Figure 1.6: *(a) DNL. (b) INL. Pictures taken from [13].*

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Working with ADC optimized for dc input signals, it is not worth using the definition of effective resolution defined in 1.6. An alternative definition of effective resolution (called ER to not be confused with the ENOB definition) in [14] can be easily applied for ADC fed with dc input signal.

$$ER = log_2\left(\frac{V_{FS}}{\sigma_n}\right) \tag{1.8}$$

This definition is very similar to the one used to evaluate the resolution of a generic electronic block, where the base-2 logarithm of the dynamic-range is used. The dynamic-range is typically defined as the ratio between the maximum signal (the full scale range) and the minimum signal (given by the noise-band) of the system. The noise-band is the peak-to-peak noise voltage, expressed as $k\sigma_n$, where k is two times the crest factor and depends on the required precision of the system. In the next chapters, for the estimation of dc performances of the proposed converters, 2.3.1 will be used, considering the peak-to-peak noise voltage instead of the rms noise voltage for a fair characterization, also called noise-free resolution [14].

1.3 Nyquist Converter and Oversampled Converter

The choice of the sampling frequency f_S compared to the signal bandwidth B_W can make a real difference on the converter performances. Already considering an ideal ADC as the one in Fig.1.1, a sampling frequency higher than two times the signal bandwidth (also called "Nyquist rate") introduces benefits for the converter resolution.

As already mentioned, under certain conditions about the input signal and the converter resolution, it is fair to consider quantization noise PSD uniformly distributed in the range $[0, f_S/2]$ [7]. The power of quantization noise is independent by the sampling frequency, while the PSD is inversely proportional to f_S. With a sampling frequency higher than Nyquist rate, it is possible to low-pass filter the quantization noise rejecting the out-bandwidth contribution, as shown in Fig.1.7. Defining the OverSampling Ratio (OSR) as the ratio between the sampling frequency f_S and the Nyquist rate $2B_W$, the increase of resolution due to oversampling operation can be expressed as:

$$SNR_{OVS} = \frac{P_{signal}}{\int_0^{B_W} S_{q-n} df} = \frac{P_{signal}}{\frac{\Delta^2}{12}\frac{2B_S}{f_S}} = \frac{SNR_{Nyq}}{OSR} \tag{1.9}$$

$$N_{OVS} = N_{Nyq} + \frac{1}{2}OSR \tag{1.10}$$

An analogous behaviour it is also valid for other white noise sources, as thermal noise. Considering a white noise source with power spectral density S_{BB}, filtered by a first order low-pass transfer function (as the typical noise spectrum of an amplifier with dominant-pole transfer function), the sampling operation introduces noise fold-over, as depicted in Fig.1.8. For sake of simplicity, it is possible to represent the PSD as constant and equal to S_{BB} in the frequency range $[0, B_{eq-n}]$ and null outside, where B_{eq-n} is the equivalent noise bandwidth of the system. Due to the sampling operation, the resulting PSD is the sum of infinite replicas of the initial PSD shifted by multiples of the sampling frequency f_S [15]. In the frequency range of interest ($[0, f_S/2]$), the PSD will result increased of a factor $2B_{eq-n}/f_S$. Analogously to quantization noise,

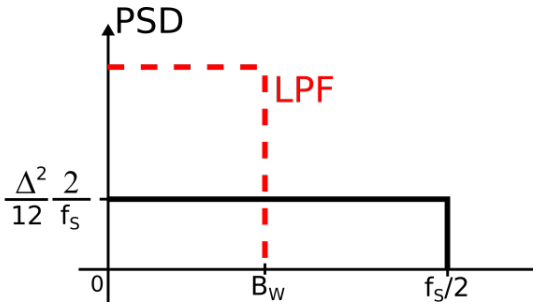

Figure 1.7: *Spectrum of quantization noise, with sampling frequency higher than the signal bandwidth.*

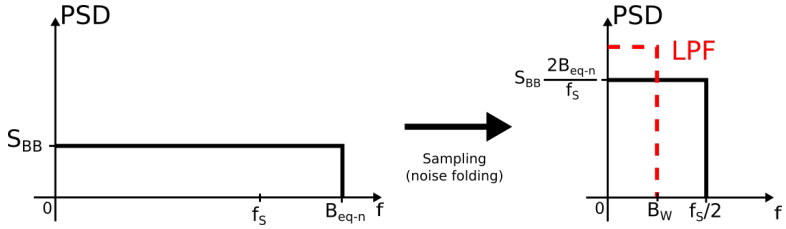

Figure 1.8: *Noise spectrum after sampling, with a sampling frequency higher than the signal bandwidth.*

choosing a sampling frequency higher the Nyquist rate and filtering with a low-pass filter (so far considered ideal) with cut-off frequency B_W, a reduction of noise power is obtained, compared to the case $f_S = 2B_W$.

$$P_{n-Ov} = \int_0^{B_W} S_{sampled}(f)df = S_{BB}\frac{2B_{eq-n}}{f_S}B_W = P_{n-Nyq}\frac{2B_W}{f_S} = \frac{P_{n-Nyq}}{OSR} \quad (1.11)$$

As for the quantization noise, also in the case of sampled noise, an increase of 3 dB of SNR for every doubling of OSR is the benefit obtained by oversampling operations. As a matter of principle, every Nyquist converter can become an oversampled converter, just increasing the sampling frequency and cascading a digital low-pass filter to the ADC. Obviously, the resolution improvement does not come for free. An higher sampling frequency requires an increase of the power consumption. Considering a linear relationship between the sampling frequency and the power consumption (that is often the case), the oversampled converters are less efficient than the Nyquist ones, as it looks evident from the FoM_W.

Oversampled converters usually exploit also additional techniques such as noise shaping, in order to better reject quantization noise in the signal bandwidth. Among the oversampled converter, Delta-Sigma (Δ-Σ) data-converters are the most diffused in different kinds of applications, and they will be explained in details in section 1.4.2 and in the next chapter.

Another inherent advantage of oversampling converter is the reduction of design complexity for anti-aliasing filters. From the Nyquist-Shannon criterion, aliasing is avoided if no signals are present for frequencies higher than the Nyquist frequency $f_S/2$. In a Nyquist converter, that coincides with the signal bandwidth, making the design of a very selective filter very challenging, depending on the SFDR specifications. In an oversampled converter, instead, the selectivity of the filter is relaxed due to the

difference between the signal bandwidth and the sampling frequency, precisely because of the oversampling fashion.

1.4 ADC architectures

There are multiple ways to implement the conversion from the analog to the digital domain. Some converters realize the conversions from voltage to an intermediate quantity (typically frequency) and then to the digital code [7]. In this brief overview on the most popular ADC, we will concentrate our attention only on direct conversion from voltage to digital domain. Several classifications can be made, depending on the different focuses. Here, a simple distinction between converter architectures suitable for high-speed and high-resolution applications is drawn.

1.4.1 High-speed ADCs

High speed data converters are sources of more and more interest over the last decades. Only considering research ADCs from ISSCC 2019, 11 of the 16 presented works show sampling frequency higher than 100 MHz [16]. Among the possible applications as video signal processing and electronic instrumentations, the most appealing ones derived from telecommunications, as high-speed serial data link, where converter throughput as high as tens of GSPS can be required. Flash, SAR and Pipeline converters are the most popular architectures to reach very high sampling frequency, with low-medium resolutions. To improve further the maximum sampling frequency, time-interleaving operations can be employed.

Flash converters

A flash converter exploits the most intuitive principle to convert a sampled voltage. The simplicity of the architecture is also the reason of its speed. In a N bit flash converter (Fig.1.9), the input signal is compared at the same time with $2^N - 1$ reference voltages, by means of the same number of comparators. The output of the comparators has a thermometer-like code, that is then converted into a binary code by means of a decoder. The reference voltages are usually generated from a unique reference voltage, by means of a resistor string with 2^N equal resistances. The conversion time is given by the delay of the comparators plus the delay of the following logic. The impedance of the ladder must be sized to reduce the time constant considering the input parasitic capacitance of the comparators, in order to reduce the effect of charge kickbacks.

Typically, flash converters show resolution from 3 to 8 bits, reaching sampling frequency of several GHz [17]. Due to the exponential dependency of power and area consumption with N, high resolution flash converters are not efficient solutions. This kind of converter is often employed as building block for more complex ADC topologies.

One of the most critical aspect is given by the offset of the comparators, that can lead to non-monotonicity of the converter characteristic. Reducing comparator offset increasing area of MOSFET devices is a possible solution, but it increases also their parasitic capacitances. This issue may lead to relevant distortion. Actually, depending on the value of the input voltage, a different number of comparators will decide '1' or '0'. The unbalancing of the comparator on one side or the other is reflected also as a

different parasitic loading of the input voltage. Together with the position dependency of the resistive ladder impedance, non-linearity of the converter may be introduced.

Comparator metastability limits converter sampling frequency and BER. Metastability is the condition occurring when the differential input of one comparator is close to zero and the comparator is not able to effectuate the correct comparison in the available time. Metastability in flash converters could be particularly detrimental, due to the arise of "sparkles" (wrong bits in the output thermometer code). Proper decoding techniques can limit the spreading of these kind of errors, at the cost of more complexity. Also pre-amplification of the comparators' input signals, averaging and interpolation are useful techniques frequently employed in flash converters [7].

Having different input signals, the comparators will have different decision times. In particular, only two comparators will have to take a critical decision, and they will be the slowest ones, due to the smallest differential input signals. Depending for example on the BER required, more or less time will be allocated for the comparator decisions, in order to increase the probability that the comparators will take the correct decisions.

Area and power consumptions, as well as the parasitic capacitances, increase linearly with the number of comparators, i.e. exponentially with the resolution N. For this reason, flash converters are usually limited to resolution lower than 8 bits. In order to reach higher resolutions, two-step architectures are often employed (Fig.1.9-b). In this topology, the sampled input signal is first converted with a coarse ADC, characterized by a resolution $M < N$. The result of the first conversion is then converted back into the analog domain by means of a DAC with M bits and then subtracted to the input signal. The difference is converted with a fine ADC with $N - M$ bits. The results of the coarse and fine conversions are then combined to obtain the whole conversion with resolution N. With this approach, instead of using a single flash converter with N bit (i.e. $2^N - 1$ comparators), two flash converters with respectively M and M-N bits (i.e. $2^M - 1$ and $2^{N-M} - 1$ comparators). As an example, an 8 bit full-flash converter would require 255 comparators; with a 2-step converter with M=4, only 30 converters are needed. The design complexity is now moved to the DAC, that must be of the same resolution and linearity of the overall converter. The sample-and-hold circuity becomes mandatory, due to the need to hold the signal for the whole conversion time. In order to avoid missing codes due to a mismatch on the full-scale range of the two converters, an over-ranging in the fine ADC is usually implemented (same principle used also for pipeline converters).

An evolution of the two-step converter is the sub-ranging converter [18]. Even in this case, one coarse and one fine stage are used, but no different reference voltages are needed for the two ADCs and no subtraction takes place. A single resistor ladder that generates $2^N - 1$ reference voltage is used, instead of two different ones. After the coarse conversion, where only $2^M - 1$ tap for the first conversion are used, the taps are switched to the $2^{N-M} - 1$ for the fine conversion. The correct position of the taps in the resistor ladder depends on the result of the coarse conversion. Still, the limitations on the performances can be found in the sample-and-hold and in the resistive ladder, which has to guarantee a N-bit linearity and accuracy.

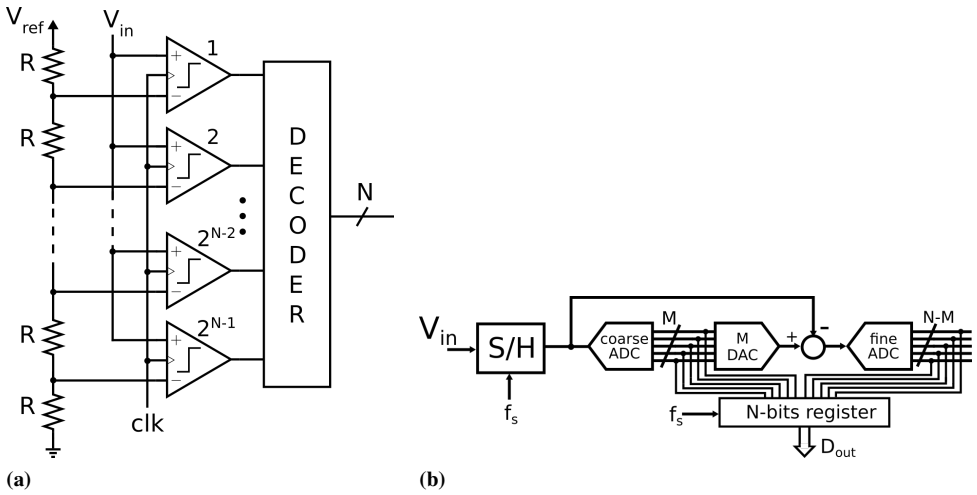

Figure 1.9: *(a) N bit Full-Flash architecture. (b) N bit two-step converter.*

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SAR converters

The Successive Approximation Register (SAR) ADC is based, as the name suggests, in iterative approximations of the sampled input signal by means of a DAC. After each iteration (or bit cycle), a comparison between the input signal and the feedback signal from the DAC establishes one bit of the output code and updates the DAC. After N iterations (where N is the resolution of the converter), the difference between the input and the feedback signals is below the LSB of the converter. Usually, the DAC in a SAR is a capacitive DAC (CDAC), because of the absence of static power consumption. Furthermore, the capacitors employed in the CDAC realize also the sample-and-hold function. Linearity and resolution of the DAC affects directly the performance of the whole converter. Larger capacitors (in order to reduce capacitor mismatch) leads to large area and power consumption, which dissuade form high resolutions implementations.

A single comparator realizes the N decisions in the N clock cycles. After each comparison, the result is stored in a latch, before resetting the comparator for the next bit-cycle. The switching algorithm for the CDAC is implemented in the digital domain, and it is chosen according to power, area and accuracy specifications. The conversion time is equal to N times the bit-cycle, whose duration is made up of the comparator delay, the logic delay and the DAC settling time. As in flash converters, comparator metastability limits the maximum speed and the converter BER.

Due to its great efficiency and its capability to benefit from technology scaling, SAR has been used for medium resolution, high-speed application, often as a single slice of time-interleaving ADC. More details about this kind of converters will be provided in Chapter 4.

Pipeline converters

Pipeline converters exploit even more the working principle of two-step converters. Instead of splitting the whole N bit conversion in two steps, pipeline converters has k steps, as depicted in Fig.1.11-a. Each of the k stages has a lower accuracy ADC with M-bit resolution. The result of the partial conversion is then converted back in the

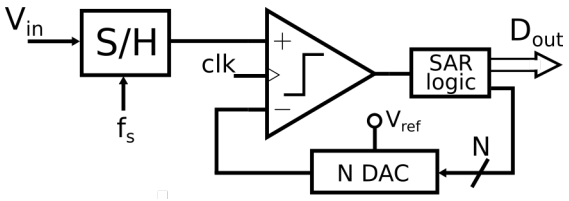

Figure 1.10: *Block diagram of N bit SAR converter.*

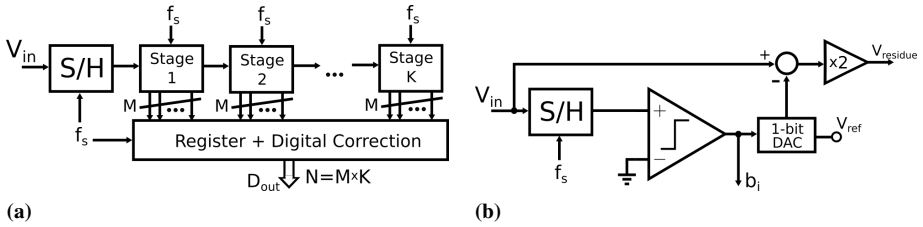

Figure 1.11: *(a) Block diagram of a N bit pipeline converter, with K stages of M bit. (b) 1-bit stage of a pipeline converter.*

analog domain by means of a M bit DAC, and then subtracted to the input signal. The difference is properly amplified by 2^M and then fed to the following stage. Usually all the stages are identical, so that the final resolution of the converter N is equal to the product of the M resolution of each stage and the number of stages K. Fundamentally there is no limitation to the number of bit of each stage; clearly, low resolution ADC and DAC are preferred. The advantage is that the sampling frequency is limited only by the delay of each stage. Once the first stage has generated its M-bit output and the residual signal for the next stage, it is ready to convert the next input voltage sample. Obviously, the latency of a pipeline converter is equal to the conversion time of one stage, times the number of stages.

The same limitations seen for the two-step ADC concerning the DAC resolution and accuracy are also present here. Extending the concept of pipeline and reducing to the minimum the resolution M of each stage (M=1), we can get rid of the limitations on the DACs. 1-bit DACs are, in fact, intrinsically linear, because of the presence of only two output levels. Fig.1.11-b shows the typical 1-bit stage. The weak point of this implementation is given by the amplification stage, that needs to be low-noise and very precise in terms of offset, gain and noise, according to the resolution of the whole converter.

Besides the 1-bit per stage pipeline converter, another popular topology is the so called 1.5 bit per stage pipeline [7]. Instead of a single-bit converter (i.e. a comparator), a 3 levels ADC (employing two comparators and two threshold voltages at $V_{ref}/4$ and $-V_{ref}/4$) is used. The DAC is basically a multiplexer that can select V_{ref}, 0 or $-V_{ref}$ depending on the decisions of the two comparators. 1.5 bit-per-stage pipeline converters implements redundancy and over-ranging techniques, relaxing the requirements on the amplification stage. Pipeline converters can reach easily throughput of 100-1000 MSPS and 9-10 bit of ENOB, as in [19].

Time-Interleaved ADC

A common technique to increment the converter sampling frequency is by time-interleaving (TI) several identical ADCs, called slices. The idea is to subsample the input signal at a frequency f_S/K and to use K slices (with resolution N) to digitize the subsampled signals (Fig.1.12). The overall converter has a resolution N and a sampling frequency f_S.

Whatever converter architecture can be matched with time-interleaving operations. Typically, each slice is either a Flash, or a SAR or a Pipeline converter, to exploit their already high speed performances. The FoM_W of a time-interleaved ADC is, ideally, the same as the one of each single slice. TI allows us to obtain very high-speed frequency ADCs without pushing over its intrinsic limitations a single-channel ADC, losing in terms of power efficiency.

Ideally, no limitation on the number of channels is present, a part from the maximum clock frequency allowed. Actually, a large number of slices and a high sampling frequency affect heavily the design complexity and the requirements of each single slice. A physical limit on the maximum sampling frequency, from which the subsampling clocks are derived, is given by time jitter. Furthermore, offset, gain, bandwidth mismatches among the different channels reduces the whole converter performances. Time skews among the different channels introduces harmonic distortions as well. A complete analysis about the effects of each error sources to the time-interleaved ADC can be found in [12]. Foreground or background calibration techniques for each slice are mandatory in order to reduce these kinds of errors, increasing the area and power consumption. The highest-speed ADCs present in the literature implements time-interleaving operations, typically with SAR architecture for the single slice (due to its great power efficiency) [20–22].

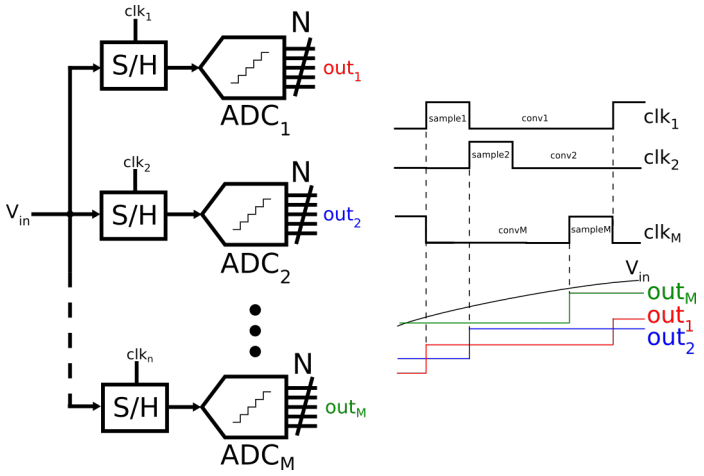

Figure 1.12: *Block diagram of a N bit time-interleaved ADC with N channels. On the right, the clock timing diagrams and the output waveforms of each slice are shown.*

1.4.2 High-resolution ADCs

In the last decade, IOT has leaded the research and the market trends of embedded systems, automation, low-power wireless communications and many other fields of in-

formation engineering. [23] foresaw the presence of 30 billion devices by the next year, with an overall market value of around $ 7 trillion. Among the countless applications of IOT, ranging from industrial applications (smart agricolture and energy management) to environmental monitoring, passing by consumer applications (as smart home), healthcare has been one of the most attractive and important for the improvement of everyday life. [24] describes the importance of wearable devices and the challenges behind these complex electronic systems, from the design of the sensor to the readout interface.

In all these fields, electronic data acquisition systems play a key role for the fulfilment of competitive performances. High-resolution and high-accuracy ADCs are mandatory in order to achieve the targetted specifications, especially when the useful information acquired from the sensors are crucial in terms of human healthcare or environmental sensing. Even in high performance electronic equipment, medium-high resolution digitizer for signal acquisition up to 1 MHz or very-high resolution digitizer for dc measurements are employed, as in [25]. In this design space, the converter architectures able to reach the highest resolutions are algorithmic converters, linear approximation converters and Δ-Σ converters. SAR ADCs are also candidates to reach high signal-to-noise ratio, limited only by the DAC linearity. Design techniques as Dynamic Element Matching (DEM), off-line calibration procedures or ad hoc manufacturing process as laser trimming may extend (not for free) SAR applications.

Algorithmic Converters

Differently from SAR converters, where the voltage generated iteratively by the DAC approximates the sampled voltage better and better, in an algorithm converter the sampled signal is only compared with V_{ref}. Depending on the result of the comparisons, the charge proportional to the input voltage stored in the sampling capacitor is manipulated. The converter block diagram is shown in Fig.1.13, and it looks very similar to the 1-bit stage of pipeline converter of Fig.1.11-b. However, the residual voltage $V_{residue}$ generated at the end of each cycle is not processed by the following stage but from the same hardware. Then, the converter latency is the same as in pipeline converters, but also the throughput is inversely proportional to the resolution. As in pipeline converters, an accurate value of the gain of the amplification stage is pivotal. This gain is usually implemented with a capacitive ratio in a Switched-Capacitor (SC) circuit. SC circuits allows the straightforward execution of offset cancellation techniques as Correlated Double Sampling (CDS) [26], avoiding detrimental effects of the offset. However, offset or gain error arising from charge injection issues must be controlled as much as possible. Typically, a maximum accuracy of 10-12 bits, limited by device mismatches, is feasible.

Linear Approximation Converters

Linear approximation converter can be implemented in several ways, starting from the Wilkinson converter, proposed for the first time around 1950 [7]. After the sampling of the input voltage on a capacitor, a very accurate reference current is used to discharge it. A comparator connected to the capacitor periodically compares its voltage with a certain threshold, and depending on the result of the comparison, it increments a digital counter. It is worth noting how the converter resolution will depend on the ratio

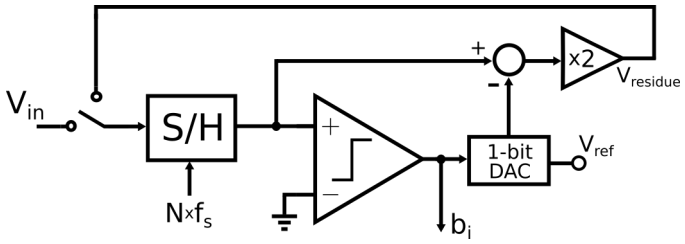

Figure 1.13: *Block diagram of an algorithmic converter.*

between the comparator clock (and then the counter updating) and the slope of the discharging voltage. When high resolutions are targeted, only very low sampling rate can be achieved. This is a typical characteristic shared by all the linear approximation converters. In the Wilkinson converter, an offset of the comparator is added to the signal. Considering the offset variations with the input common mode (i.e. with the input signal), also harmonic distortion will be introduced.

A similar operating principle is exploited in single-slope ADCs [27]. A voltage ramp is periodically compared with the input sampled voltage. Knowing the slope of the ramp and the instant when the comparator changes decision (i.e. when the ramp becomes higher than the input voltage), the input voltage can be digitized. The ramp generator is typically a Miller integrator, with the reference voltage as input. Very precise values of the components are required. The resolution of the converter is a function of the clock frequency of the comparator, in order to detect with less uncertainty the zero crossing of the comparator differential input. As for the Wilkinson converter, comparator offset affects converter performances, as well as integrator non-idealities.

The dual-slope ADC overcomes some of the limitations of the previous converters. As depicted in Fig.1.14, first a ramp with a slope proportional to the input voltage is generated, starting from a zero output voltage. Then, switching the integrator input from V_{in} to $-V_{ref}$, a ramp with the slope proportional to $-V_{ref}$ is generated. When there will be the zero crossing of the decreasing ramp, the comparator will detect it, changing decision. In this case, the requirements on the integrator components, as well as for comparator offset, are less strict. Furthermore, there is no need of linear capacitor, since the same is used for both charging and discharging. An interesting feature which makes this kind of converters very popular, is the possibility to reject interferences at known frequency. 50 Hz disturbs due to crosstalk with the power supply are easily cancelled, setting the proper conversion period. The resolution range for this kind of converters is typically from 12 to 16 bit.

Delta-Sigma ADC

As already mentioned in paragraph 1.3, oversampling allows the reduction of quantization noise power in the signal bandwidth, as well as thermal noise power of the converter. The resolution improvement due to the OSR increasing, however, is not sufficiently worthy, often compared to the increasing design complexity due to the higher sampling speed.

Delta-Sigma converters [28] show an intrinsic filtering function, called noise-shaping, which allows a further decreasing of the in-bandwidth quantization noise, moving its power to highest frequencies, where it will be filtered out by the digital low-pass filter

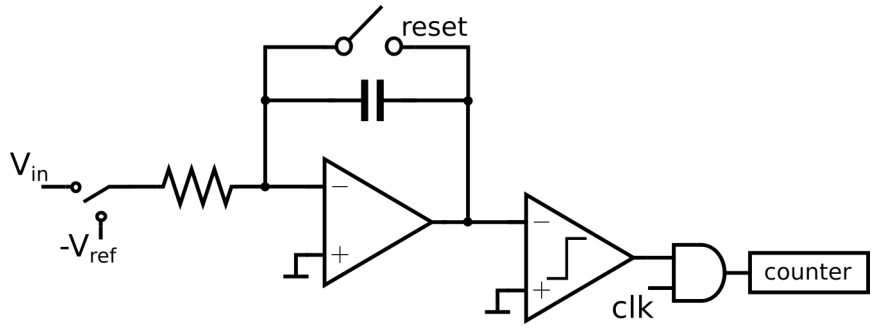

Figure 1.14: *Block diagram of a dual-slope ADC.*

cascaded to the modulator (as shown in Fig.1.15). The operating principle is mainly the one of a negative feedback architecture, where a loop filter provides a very high dc gain, before the effective injection of the quantization noise. The converter employed inside the modulator introduces a certain quantization error (related to its resolution N_0) that will be shaped approximately by the inverse of the loop filter transfer function, i.e. heavily attenuated in the signal bandwidth. The feedback is closed by means of a DAC, with a resolution equal to the one of the ADC. The bitstream at the output of the modulator, with a throughput f_S (also called oversampling frequency), is then filtered and decimated by a digital low-pass filter. The output throughput is then f_S/OSR, i.e. the Nyquist rate of the converter. At the filter output, the resolution N will be higher than the resolution N_0, thanks to the noise shaping and the low-pass filtering function. The resolution increasing can be generally expressed as $kOSR$, where k (higher than one) will depend on the modulator topology.

Several modulator architectures are present in the literature, each with its advantages and drawbacks. In the next chapter, several topologies will be investigated with more details. Typically, the loop filter is realized with the cascade of integrator stages, where the number of stages represent the order of the Δ-Σ modulator, related with the factor k of the resolution improvement just mentioned.

As for pipeline converters, also in Δ-Σ converters is often preferred the employment of a single-bit ADC (i.e. a comparator) inside the modulator. In single-bit modulators, the feedback path will be generated by means of a single bit DAC (a simple matrix of switches), that is intrinsically linear. Then, the linearity of the whole Δ-Σ converter is not limited by the employed DAC, as for example in SAR converters, where maximum resolution of 10-12 bits are usually achieved. However, multi-bit modulators are feasible solutions when high-resolution are targeted and high OSR are not allowed, as for intermediate-frequency conversions in radio-communications or direct conversions for software-defined radio [29].

1.5 Trends of Analog-to-Digital Converters

As already said, the world of Analog-to-Digital Converters is very wide and it can not be explored exhaustively in this introductive chapter. In this section, a quick insight on the trends of the ADCs of the last years will be provided, investigating both scientific works and commercial products.

[16] reports published works from ISSCC and VLSI international conferences (from

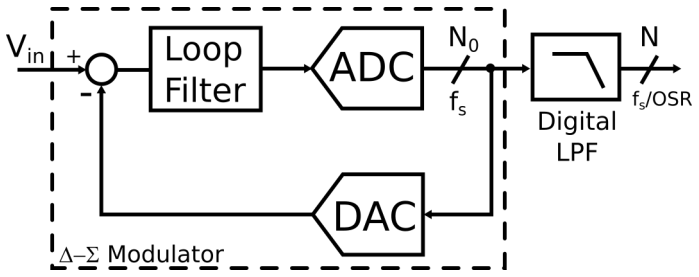

Figure 1.15: *Block diagram of a Δ-Σ ADC.*

1997 to 2019), with a summary of their performances in terms of power, resolution and sampling frequency. They have also been classified according to the converter architecture. In order to easily compare different converters, designed with different specifications, some parameters as the energy per Nyquist sample, the FoM_W and the Schreier Figure of Merit (FoM_S) are reported. The energy per Nyquist sample is defined as the ratio between the dissipated power P and Nyquist rate f_{Nyq}. For a certain resolution, it is possible to identify the lowest-energy designs, recognizing the most efficient architectures for the different design spaces. The figures of merit take into account, at the same time, power dissipation, maximum speed (related to the Nyquist rate) and resolution. Two figure-of-merits are typically used: FoM_W and FoM_S. We have already defined FoM_W in 1.5. It is conventionally used for low-resolution data converters. FoM_S, also called "thermal FoM", is used instead for high-resolution converters, where typically the signal-to-noise ratio is limited by thermal noise.

Fig.1.16 shows the bandwidth-SINAD plot, highlighting the limits dictated by jitter on the sampling pulse. Targeting both high resolution and high speed, jitter lower than 1 ps-rms is required, increasing the power consumption and the design complexity for the clock generation. Figures 1.17 and 1.18 show the trends of the two different figure-of-merit for scientific ADCs, designed for Nyquist rate from 100 Hz to 100 GHz. The envelope curve has been evaluated considering the best 5 data points in terms of FoM, and considering the 10 dB/dec rise (or drop) due to the quadratically growth of power with speed in that region, as argued in [30].

From the data collected in [16], it is worth plotting the energy plot and the Figure-Of-Merit plot for high-speed (Fig.1.19) and high-resolution (Fig.1.20) ADCs, reporting the data points classified for converter architectures.

Flash and 2-steps converters are typically used for Nyquist rate higher than 1 GHz and low resolutions, achieving not optimal energy efficiency. SAR and TI SAR are the most efficient solutions for very high-speed applications, with effective resolutions lower than 8-9 bits. Pipeline and continuous-time (CT) Δ-Σ converters can reach resolutions higher than 10 bits (for sampling frequency lower than 1 GHz), with the best energy efficiencies. Some of the best data-points in terms of FoM_W[3] are reached by those kinds of converters.

For high-resolution converters (ENOB higher than 12 bit), Δ-Σ converters lead the design space, with CT architectures that show the best FoM_S, typically for higher Nyquist frequencies. Also SAR architectures are competitive due to their great energy efficiency, typically limited to 7-8 bit of effective resolution. Algorithmic and linear

[3] FoM_W has been used, considering the low SINAD values in play.

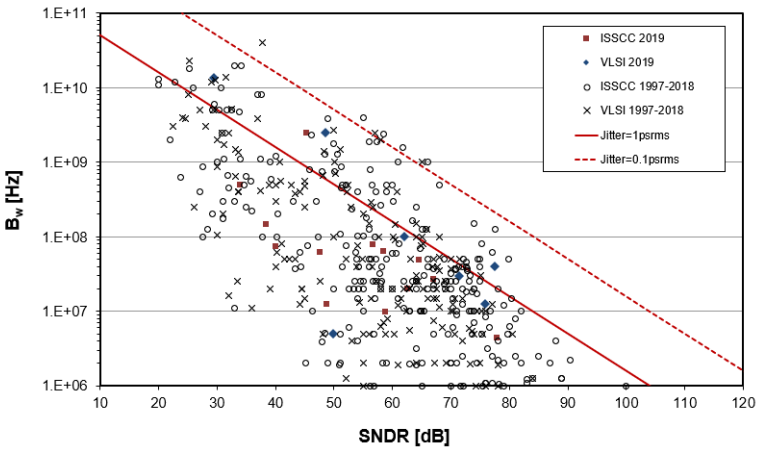

Figure 1.16: *Plot SNDR-B_W of the most recent ADCs present in the literature, considering also the limits due to jitter. Graph taken from [16]*

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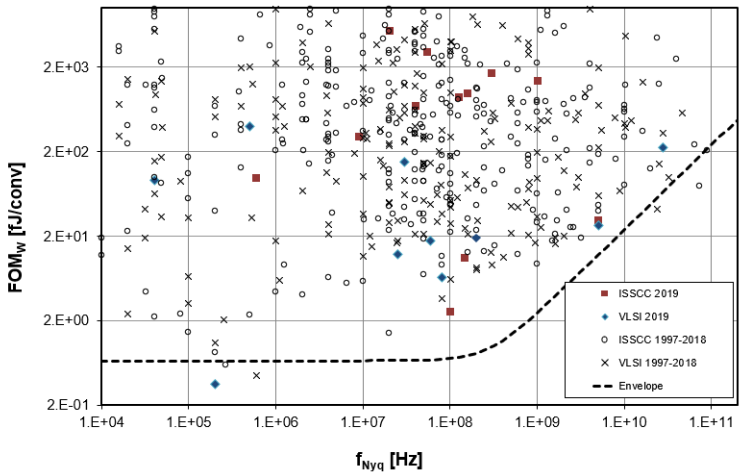


Figure 1.17: *Plot f_{Nyq}-FoM_W of the most recent ADCs present in the literature. Graph taken from [16].*

approximation converters are not present among the best ADCs of the last two decades, due to their low energy efficiency and very low signal bandwidth. However, some commercial ADCs exploit those kind of architectures due to their stable and robust performances.

Interesting considerations can be made also about the migration of ADC implementations to newer technologies and the consequent supply voltage scaling [31]. Traditionally, a so called "scaling gap" has always been present between analog/mixed and digital integrated circuits. While digital design has always obtained benefits from aggressive technology scaling, analog circuit designers have to face new problems during the migration towards new technology nodes. Non-idealities of transistor devices such as short-channel effect, gate leakage and gain degradation are only some of the main drawbacks. Also increased mismatch between devices on the same chip or larger process variations among different dies have reduced the robustness of analog designs.

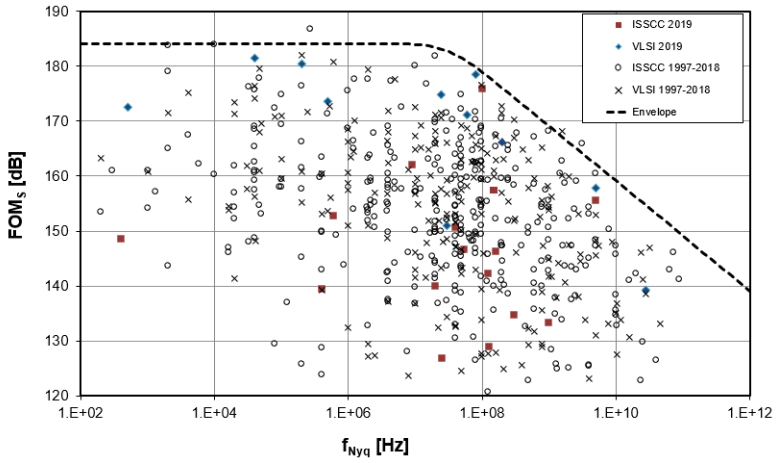


Figure 1.18: *Plot f_{Nyq}-FoM_S of the most recent ADCs present in the literature. Graph taken from [16].*

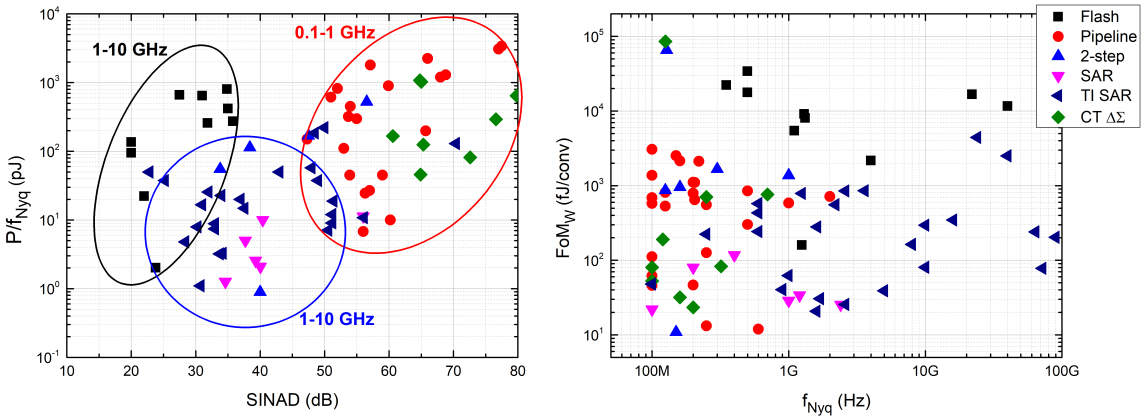


Figure 1.19: *a) Energy plot of high-frequency ADCs from ISSCC 1997-2019, grouped for different architectures. b) FoM_W plot of high-frequency ADCs from ISSCC 1997-2019, grouped for different architectures.*

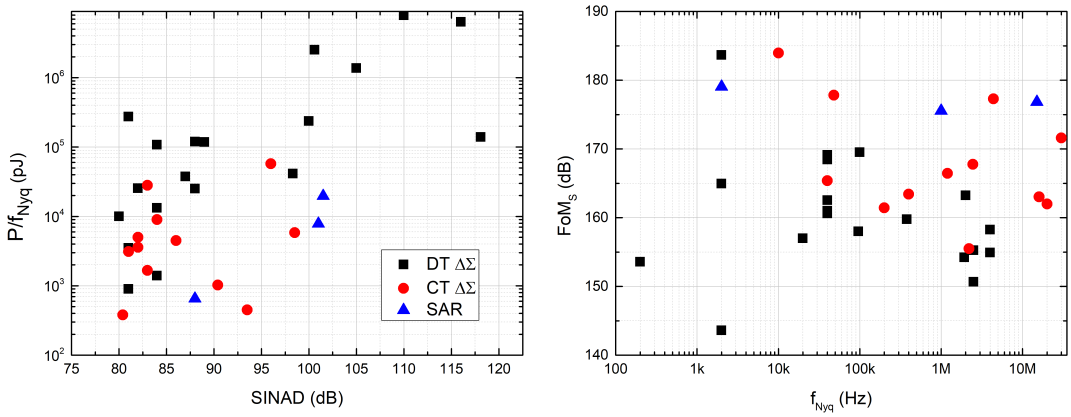


Figure 1.20: *a) Energy plot of high-resolution ADCs from ISSCC 1997-2019, grouped for different architectures. b) FoM_S plot of high-resolution ADCs from ISSCC 1997-2019, grouped for different architectures.*

However, the increasing popularity of digital-centric SoCs has leaded to the scaling of several analog/mixed-signal circuits. The presence of the ADCs on the same chip with the digital core is often unavoidable: this has led to a fast process scaling also of the ADCs, compared to other analog circuits. Together with process scaling, supply voltage decreasing further enhances ADC design complexity. From 350 nm to 10 nm technology node, the core supply voltage has scaled from 3.3 V to 0.7 V, without a proportional scaling of MOSFET threshold voltage (from about 0.5 V to 0.28 V). Concerning scientific ADCs designed for low-voltage or ultra-low voltage applications, we have been witnessed of a halving of supply voltage every 5 years in the last three decades, reaching supply voltage as low as 0.2 V [32]. Over the last decade, several ADCs capable of working with supply voltages in the range of 0.2 V - 0.5 V have been presented, mainly motivated by emerging applications as IOT, wireless sensor networks and wearable electronics. However, it is tough to imagine a further decreasing of V_{DD} for low-voltage ADC; the trends are moving towards the improvements of power consumption, speed and resolution. However, it is worth noting how the performance improvements of regular voltage ADC is increasing with a rate of only 1dB/year [33].

A brief overview on the most performant commercial ADCs present on the market will end the general framework about the actual state-of-the-art of Analog-to-Digital Converters. Great ICs design company as Analog Devices, Maxim Integrated, Texas Instruments, etc. offer multiple monolithic ADCs for different solutions.

The highest speed ADC of Analog Devices is HMCAD5831, a full-flash converter with 20 GHz of input bandwidth and 3 bit of resolution. AD9213 is a 12-bit, 6 GSPS/10.25 GSPS ADC with a 6.5 GHz input bandwidth, which exploits a time-interleaving pipeline architecture. ADC12DJ5200RF from Texas Instruments exploits a time-interleaving folding interpolating architecture (a modification of the two-step flash architecture) to reach 12 bits at a maximum sampling frequency of 10 GHz. Extrapolating some general information, folding interpolating and pipeline architectures are the most used in high-speed monolithic ADCs. For sampling rates lower than 100 MSPS, also SAR and two-step architectures have been adopted. The power consumption is on the order of several watts, due to the very high targeted sampling frequency. "Low power" high-speed ICs do not dissipate less than tens of mW.

Looking at high-resolution monolithic ADCs, it is very easy to identify the most employed architectures. Δ-Σ and SAR are the (almost) undisputed leaders of the market. Analog Devices uses both architectures for targeted (nominal) resolutions from 32 to 16 bits. For lower resolutions, also pipeline architectures start to be used, when higher sampling frequency are needed. LTC25xx and AD7177, respectively a SAR with oversampling and digital filter and a Δ-Σ converter, show the highest resolutions (24.2 bit and 24.6 bit, respectively, with output rate lower than 100 SPS). A similar trend is present looking at the portfolio of Maxim Integrated. SAR converters are present only for resolution lower than 20 bit; for higher effective resolutions, only Δ-Σ converters are employed. Also linear approximation converters as multi-slope converters MAX132 and MAX135 are sold, with resolutions lower than 18 bit. Looking at Texas Instruments ICs, the converter leader for very high-resolution is the Δ-Σ. From 32 bit to 20 bit, no other architecture is present. SAR converters and pipeline converters can be found with resolutions lower than 20 bit and 12 bit, respectively. Typical power consumptions of these ICs are from tens of mW to few hundreds of mW (depending

also on the number of channels in the same package). Depending on the settings, lower power consumptions can be obtained, at the cost of lower sampling frequency and/or resolution. Low-power ICs are AD7091R-5 of Analog Devices and ADS112C04 of Texas Instruments, respectively a SAR architecture for 12 bit resolution dissipating 90 µW and a Δ-Σ modulator for 14 bit resolution dissipating 315 µW, but with a very low output rate (20 SPS).

Commercial microcontrollers often contain embedded analog-to-digital converters. Looking at the portfolio of MCU sold by Analog Devices, almost the totality employs Δ-Σ converters, exploiting their programmability and further digital filtering functions to extend their performances. Low-power microcontroller (minimum Vdd of 1.8 V and a maximum current consumption of 5 mA) ADuCM362 embeds dual 24-bit ADCs (with ENOB of 21 bit with enabled chopper and an output update rate of 3.53 Hz).[4] [34] explains the CHS technique implemented for the Δ-Σ ADCs. It realizes offset cancellation of the whole chain, modulating the input signal before the Programmable Gain Amplifier (PGA) and demodulating the bitstream after the Δ-Σ modulator. The chopper frequency is a fraction of the update rate and it needs further digital averaging after the $sinc^3$ filter. Further details about the operating principle of this CHS technique are given in paragraph 2.3.4. ADSP-CM40X implements two 16-bit SAR ADCs with 13 bits of effective resolutions. Also for embedded ADCs in MCUs, Δ-Σ and SAR converters are the most popular choices of several integrated device manufacturer companies.

1.6 Discussion and conclusion

In this first chapter, a brief overview about the main characteristics and applications of analog-to-digital converters is presented. After the definitions of the fundamental parameters describing the dynamic and static behaviour of the ADCs, a first classification of the converters on the basis of the main two features (speed and resolution) is given, focusing on the different architectures for the target requirements. At the end, a survey on the ADC trends of the last years, including both research works and commercial products, pulled the threads of this introduction, providing some general considerations about the actual limitations of this kind of data converters. In the next chapters, the design of three different analog-to-digital converters for highly-specific applications will be provided, focusing on the novel techniques which allowed the fulfilment of the different requirements. All of them have been evaluated by means of the static and dynamic parameters described in this chapter, through electrical simulations and/or measurements on silicon prototypes.

[4] ENOB is evaluated from the dynamic range, considering the peak-to-peak noise voltage.

CHAPTER 2

Design of high-resolution and high-accuracy Delta-Sigma for sensor applications

2.1 Introduction

Delta-Sigma data converters are the most diffused oversampled data converter and they are employed in many different applications, from audio systems to RF receivers. The appealing features of this kind of converters are the noise shaping function and the relaxed requirements on both the anti-alias filter before the converter and on the passive element matching, even targeting high resolution and high linearity. As briefly described in the previous chapter, noise shaping reduces the in-band quantization noise power, leading to an increase of resolution with respect of the low-resolution ADC employed inside the modulator. To achieve this result, a digital decimating low-pass filter is required. Furthermore, it is possible to exploit its presence also to reject additional interferences at known frequencies, as artefacts introduced by CHopper-Stabilization (CHS) technique [26] or supply line cross-talk interferences.

Several modulator topologies are present in the literature and a complete dissertation on the whole design space would not be possible here. In this chapter, a brief introduction on the basic theory of Δ-Σ converters is provided, focusing on the most interesting aspects for high-resolution and high-accuracy applications, such as low frequency signal acquisition for environmental sensor interfacing. Typical signal bandwidth from dc up to few kHz are distinctive of pressure and inertial sensors, thermal sensors, or sensors based on thermal principles, bio-sensors, etc. Commercial sensor interfaces with digital output interface (typically I2C and/or SPI) often embeds Δ-Σ converters; some examples are reported below. Pressure sensor interface FXPS7115D4 for automotive application by NXP semiconductor employs a second order Δ-Σ modulator with 1 MHz of sampling frequency and a digital $sinc^3$ decimation filter. Temperature sensor

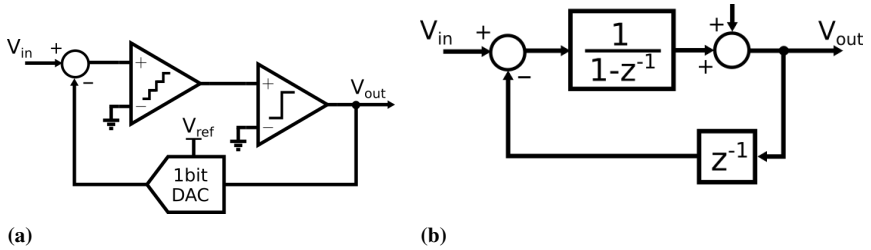


Figure 2.1: *(a) 1st order, single-bit quantizer, discrete-time Δ-Σ Modulator (b) Linearised model of the modulator.*

PCT2075 by NXP embeds a 11 bit Δ-Σ converter. AIS1120SX MEMS automotive acceleration sensor of STMicroelectronics embeds a 2nd order delta-sigma converter, as well as the digital temperature sensor and thermal watchdog STCN75 of STMicroelectronics. MSP430 polyphase IC of Texas Instruments also embeds multiple independent 24-Bit Sigma-Delta ADCs. AS89010 current-to-digital converter embeds 4-channel Δ-Σ ADCs for precise conversion of photo currents for optical sensors. These are only few examples but already quite indicative of the popularity of this kind of converters for high-resolution, low-speed applications. Another important commercial application of Δ-Σ converters is in microcontroller, as MCU (microcontroller units) for multichannel sensor monitoring as [34].

In this chapter, the design of a 2^{nd} order, discrete-time Δ-Σ ADC is fully-described, starting from the high-level description and ending with the transistor-level implementation. The converter has been optimized for digitizing dc and low frequency signals, with high resolution and high accuracy. Two critical issues will be analysed in details: (i) offset and flicker noise, (ii) settling time errors in discrete-time (DT) integrators. Two original solutions to the above mentioned problems will be described in details. Measurements on a prototype designed in UMC 0.18 μm process will provide better insights.

2.2 Overview of Δ-Σ Converters

2.2.1 1st order Δ-Σ Modulator

The simplest implementation of a Δ-Σ is the 1st order, single-bit modulator depicted in Fig.2.1-a. Only a discrete-time (DT) integrator, a single-bit ADC (i.e. a comparator) and a single-bit DAC (a simple switch demultiplexer, or the cascade of two inverters) are employed. Even if it is not very diffused in practical implementations due to its several limitations, it is very instructive to analyse the operating principle of Δ-Σ modulators. Higher order or multi-bit topologies share most of the features already present in this modulator.

In order to study this circuit, the linearised model shown in Fig.2.1-b can be drawn, replacing the discrete-time integrator with its transfer function in the z-domain, while the quantizer is replaced only by its injected quantization noise and the DAC by a unit-cycle delay.

Two important transfer functions can be defined for a Δ-Σ modulator: the Signal Transfer Function (STF) and the Noise Transfer Function (NTF). They are defined,

respectively, as the ratio between the output and the input of the modulator, and the output and the quantization noise.

$$STF(z) = \frac{V_{out}(z)}{V_{in}(z)} = 1 \tag{2.1}$$

$$NTF(z) = \frac{V_{out}(z)}{V_{n-q}(z)} = 1 - z^{-1} \tag{2.2}$$

The STF of a first order modulator is constant and equal to one[1]. The NTF, instead, is the z-transform of an ideal differentiator (zero placed in $z = 1$), which, in the frequency domain, means a zero in the origin (Fig.2.2).

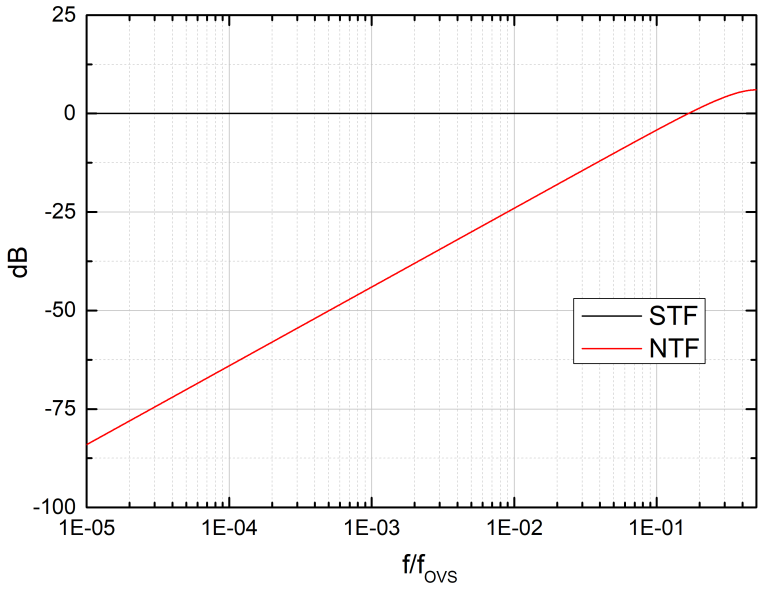


Figure 2.2: *STF and NTF of a 1st order* Δ-Σ

The quantization noise of the quantizer $v_{n\text{-}q}$, with a power spectral density equal to $2V_{FS}^2/(12f_s)$, is shaped by the NTF and then is low-pass filtered by the digital filter cascaded to the modulator. Considering an ideal low-pass filter with cut-off frequency equal to the signal bandwidth B_W, the SNR at the output of the converter (i.e. after the filter) is:

$$SNR = \frac{P_{sig}}{P_{q-n_{out}}} = \frac{P_{sig}}{P_{q_n}\pi^2/(3OSR^3)} \tag{2.3}$$

Where P_{q-n} is the quantization noise power of the converter employed inside the modulator. As it looks evident from 2.3, every doubling of the OSR, the SNR increases of a factor 9 dB (=1.5 bits of resolution improvement). Compared to the benefit of just oversampling (described in paragraph 1.3), noise shaping of a 1st order Δ-Σ modulator introduces an extra bit advantage, for every doubling of OSR. So far, no hypothesis on

[1]STF=1 is the result of using a delay-less integrator. Typically, switched-capacitor integrator as the one analysed in appendix A are delaying-integrator. Employing delaying-integrator and removing the unit-cycle delay in the feedback path, the STF results in z^{-1}, which has flat frequency response with magnitude equal to one. No modifications, ideally, affect the NTF

the quantizer resolution has been made. Theoretically, employing ADC with resolutions higher than 1 bit, has the only effect to reduce the quantization noise power of v_{n-q} and then to reach an higher resolution of the Δ-Σ converter.

From the analysis of the linearised model of Fig.2.1-b, it looks evident the stability of the modulator. Validity of the linearised model is guaranteed under the assumption of large and random variations of the output of the integrator, for which the quantizer cannot be modelled simply with the insertion of white noise. Concerning dc input signals, it is possible to prove that the modulator stability is guaranteed if the input signal is bounded by 1 (i.e. lower than the full-scale).

A first drawback of one-bit modulators is related to the quantizer (i.e. the comparator) gain, which is not straightforwardly defined. Replacing the quantizer in the linearised model with a constant gain (1 in Fig.2.1-b) can lead to not negligible differences compared to the behaviour of the actual modulator. Unfortunately, the gain of the quantizer is a function of the statistics of its input (the output of the integrator), which is in turn a function of the input of the converter. Variation of the quantizer gain due to different input statistics may also cause modulator instabilities, especially for higher-order modulators [28]. In multi-bit modulators, the quantizer gain is well defined and not dependent from the input signal; it is a typical solution in high-order modulator, where stability issues are particularly relevant.

Another peculiarity of Δ-Σ modulators with dc input signals is the presence of the so called idle tones (or limit cycles). Considering, for example, an input dc signal of half of the full-scale, the output bitstream will be made up by the repetitions of a periodical sequence, e.g. (1,1,-1,1). The mean value of this code is indeed 0.5. On top of this dc value, an additional tone at $f_s/4$ will be present. Having an OSR usually higher than a few tens, that tone will be effectively rejected. The problem, has can be easily foreseen, is that the frequency of this idle tone is related to the value of the dc signal. In particular, under certain conditions of dc input amplitude [28], the frequency of the idle tone may fall in the signal bandwidth, resulting in a degradation of the SNR. It is proven that higher order modulators are less prone to idle tone generations.

The electrical implementation of the ideal DT integrator introduces several drawbacks. Usually, the DT integrator is realized with a SC integrator, employing an operational amplifier with finite dc gain A_0. This will cause a saturation of the integrator gain at low frequency and the shift of the pole to a non-zero frequency. The z-transfer function of the DT integrator can be expressed as:

$$H(z) = \frac{z^{-1}}{1 - pz^{-1}} \tag{2.4}$$

where p is $(1 - A^{-1})$ [2]. The lower is the integrator dc gain, the higher is the pole frequency of the "leaky" integrator. It is possible to evaluate the NTF of the first order modulator, considering the integrator finite dc gain:

$$NTF(z) = 1 - pz^{-1} \tag{2.5}$$

The zero is not in $z = 1$ any more, but in $z = p$. The noise transfer function, then, does not goes to 0 for frequency close to zero, but it will saturate at a value equal to $1/A$.

[2] This is a generic formulation. Actually, p will depend also on the capacitive ratio in the SC integrator, as described in appendix A

The increase of quantization noise power, compared to the ideal case of $A \to +\infty$, will be:

$$P_{q-n-fg} = \left(1 + \frac{3OSR^2}{A^2\pi^2}\right) P_{q_n} \tag{2.6}$$

With finite dc gain equal to the OSR, an increase of quantization noise power of 1.15 dB is present. With traditional amplifier topology employed in switched-capacitor circuits, this constraint is not a problem. Issues can arise in ultra-low voltage design, where high-dc gain amplifier are difficult to realize. In that case, the increase of quantization noise could effectively limit the resolution of the converter. Moreover, this problem could be detrimental if related also with low linearity of the amplifier gain [35]. In the next chapter, more details will be provided.

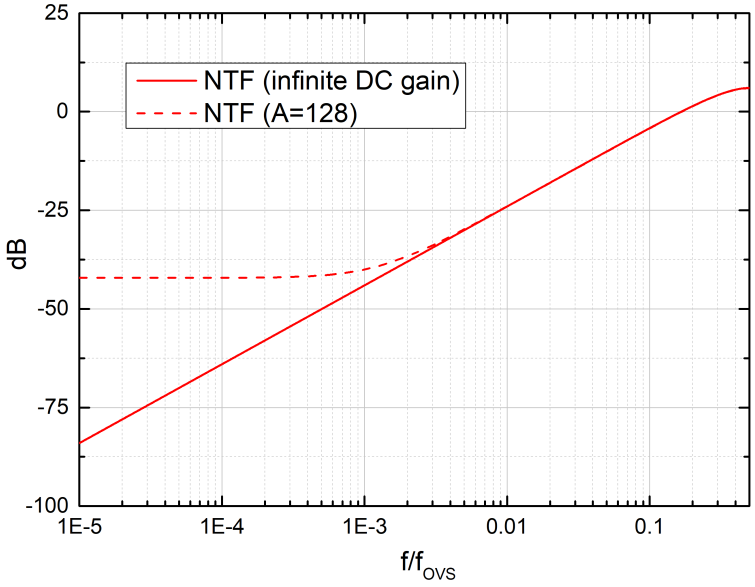


Figure 2.3: *Comparison of NTF of a 1st order Δ-Σ Modulator, with infinite DC gain and with finite dc gain A_0=128*

Another critical aspect due to the finite dc gain of the integrator is the presence of dead-zones in the converter response. Dead-zones are ranges of the input signal for which the modulator does not recognize input variations and the output bit-stream does not change. The largest dead-zone is located around zero input voltage; smaller dead-zones are present around all the rational values of the input dc signal [28]. Dead-zones are inversely proportional to the finite gain of the integrator. Typically, a dc gain higher than 2^N, where N is the resolution of the Δ-Σ converter, will provide dead-zones smaller than the LSB.

In order to increase the resolution of the converter without increasing the OSR, an ADC with a larger resolution can be employed inside the modulator. The multi-bit modulator, then, will have a higher resolution due to the lower quantization noise injected by the ADC. However, a DAC with the same resolution of the ADC must be present in the feedback path. The main problem related to multi-bit modulator is the linearity of the DAC. A 1-bit DAC, in fact, is intrinsically linear, because of the presence of only two output levels. Already for a 2-bit DAC, the same advantage is not present

any more. A non-linearity in the feedback path, as in every feedback architecture, is exactly reflected as a non-linearity of the whole circuit. In multi-bit modulators, then, the capability of reaching high resolutions without requiring elevate matching properties to the DAC is lost. However, multi-bit modulators are still employed when high signal bandwidths are required and the OSR can not be as large as the target resolution would require for a single-bit modulator. In these implementations, Dynamic Element Matching (DEM) techniques reduce mismatch effects in the DAC, shifting the non-linearities outside the signal bandwidth [36]. All these techniques come with an increase of the circuital complexity, spoiling partially one of the most appealing benefit of Δ-Σ converters.

A digital low-pass filter is mandatory in order to achieve the improved SNR enabled by oversampling and noise shaping techniques. The output bitstream, with a throughput of f_S, must be decimated, reducing the throughput to the Nyquist rate. The filter response should be flat in the signal bandwidth and reject the quantization noise outside. Furthermore, a flat group delay is usually recommended. For this reason, a Finite-Impulse Response (FIR) filter is generally employed. Among the possible filter topologies, one of the most diffuse and hardware efficient is the sinc filter. With a single-bit quantizer, the implementation of a sinc filter is extremely simple: it is basically an accumulator, downsampled and reset at the Nyquist rate. A simple sinc filter is not sufficiently selective and would cause a not negligible resolution loss compared to the case in equation 2.3. Usually, for a first order modulator, a sinc^2 filter represents a good trade-off between hardware complexity and output SNR. A small drop of the filter gain is present already in the signal bandwidth, but it can be compensated later in a following digital stage.

2.2.2 2nd order Δ-Σ Modulator

As already explained in the previous section, the first order modulator shows some limitations in terms of rejection of in-bandwidth quantization noise and high dependency from integrator finite dc gain. In order to increase the effectiveness of noise shaping, a second integrator can be added in the loop filter. Replacing the quantizer present in Fig.2.1 with a first order modulator, a second order Δ-Σ modulator is obtained (Fig.2.4). In the same way described in the previous paragraph, a linearised model of the circuit can be used to evaluate the STF and the NTF:

$$STF(z) = \frac{V_{out}(z)}{V_{in}(z)} = 1 \tag{2.7}$$

$$NTF(z) = \frac{V_{out}(z)}{V_{n-q}(z)} = (1 - z^{-1})^2 \tag{2.8}$$

The STF is the same as for the first order modulator. NTF shows two zeros in $z = 1$, which means a 40 dB/dec low-pass filtering, doubled compared to the first order modulator, as shown in Fig.2.5. Considering an ideal low-pass filter with cut-off frequency B_W, the SNR results:

$$SNR = \frac{P_{sig}}{P_{q-n_{out}}} = \frac{P_{sig}}{P_{q-n}\pi^4/(5OSR^5)} \tag{2.9}$$

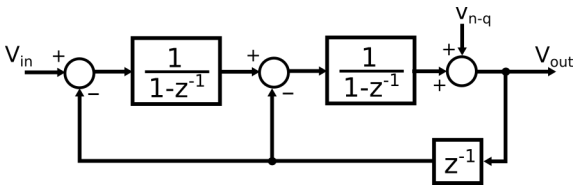


Figure 2.4: *Linearised model of a 2^{nd} order Δ-Σ modulator.*

From 2.9, it looks clear the enhancement in terms of SNR (actually, SQNR) compared to the first order modulator. For example, with an OSR of 256, the increment of resolution due to noise shaping and oversampling in a first order modulator is around 11 bit, while for a second order modulator with the same OSR is almost 18 bit. This is already a good reason to move from the first to the second order modulator. Other improvements are also present and will be here explained.

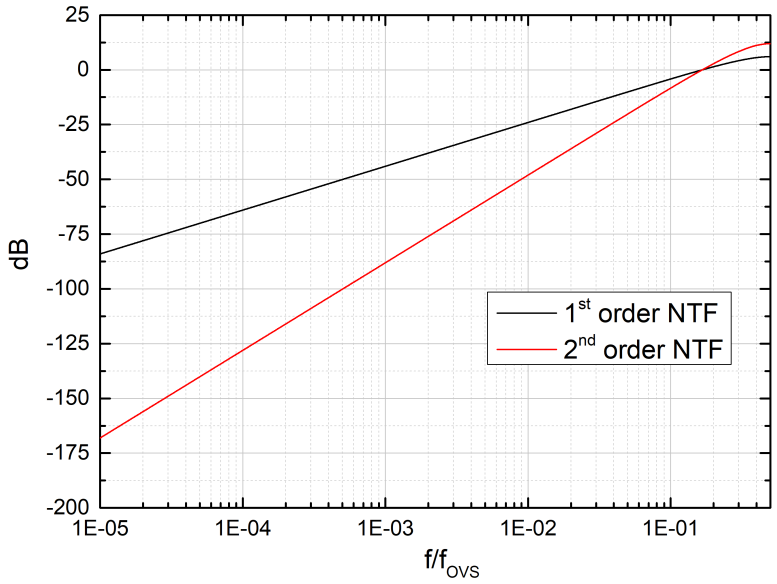


Figure 2.5: *Comparison of NTF of a 1^{st} order and a 2^{nd} order Δ-Σ Modulator.*

It is easy to demonstrate that in a 2^{nd} order Δ-Σ modulator, the amplitude of the dead-zones is inversely proportional to the product of the finite dc gain of the two integrators. A similar improvement is related to idle-tones: having a 2-dimensional state space (every integrator output is a state variable of the system), the probability of having repetitive state configurations and consequently repetitive patterns in the output bitstream for a certain input is much lower than in the first order modulator (a mono-dimensional space).

Concerning modulator stability, it is possible to derive the bounds of the internal state variables as a function of the input signal. Even if the internal states are bounded for input dc signal lower than the full-scale, the input of the quantizer (i.e. the output of the second integrator) may become arbitrary large for dc input signals approaching the full-scale. Also time-varying input signals with amplitudes lower than the full-scale may lead to diverging oscillations of the internal variables, even if these signals should have particular properties which do not occur often in practice. Typically, the input of

a second order modulator is bounded to 80-90% of the full-scale range.

Several modulator topologies can implement the same STF and NTF evaluated in equations 2.7 and 2.8. One of the most popular is the "Boser-Wooley modulator" [37], which replaces the delay-less integrators in Fig.2.4 with delaying integrators and removing the feedback delay, as depicted in Fig.2.6. The popularity of this topology is due to the relaxed requirements for the amplifier settling times and slew-rates, because the settling of each integrator is now independent. The coefficients in Fig.2.6 may be evaluated by means of high-level simulations as described in [28], taking into account the limited dynamic range of the integrators (due to amplifier saturation). The Boser-Wooley modulator is also called Cascade of Integrators FeedBack (CIFB).

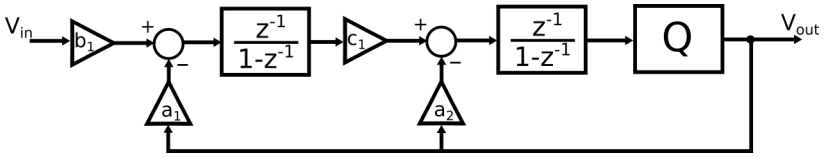


Figure 2.6: *Block diagram of 2nd order Boser-Wooley Δ-Σ modulator.*

An alternative to the CIFB topology is the Cascade of Integrators FeedForward (CIFF), or Silva-Steensgaard topology [38]. In this case, only the main feedback path from the quantizer output to the input of the first integrator is present. Feedforward paths from the input of the modulator and the output of the first integrator to the quantizer input are used to realize the same signal transfer function and noise transfer function of equations 2.7 and 2.8. In this topology, the input of the loop filter ($V_{in} - V_{out}$) is only the shaped quantization noise, instead of the high-pass filtered version of the input signal, relaxing the linearity specifications of the first block. Furthermore, the output of the second integrator is a delayed version of the quantization error, and this can be exploited in MASH structures, which will be described in the next paragraph. The other two topologies that complete the framework of second order modulators employed resonators in feedback or feedforward architectures. The drawbacks of resonators (or delay-less integrators), are the more strict specifications in terms of settling time errors of the amplifiers.

For a first order modulator, we have already observed how a $sinc^2$ is more effective to reject the quantization noise. It is possible to generalize this consideration about the digital filter, as stated in [28]: "the determining factors in finding the order K of the $sinc^K$ filter for an L^{th}-order $\Delta\Sigma$ modulator are

- the filter should cut off at a faster rate around f_B than the NTF of the $\Delta\Sigma$ modulator rises there, and;
- its gain response should be flatter around f_s/OSR and its harmonics than the NTF is around dc."

The two conditions guarantee a filtering response sharper than the NTF slope and a noise foldover around f_S/OSR and multiples sufficiently attenuated by the filter. It is easy to demonstrate that a low-pass filter with an order higher than the modulator order L satisfies the two conditions. Typically, an order $K = L + 1$ represents the optimal solution, as regards the trade-off between hardware complexity and the filter selectivity.

Thus, for a second order modulator, a third order low-pass filter is sufficient to properly reject the in-bandwidth quantization noise.

A very efficient way to implement a $sinc^K$ digital filter (with $K > 1$) is the Cascaded Integrator-Comb (CIC) filter, also known as Hogenauer filter [39]. A 3^{rd} order CIC filter is made up of the cascade of three accumulator stages, running at $f_S = f_{OVS}$, followed by three subtractor stages, running at the Nyquist rate. Between the accumulator and the subtractor stages, a downsampling of a factor OSR is performed. In [39], an optimization of the intermediate stages is also described, allowing a remarkable reduction of the filter hardware.

2.2.3 Higher order Δ-Σ Modulators, MASH topology and Bandpass modulators

A straightforward idea to improve further the converter resolution (keeping the OSR constant) is increasing the order of the modulator. For each integrator present in the loop filter, the multiplicative factor between resolution increasing and OSR improves by one. On the other hand, the stable input range decreases with the order. With a single-bit quantizer, the non-linear gain of the quantizer complicates the stability analysis with the linearised model of the modulator. The root locus technique may allow the analysis of the position of the poles for all the possible quantizer gains, and extensive behavioural simulations must be performed to ensure the modulator stability for the widest range of input signals. Multi-bit modulators can reduce stability issues, because of the well defined quantizer gain, at the cost of more circuital complexity to solve non-linearity issues introduced by the DAC.

An alternative way to increase the modulator order is to cascade two different Δ-Σ modulators, in order to increase the quantization noise rejection. Among those kinds of topologies, the most popular is the Multi-stAge noise-SHaping (MASH) modulator (Fig.2.7). The basic idea is to process the shaped quantization noise of a Δ-Σ modulator with another Δ-Σ modulator, and then to subtract the output of the two modulator, properly conditioned, in order to remove the quantization noise of the first modulator. The final quantization noise is the one of the second order, shaped by a noise-transfer function equal to the product of the NTF of the two modulators.

It is straightforward to study the behaviour of the MASH modulator:

$$V_1(z) = STF_1(z)V_{in}(z) + NTF_1(z)v_{n-q1}(z) \tag{2.10}$$

where STF_1 and NTF_1 are respectively the signal transfer function and noise transfer function of the first modulator.

$$V_2(z) = STF_2(z)v_{n-q1}(z) + NTF_2(z)v_{n-q2}(z) \tag{2.11}$$

$$\begin{aligned} V_{out}(z) &= V_1(z)H_1(z) - V_2(z)H_2(z) \\ &= V_{in}(z)H_1(z)STF_1(z) + v_{n-q1}(z)(NTF_1(z)H_1(z) - H_2(z)STF_2(z)) \\ &- v_{n-q2}H_2(z)NTF_2(z) \end{aligned} \tag{2.12}$$

If the condition $H_1(z)NTF_1(z) = H_2(z)STF_2(z)$ is guaranteed, than the quantization noise of the first modulator is rejected. The simplest choice is $H_1(z) = STF_2(z)$

and $H_2(z) = NTF_1(z)$, obtaining the overall transfer functions:

$$STF_{MASH}(z) = STF_1(z)STF_2(z) \tag{2.13}$$

$$NTF_{MASH}(z) = NTF_1(z)NTF_2(z) \tag{2.14}$$

For example, considering two 2nd order modulators in a MASH topology, a 4th order noise-shaping function is obtained. The main drawbacks is related to the criticality of matching between the analog transfer functions of the modulators and the digital ones $H_1(z)$ and $H_2(z)$. Variations of the analog transfer functions from the nominal ones, for example due to mismatch of passive components (as the capacitive ratios in the integrators) or amplifier finite gain, increases the MASH noise due to an imperfect cancellation of the first modulator's quantization noise.

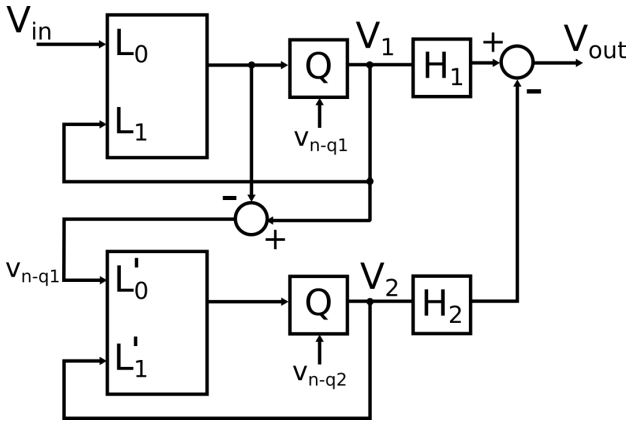


Figure 2.7: *Block diagram of a MASH modulator.*

Another interesting topology is the bandpass Δ-Σ modulator, very diffused in telecommunications systems. Typical wired and wireless communication systems exploits homodyne or heterodyne conversion in the receiver, downconverting the incoming signal to a frequency lower than the carrier frequency. Depending on the bandwidth of the signal and the kind of downconversion, Δ-Σ low-pass converters can be used for digitizing the signals, thanks to their good trade-off between resolution, power consumption, linearity and anti-alias filtering requirements (especially with continuous-time implementations, as we will see in the next paragraph). An interesting alternative avoids the down-conversion, implementing a band-pass Δ-Σ modulator which presents a STF and a NTF not centred around dc, but around a certain frequency f_0. Typically $f_0 = f_S/4$, such that the sampling frequency is not much higher than the carrier frequency, as it would be with low-pass modulators. The converter frequency range is $[f_0 - B_W/2 : f_0 + B_W/2]$, where $B_W = f_S/(2OSR)$ gives the usual advantage of oversampling and noise-shaping seen for low-pass modulators. In this way, the bitstream will be down-converted by a digital mixer and low-pass filtered and decimated to obtain the final increased resolution. This receiver can be a much more efficient solution because of the suppression of the down-conversion in the analog-domain, which can affect heavily the power consumption and spoil the signal integrity.

The implementation of a n-th order band-pass modulator required, in general, a doubled complexity compared to a n-th order low-pass modulator. Effectuating the

substitution $z \rightarrow -z^2$ in the STF and NTF seen for low-pass modulator, the band-pass functions are obtained. This substitution can be obtained straightforwardly by a pseudo 2-path transformation of a low-pass modulator, which requires 2 low-pass modulators [28] as in Fig.2.8.

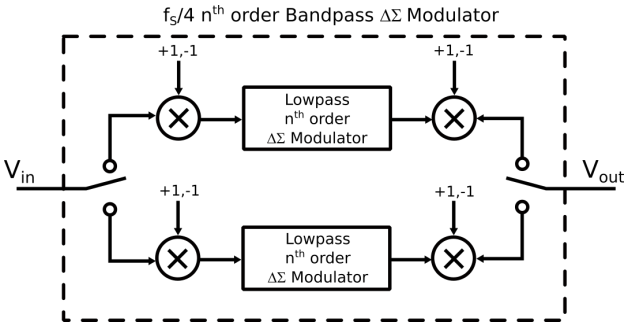


Figure 2.8: *Block diagram of a $f_S/4$ n^{th} order Δ-Σ modulator.*

An alternative way to implements a resonator at $f_s/4$ with a single op-amp is by means of periodically swapping of the integrating capacitors in the discrete-time integrator. This technique has been exploited to implement system-level CHS for a low-pass modulator [40]. A detail analysis is provided in 2.3.4.

2.2.4 Continuous-time Δ-Σ converter

So far, we have analysed the behaviour of discrete-time Δ-Σ modulators. DT implementations sound very attractive due to their good linearity and accuracy, without strict requirements on passive element matching. Moreover, the modulator transfer functions, in the z-domain, are independent from the sampling frequency, so that it is very easy to scale the sampling frequency. Finally, jitter does not have critical effects, once we have guaranteed the correct settling time for all the blocks.

The other family of Δ-Σ converter is the continuous-time one. Unlike DT modulators, where the input signal is sampled at the very beginning before the loop filter, in CT modulators sampling occurs just before the quantizer, after the loop filter (Fig.2.9). This means that the low-pass response of the loop-filter, employed to suppress the quantization noise, also acts like anti-aliasing filter before the sampling and the effective quantization. This feature is very important because it allows the suppression of anti-alias filters, which often represent the bottleneck of the ADC design in several applications. Furthermore, CT modulators are able to work with sampling frequency 2-4 times higher than the DT modulators, allocating the same power consumption for the amplifiers, because there is not a severe degradation of linearity performance between sampling frequency and the amplifier settling time as in switched-capacitor circuits. These advantages make CT modulator very attractive for high-frequency applications, where typically DT modulators are not power efficient, as it looks evident also from the plots in Fig.1.5. It is worth noting that CT modulators suffer much more of noise jitter in the DAC, because a variation on the clock period directly affects the amount of charge accumulated in the continuous-time integrators. In general, for high-resolution applications with low-frequency input bandwidths, DT modulators results more appealing due to their flexibility with the variation of the sampling frequency and robustness

with respect to mismatch of passive elements and clock jitter.

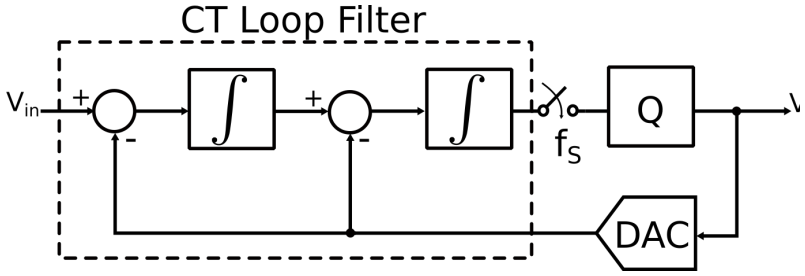


Figure 2.9: *Block diagram of 2^{order} CT Δ-Σ modulator.*

2.3 Proposed Δ-Σ converter

After this brief introduction, the design of a 2nd order, discrete-time Δ-Σ ADC will be described. This converter has been optimized for sensor acquisition systems with elevate requirements of accuracy and resolution. It has been designed to work properly with low-frequency input signals (from dc to few kHz), with a resolution of 16 bit. Particular attention has been spent for offset and flicker noise minimization, implementing two different CHS techniques. A power-efficient solution to reduce settling-time errors has also been developed and fully described. Preliminary measurements on a UMC 0.18 μm prototype show its good performances for dc readout and low-frequency signal acquisitions.

2.3.1 High-level design

Among the possible modulator topologies explained in the previous section, we opted for a second order, discrete-time, single-bit, Cascade Integrator FeedBack (CIFB) modulator. The choice has been dictated by stability, timing requirements and hardware compactness. A second order modulators offers an optimum trade-off in these terms: first order modulator does not provide sufficient quantization noise rejection, and it is more prone to idle tones and dead zones. Discrete-time converters does not suffer of jitter as continuous-time ones and they are more flexible with respect of the variations of the sampling frequency. Single-bit modulator offers the great advantage of reaching high resolutions without strict requirements on DAC matching properties. In fact, single-bit implementation are typically more simple and compact, not requiring additional digital technique for the randomization of the DAC elements. In this work, we focused on the design issues concerning the analog part of the modulator, leaving the space for future developments. Possible improvements may concern the digital part, involving the DEM technique for a multi-bit modulator.

High-level simulations in Matlab-Simulink (MS) environment are the first step towards the design of a Δ-Σ modulator. The DSToolbox developed by R.Schreier [28] allows the proper sizing of the coefficient needed in CIFB topology, taking into account the possible limitation of the state variables (i.e. the integrators' outputs) due to the saturation of the amplifiers. Transient simulations allow the verification of the dynamic performances of the converter, verifying if SQNR and SINAD are the ones targeted. Eventually, the coefficient values a_1,b_1,c_1,a_2 are obtained and they will be implemented

by means of capacitive ratios. The absolute value of the input sampling capacitor of the first integrator, instead, will be obtained by means of thermal noise considerations.

Several tools for MS verifications have been developed [41–44] in order to take into account as much as possible the modulator non-idealities. Amplifier finite dc gain and non-linearities, amplifier finite bandwidth and slew-rate, thermal noise and jitter can be easily simulated in a fast and accurate way in MS. In paragraph 2.3.4, a modification of the MS tool developed in [41] has been proposed in order to take into account also flicker noise and to simulate the proposed CHS technique.

A critical aspect in high-resolution Δ-Σ concerns the thermal noise, in order to size properly the value of the sampling capacitors C_S of the first integrator (Fig.2.11). It is possible to model the error sources introduced by each single block as in Fig.2.10. The error voltages v_{n1} and v_{n2} include the Referred-To-Input (RTI) offset and noise rms voltages of each integrator H(z). These noise contributions affect the output through the following transfer functions in the z-domain:

$$NTF_1(z) = \frac{Y(z)}{v_{n1}(z)} = \frac{z^{-2}}{b_1} \tag{2.15}$$

$$NTF_2(z) = \frac{Y(z)}{v_{n2}(z)} = z^{-1}(1 - z^{-1}) \tag{2.16}$$

It is worth noting from 2.16 that offset and low-frequency noise of the second integrator are intrinsically high-pass filtered, so that they do not give significant contributions in the signal passband. The Fully-Differential (FD) Parasitic-Insensitive (PI) integrator (Fig.2.11) can be used to implement the needed H(z) function. The expression of its RTI Noise Power and the effects on the ADC resolution can be evaluated as follows (for more details, see appendix A). Let us start from the input spectral density of the amplifier (A), which can be expressed by:

$$S_n(f) = \left(1 + \frac{f_k}{f}\right) S_{BB} = \left(1 + \frac{f_k}{f}\right) 4kT \frac{1}{G_M} \gamma \tag{2.17}$$

where S_{BB} is the thermal noise power spectral density (PSD), referred to an equivalent resistance equal to $1/G_M$ (G_M is the transconductance of the input pair of A) increased by a factor $\gamma > 1$, depending on the amplifier topology. Frequency f_k is the flicker corner frequency of the amplifier. To determine the thermal component of the total integrator RTI noise power (P_{th}), the integral of S_{BB} over the amplifier equivalent noise bandwidth (B_{eq-n}) should be added to the kT/C noise coming from the switch activity (doubled due to the differential structure) [41, 45]:

$$P_{th} = 2\frac{kT}{C_S} + S_{BB} B_{eq-n} = \frac{kT}{C_S}(2 + \gamma) \tag{2.18}$$

P_{th} is uniformly spread across the bandwidth $[0, f_S/2]$ due to the sampling operation (noise foldover). It can be assumed that foldover affects less the flicker noise component, leaving it practically unchanged. The electrical noise power at the output of the converter can be obtained by integrating the integrator RTI PSD filtered by the low-pass filter H(f):

$$\sigma^2_{el-n} = \int_{f_{min}}^{f_S/2} \left(\frac{f_k S_{BB}}{f} + P_{th} \frac{2}{f_S} \right) |H(f)|^2 \, df \tag{2.19}$$

where f_{min} is the minimum observable frequency, roughly equal to the inverse of the period of observation. From the expression of the effective resolution 2.3.1 (or better the expression of the noise-free resolution), the quantization-noise power and the thermal noise 2.19, it is easy to get the expression of the ENOB as a function of the flicker corner frequency of the amplifier A, as well as a function of γ and C_S. From 2.15 and 2.19 it is also evident that offset and low-frequency noise of the first integrator affect directly the converter performances and they must be faced with proper techniques.

In section 2.3.4, the description of an alternative chopper technique adapted specifically for a Δ-Σ modulator is widely discussed. Behavioural simulations help the understanding of its operating principle, while electrical simulations show its effectiveness also for Electrochemical Impedance Spectroscopy applications. Finally, measurement results confirm its effectiveness and its superiority against the standard CHS technique in terms of offset rejection and flicker reduction.

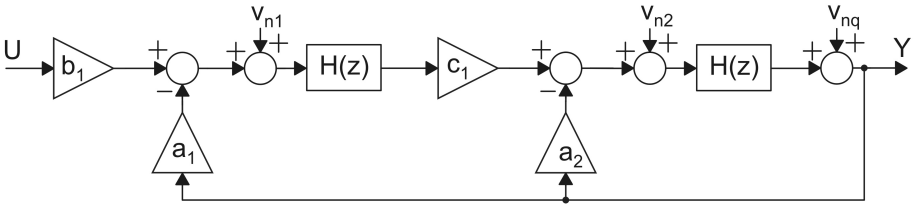


Figure 2.10: *Block diagram of a 2nd order discrete-time Cascade-Integrator-FeedBack (CIFB) Δ-Σ Modulator, with error voltage sources of each integrator and quantization error.*

The value of the sampling capacitor of the first integrator has been optimized, taking into account the requirements of resolution, area and power consumption. According to , it is possible to write the thermal noise of the first integrator (that is, as already explained, the dominant one even in a second order modulator) with the well-known form of kT/C noise, including the factor γ, which takes into account the amplifier topology. Exploiting the definition of ER defined in , it is possible to find the value of sampling capacitor C_S needed for the fulfilment of a certain resolution, as a function of the oversampling ratio. A sampling capacitor of 4 pF represented for us a good trade-off, in the light of the above-mentioned considerations.

2.3.2 Transistor-level design

In this paragraph, a brief insight on the transistor-level design of the proposed Δ-Σ converter will be provided, with particular attention on the design of the first integrator, the most critical block, and the amplifier employed in it. A Fully-Differential (FD) approach has been chosen, due to its better performances in terms of interferences rejection (as capacitive coupling to interfering lines, substrate noise and non-uniform ground voltage), double output range range and increased linearity [15, 46, 47]. The target supply voltage range goes from 1.8 V (the supply voltage of the digital core

devices for the UMC 0.18 μm process) to 3.3 V (the maximum voltage allowed for the I/0 devices in the same process). The maximum sampling frequency is 1 MHz, high enough to allow sufficient OSRs in order to achieve the target resolution of 16 bits in the bandwidth of interest.

First integrator

The topology of the two integrators is a fully-differential, parasitic-insensitive (PI), switched-capacitor integrator. The input capacitors C_s^+ and C_s^+ together with the input switches, effectuate the sampling of the input signal. Due to the same value of the two coefficients a_1 and b_1 (because of the desired unity gain for the STF of the converter), the input capacitors $C_S^{+,-}$ also implements the subtraction of the input and the feedback differential signals. The charge proportional to the difference of the two sampled voltages is transferred on the feedback capacitors $C_F^{+,-}$. The coefficient $a_1 = b_1$ is implemented by means of the capacitive ratio C_S/C_F. More details about the behaviour of this type of circuit is provided in appendix A, where the analysis in the ideal case and in the presence of finite dc gain and noise are given for a single-ended topology. As well known, the first integrator is the most critical block in terms of offset, noise and non-linearities, because its contributions are one-to-one referred to the input signal of the converter. Two non-overlapping clock phases are generated to properly drive the switches, and a bottom plate sampling technique (BPS) [37] has been implemented to reduce charge injection issues.

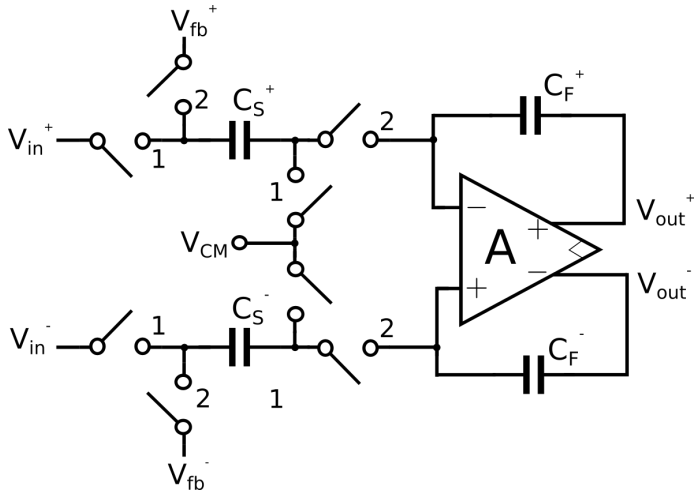


Figure 2.11: *Schematic view of the fully-differential, parasitic-insensitive, switched-capacitor integrator which implements the first integrator.*

The design of the amplifier employed in the integrator is very important and requires great attention. High dc gain is required in order to reduce dead-zones, converter gain-error and to improve quantization noise rejection. Differential output range should be as large as possible, in order to exploit the whole dynamic range of the integrator; the lower is the range, the higher are the coefficients a_1,b_1, which decrease converter performances in terms of speed and area consumption. At the same time, minimization of amplifier noise is a main concern, due to the high resolution required. In order to minimize amplifier thermal noise power, transistor sizing is in contrast with the design

for maximizing output differential range. About flicker noise and offset, higher area consumption would be requested, with severe penalties in terms of occupation of silicon area and speed performances. The implementation of a CHS technique is almost mandatory, considering the low-frequency band of interest.

Concernig the amplifier, a single-stage folded-cascode topology (Fig.2.12) has been chosen, due to its excellent performances for high-resolution converters [48]. The PMOS input pair has been used in order to realize the bulk-source connection and reduce the body effect, achieving an higher input common mode range[3]. The high output resistance guarantees a dc voltage gain high enough, because no resistive load is present. The simplicity of a single-stage amplifier, compared to a two-stage amplifier, in terms of common-mode stabilization and current consumption, has driven the choice towards a single-stage amplifier.

Output common-mode voltage stabilization is realized by means of a dynamic Common-Mode FeedBack (CMFB) circuit as the one described in [15] and shown in Fig.2.13. Values of the CMFB capacitors C, and clock frequency as well, are critical in order to not affect the amplifier gain, because of the equivalent resistive load caused by the switching capacitors that may lower the output load. Capacitors C' and C" realize a kind of class AB common-mode control, acting only in ac. While the SC operations stabilize the steady value of the output common mode, C' and C" are able to correct fast output common-mode variations, controlling the gate voltages of the common-source stages.

To achieve better performances in terms of dc gain and speed, the common-source stages are realized by means of trapezoidal-shape transistors (T-transistors) [49–51], as shown in Fig.2.14-b. It is easy to demonstrate how, for the same area and the same mirror ratio as the simple mirror of Fig.2.14-a, an increase of the output resistance is obtained. In the same way, a lower area consumption is made possible by the T-mirror compared to the standard one, for the same output resistance and mirror ratio. The noise analysis of T-transistors can be found in [52].

In order to reduce the offset and flicker noise contribution of the amplifier, a dynamic offset cancellation technique [26] can be implemented. As it will be further explained in paragraph 2.3.4, CHopper-Stabilization technique fits Δ-Σ converters perfectly because of the presence of the digital low-pass filter, which can be exploited to reject the offset ripple. However, the straightforward implementation of the CHS technique shown in Fig.2.15 would decrease the output resistance, due to the continuous charge and discharge of the parasitic capacitances of the demodulator switches. For this reason, the chopper demodulation has been realized at low-impedance nodes inside the amplifier, more precisely between the sources of the common-gate stages and the drains of the common-source stages of the cascode structures, as depicted in Fig.2.16. In this way, offset and flicker noise contributions of common-gate MOSFETS is not rejected by CHS. Anyway, contributions from those transistors is typically negligible, as explained in [15]. Besides the implementation of the described CHS technique, a novel chopper stabilization technique has been adopted, in order to reject also offset contribution from charge injection mismatches and other offset contributions of the whole modulator. More details will be provided in paragraph 2.3.4 and measurements on the

[3]The process used for this design is a twin well CMOS process, than the bulk-source connection is allowed only for the PMOS devices.

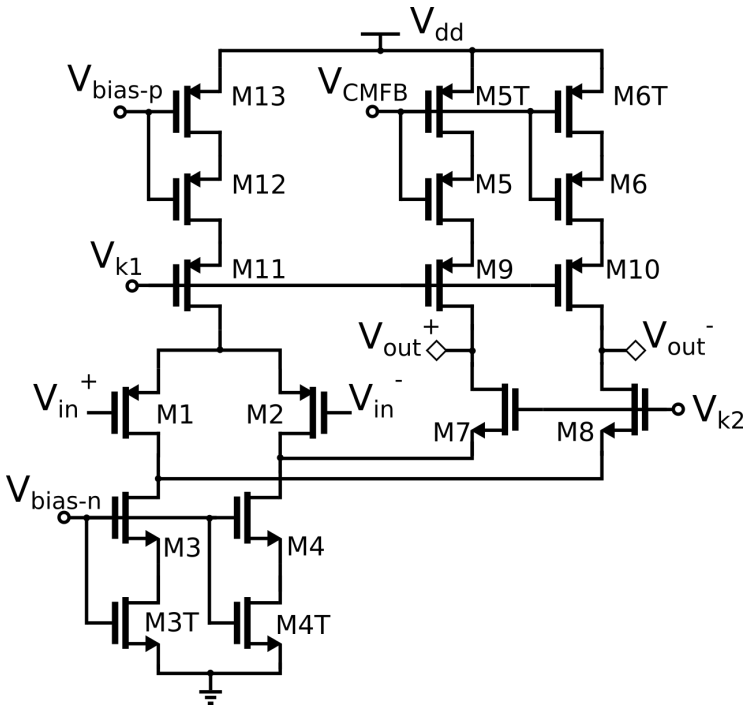


Figure 2.12: *Schematic view of the fully-differential folded-cascode amplifier with T-transistors.*

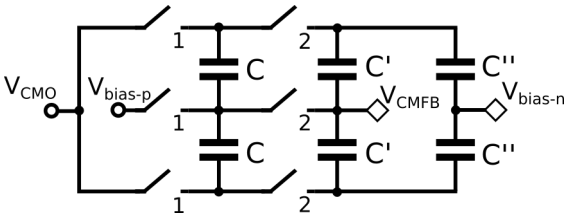


Figure 2.13: *Schematic view of the common-mode feedback control circuit.*

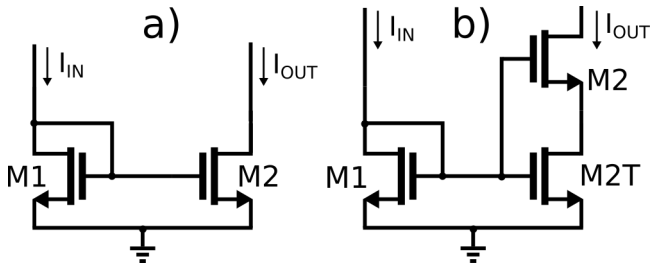


Figure 2.14: *a) Simple NMOS mirror. b) Simple NMOS mirror with T-transistor.*

prototype will also provide a comparison between the two CHS techniques.

In table 2.1, the sizing of each MOSFET device present in Fig.2.12 is reported.

Second integrator

The topology chosen for the second integrator is the same as for the first one. Due to the different coefficients c_1 and a_2, it would not be possible to reuse the same sampling capacitors to sample the output of the first integrator and the feedback voltage, in a

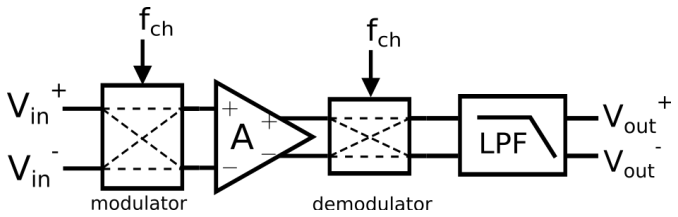


Figure 2.15: *Block diagram of a traditional chopper in a fully-differential system.*

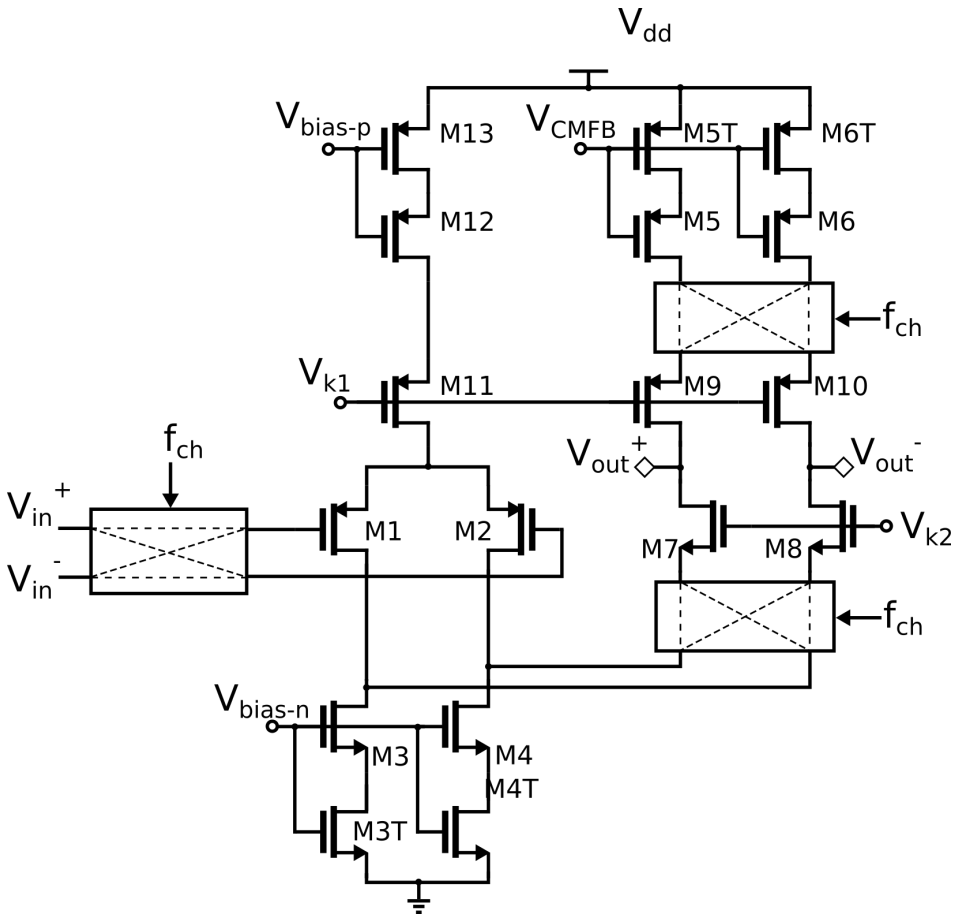


Figure 2.16: *Schematic vivew of the fully-differential folded-cascode amplifier with chopper modulation technique.*

similar fashion as described for the first integrator. Additional branches are required, with consequent negative effects also on the first integrator loading. The sampling capacitors, in fact, are periodically charged to the first integrator output and then discharged, behaving like an equivalent resistance that can reduce the effective dc gain of the first amplifier. For this reason, a different approach with respect to the conventional one has been chosen (Fig.2.17). An additional DAC with a reference voltage V_{ref2} is used to generate the feedback voltage for the second integrator. In this way, the second reference voltage, obtained from an attenuation of the main one, implements part of the coefficient a_2 needed in the second feedback path. Designing V_{ref2} such that: $V_{ref2} = \alpha V_{ref}$, where $\alpha = a_2/c_1$, a unique coefficient c_1 for the second integrator is

Table 2.1: *Sizing of the folded cascode amplifier:*

Device	Length (μm)	Width (μm)	Finger number	Multiplier
M1-2	0.9	72	1	4
M3-M4	4.8	0.8	10	6
M3T-M4T	4.8	0.8	10	3
M7-M8	1	10	4	1
M5-M6	2	1.6	5	6
M5T-M6T	2	1.6	5	3
M9-M10	3	15	5	2
M12	2	1.6	5	12
M13	2	1.6	5	6
M11	3	15	5	4

required. With this approach, the same sampling capacitors can be used to sample the output of the first integrator and the attenuated feedback voltage. Thanks to the negative feedback of the Δ-Σ modulator, virtual short-circuit is present between the mean values of the two differential input signals of the two integrators (if a single coefficient is present, as in Fig.2.17). Than, no loading effect (at low frequencies) is present and the dc gain of the first integrator is not penalised.

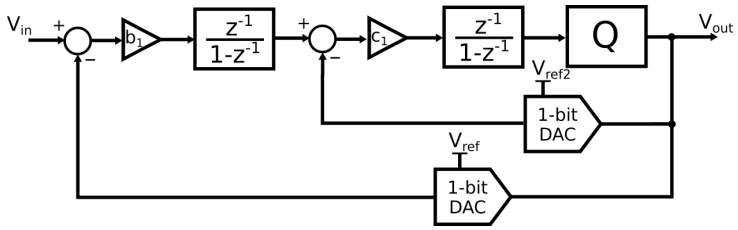


Figure 2.17: *Block diagram of the proposed 2nd order discrete-time Cascade-Integrator-FeedBack (CIFB) Δ-Σ Modulator, with two different reference voltage Vref and $Vref_2$.*

As already mentioned, offset and noise contribution of the second integrator is typically negligible, due to the high-pass filtering function from the second integrator input to the converter output. For this reason, no offset cancellation technique has been implemented for this amplifier. Sampling capacitors are realized with a value ten times lower compared to the ones for the first integrator, reducing the current consumption of the amplifier. A folded cascode topology has been adopted also for the second integrator, with considerably relaxed specifications in terms of power consumption, dc gain, noise and offset. The second reference voltage is generated by means of a resistive voltage divider starting from the first reference voltage (generated by a bandgap reference voltage or taking directly the supply voltage). Having low capacitance in the second integrator, a relatively high overall impedance of the voltage divider is allowed without degrading the speed performance (740 $\mathrm{k}\Omega$). Furthermore, we do not impact heavily on the power consumption: the current consumption on the resistive ladder is lower than 4.5 μA.

In table 2.2, the sizing of each MOSFET device of the folded-cascode amplifier employed in the second integrator is reported, considering that the amplifier topology is the same as the one depicted in Fig.2.12, without the T-MOS transistors (then M3T,

Table 2.2: *Sizing of the folded cascode amplifier:*

Device	Length (μm)	Width (μm)	Finger number	Multiplier
M1-2	0.9	36	1	2
M3-M4	2	4	1	2
M7-M8	1	30	1	1
M5-M6	1	12	1	1
M9-M10	0.9	12.6	1	1
M12	1	12	1	2
M11	0.9	12.6	1	2

M4T, M5T, M6T and M13 are not present).

Comparator

Offset and noise of the comparator is further high-pass filtered, thanks to the second order high-pass filtering function from the comparator input to the modulator output. A latched comparator with a preamplifier, in order to reduce the comparator hysteresis, has been implemented as shown in Fig.2.18. The preamplifier is a simple amplifier with mirror load, while the comparator is depicted in Fig.2.18. Phase 1 is when the comparison takes place, while phase 2 is the hold phase, where the two outputs of the comparator stage are pulled-up to V_{dd}, so that the cascaded SR latch keeps the result of the previous comparison, realizing a not-return-to-zero (NRZ) codification.

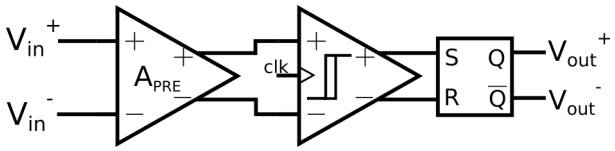


Figure 2.18: *Block diagram of the whole comparator, made up of the preamplifier, the actual comparator and the SR latch.*

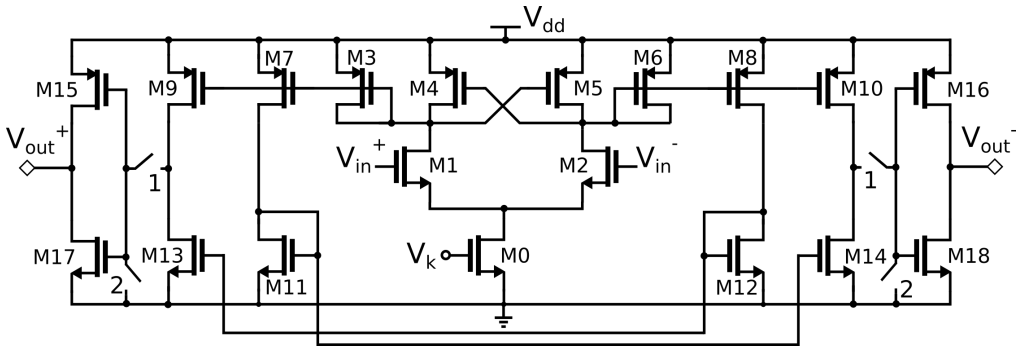


Figure 2.19: *Schematic view of the comparator.*

The output of the comparator, which coincides with the modulator output, is fed-back to the integrators through the two DACs of Fig.2.17, realized by means of two inverters connected to the differential reference voltage (supply voltage and ground, as in ratiometric application, or a differential reference voltage provided by a bandgap

Table 2.3: *Sizing of the comparator:*

Device	Length (μm)	Width (μm)	Finger number	Multiplier
M0	2	2.5	1	1
M1-2	1	4	1	1
M4-5	1	1.5	1	1
M3-6	1	1	1	1
M7-8	1	1	1	1
M9-10	1	1	1	4
M13-14	1	1	1	4
M11-12	1	1	1	1
M15-16	0.8	0.8	1	4
M17-18	0.5	0.5	1	1

circuit). The positive output of the comparator is also the input of the digital filter, as the bitstream that must be low-pass filtered and decimated in order to obtain the filtered data.

In table 2.3, the sizing of each MOSFET device of the comparator is reported.

2.3.3 Digital filter

As already mentioned, the Cascaded Integrator-Comb (CIC) is a hardware-efficient solution to implement a digital, low-pass, decimator filter with $sinc^n$ frequency response. The block diagram of the implemented 3rd order filter is shown in Fig.2.20. Three accumulator stages work at the oversampling frequency, which is the throughput of the modulator. After the decimation stage, characterized by a decimating factor OSR, the comb stages work at the Nyquist frequency, which is also the output throughput. Changing the oversampling frequency f_S and/or the oversampling ratio OSR, it is easy to change the notch frequencies of the filter, in order to reject specific spurs at well-known frequencies.

The sizing of each intermediate register has been optimized as suggested in [39], taking into account the programmability of OSR from 32 to 4096, an input bitstream of 1 bit length and an output word of 20 bit. Furthermore, the CIC filter implements the bitstream demodulation, when it is required during system-level CHS (see next paragraph). A Hardware Description Language has been adopted to describe the CIC filter, in order to effectuate the standard-cell synthesis and the place-and-route by means of the automatic tools present in Cadence environment.

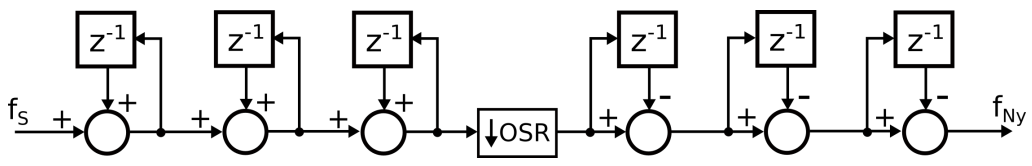
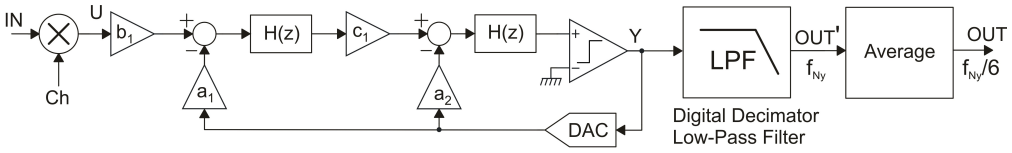


Figure 2.20: *Block diagram of a 3rd order CIC filter.*

2.3.4 System-Level Chopper Technique

Several solutions have been adopted in the literature to reject low-frequency noise and offset in Δ-Σ modulators. One possible solution often employed in commercial products as in [34] implements the chopper modulation at the input of the modulator (or at the input of the programmable gain amplifier preceding the ADC) and the demodulation in the digital domain, after the CIC filter (Fig.2.21-a). Fig.2.21-b shows the output code of the filter, between the demodulation and further averaging. As it looks evident, the chopper frequency is limited by the filter settling time, reducing the effectiveness of the CHS with respect to flicker noise rejection.

(a)



(b)

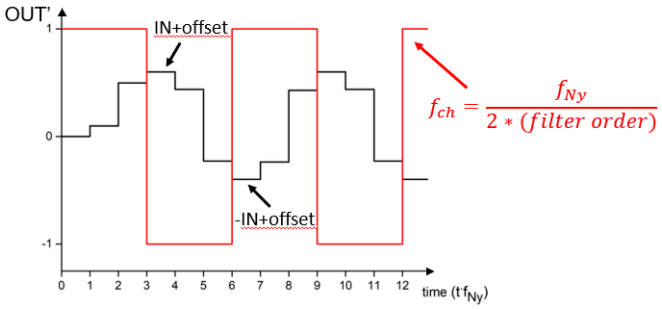


Figure 2.21: *a) Block diagram of the chopper technique implemented in commercial Δ-Σ ADCs. b) Output of the digital decimator filter and chopper clock signal.*

Several offset cancellation techniques have been applied in the analog domain. CDS techniques generally require more complex SC integrator topologies and they will not be considered here [53]. On the other hand, CHS techniques can be easily implemented in FD PI integrators in two alternative ways. The more straightforward one consists in the synchronous periodic swapping of the two inputs and the two outputs of the FD amplifier [26], as depicted in Fig.2.15. The second CHS technique requires the periodic swapping of the integrator capacitors and the modulation of the integrator inputs at the same chopper frequency (f_{ch}) [54]. Chopped offset introduced by CHS techniques can be rejected if the chopper frequency is a multiple integer of the Nyquist frequency, so that the chopper artefacts coincide with the notches frequencies of the CIC filter. Both techniques are fulfilled at high frequency to reject effectively flicker noise. After CHS, in fact, the contribution of flicker noise on the integrator RTI PSD is [26]:

$$S_{fk_{ch}} \cong \frac{8}{\pi^2} S_{BB} \frac{f_k}{f_{ch}} \tag{2.20}$$

However, a residual offset due to the mismatch of charge injection from the switches is still present in both cases. Furthermore, high frequency transitions due to chopper modulation lead to continual upsets of amplifier inputs and outputs, which can make the amplifier prone to static gain decrease and total harmonic distortion rising. These

drawbacks are partially solved by the system-level CHS technique, combined with the traditional high-frequency CHS applied to the amplifier [55]. The high-frequency CHS rejects effectively the amplifier flicker noise, while the system-level CHS at $f_{ch} = f_S/OSR$ rejects the residual offset. The system-level CHS (Fig.2.22-a) implements the modulation of the input signal in the analog domain and the demodulation of the output bitstream in the digital domain. A low-pass modulator would not allow the straightforward implementation of this technique: this issue can be easily overcome by means of the periodical flipping of the integrator capacitors, obtaining the flipped-capacitor integrator (FCI) shown in Fig.2.22-b.

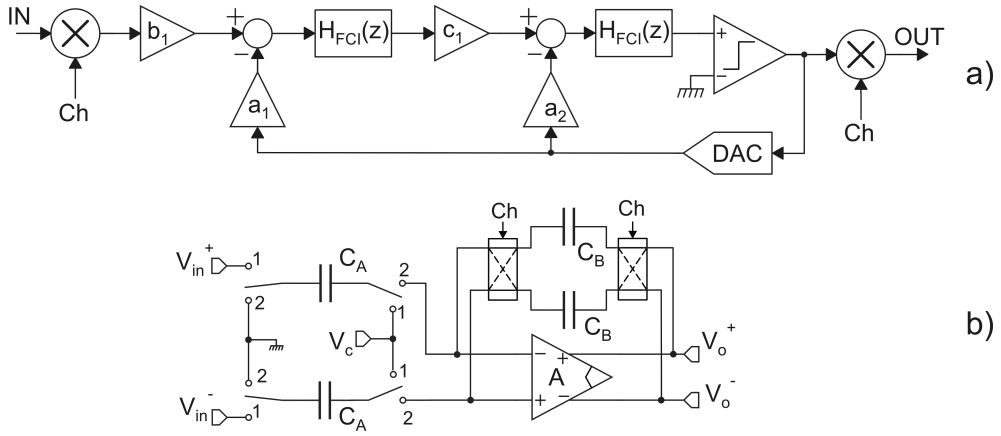


Figure 2.22: *a) Block diagram of system-level chopping; b) schematic view of FCI.*

The FCI has been already employed in band-pass Δ-Σ converters for Intermediate Frequency (IF) data conversion using $f_{ch} = f_S/2$ [56]. To our knowledge, in the literature there are no examples of Δ-Σ converters employing FCIs at chopper frequencies different from $f_S/2$ and f_S/OSR. We propose to extend the FCI chopper frequency range for the system-level CHS. For this reason, we have studied the effects of the capacitor flipping at frequency f_{ch} on the integrator transfer function. The generic FCI transfer function in the z-domain for $f_{ch} = f_S/M$, with M even number greater than 2, is:

$$H_{FCI}(z) = \frac{V_{out}(z)}{V_{in}(z)} = k_s z^{-1} \frac{1 - \sum_{i=1}^{M/2} z^{-1} \sum_{j=\frac{M}{2}+1}^{M-1} z^{-j}}{1 - z^{-M}} \tag{2.21}$$

where k_s represents the capacitance ratio C_A/C_B in the integrator of Fig.2.22. Fig.2.23-a shows the magnitude frequency response of the FCI, considering, for example, a chopper frequency $f_{ch} = f_S/64$. The peaks of $|H_{FCI}(f)|$ at f_{ch} and odd order harmonics lead to the NTF and the STF in Fig.2.23-b for a first order Δ-Σ modulator. The NTF shows a notch-response at f_{ch} and odd order harmonics, while the STF is nearly flat and equal to 0 dB close to those frequencies. The modulator shows the desired frequency response, without the need of doubling the complexity as for band-pass modulators [28]. When quantization noise is digitally demodulated, its power after the filtering is the same as in a standard low-pass Δ-Σ modulator. On the other hand, offset and low-frequency noise of the whole modulator are only up-converted to f_{ch} and then rejected by the digital decimating low-pass filter, choosing a chopper frequency

multiple of the Nyquist-rate $2B_W$.

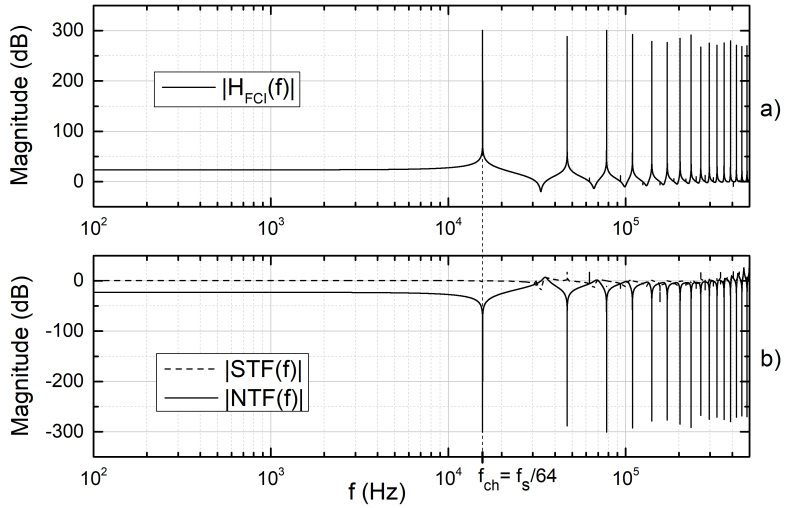


Figure 2.23: *a) Magnitude response of FCI with f_S=1 MHz and f_{ch}=f_S/64; b) magnitude response of STF and NTF of a 1st order modulator with FCIs.*

High-Level Description

Behavioural descriptions of Δ-Σ modulators are very useful to estimate their performances and simplify the sizing of the key blocks. As already said, several MS tools have been developed [28, 41] and, usually, amplifier flicker noise is neglected, assuming the implementation of dynamic techniques of offset cancellation.

Typical mathematical modeling of flicker noise exploits algorithms like Moving Average (MA) or Autoregressive (AR) time series. Due to the limited memory resources, the generated number sequence turns out to be stationary, and its PSD shows a flat behaviour for frequencies lower than a limiting frequency depending on the available memory [57]. A MS block called "coloured noise" is capable to generate a sequence with 1/f PSD at a specified output sampling rate. This block exploits the AR algorithm and suffers from PSD saturation at low frequencies, depending on the desired output sample rate (red curve in Fig. 2.24). To overcome this issue, we have developed a simple solution alternative to [58]: the outputs of two "colored noise" blocks with different sample rates are summed up to reach the 1/f behaviour from the sampling frequency down to f_{min}, with a good approximation (Fig.2.24). Choosing properly the two different output sampling rates, where one is multiple of the other, there is no need of additional "sample and hold" blocks.

The proposed behavioural model of the FCI is shown in Fig.2.25-a: the capacitor flipping is modelled by means of the product of the delay block output with a proper signal (mod), whose temporization is depicted in Fig.2.25-b. The factor α represents the effect of the amplifier finite dc gain.

Simulations

The effectiveness of the system-level chopper technique has been proved by means of the proposed MATLAB/Simulink modeling, considering as amplifier case study a

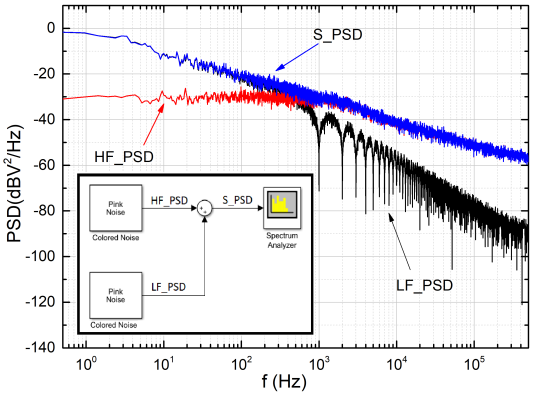


Figure 2.24: *MS flicker noise PSDs: HF-PSD has a sampling rate of 1 MHz, LF-PSD has a sampling rate of 1 kHz and it is represented in the same frequency range, S-PSD is the resulting PSD obtained as depicted in the inset.*

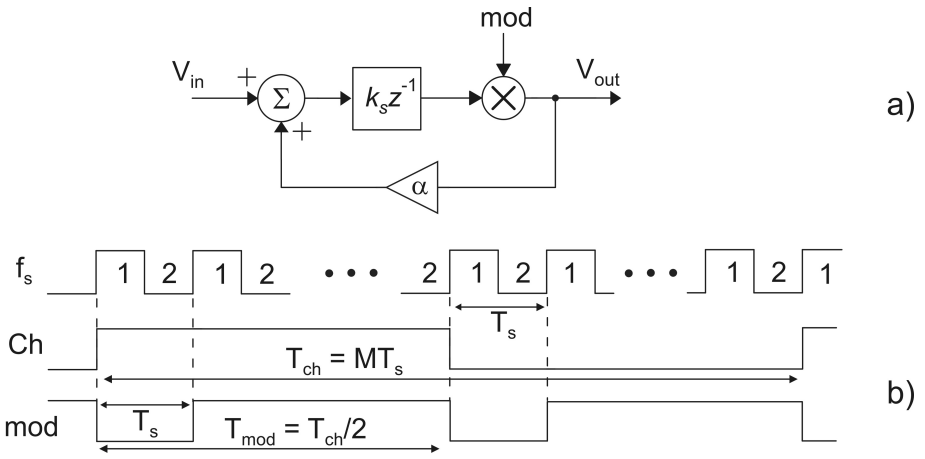


Figure 2.25: *a) Behavioural model of FCI; b) timing diagram.*

fully-differential folded cascode, usually employed for SC PI integrators in DT Δ-Σ modulators. The prototype was designed with the UMC 0.18 µm CMOS process, considering a sampling frequency f_S of 1 MHz and an input sampling capacitance of 4 pF. The total current consumption is 40 µA and the estimated area occupation is only 430 μm^2. From electrical simulations in Cadence environment, the RTI PSD shows a broadband noise S_{BB} of 3.42·10-16 V^2/Hz and a flicker corner frequency f_k of 280 kHz. The digital low-pass decimating filter is a 3rd order Cascade-of-Integrator-Comb (CIC) filter, implemented in MATLAB with a decimation factor of 512, obtaining a throughput of 1.953 kHz. Applying the analytical model above mentioned, the estimated resolution for a second order Δ-Σ converter with $OSR = 512$ based on the amplifier prototype is 15.29 bits. MS simulations, exploiting the proposed flicker noise model, provide an effective number of bits of 15.41, very close to the theoretical result. In all the tests, the contribution of the second integrator noise to the resolution was confirmed to be negligible. Behavioural simulations show that the RTI offset of the first integrator results directly in a converter offset, while a 10 mV offset of the second integrator causes a converter offset of 29.56 µV, due to the finite DC gain of the

amplifiers.

System-level chopper technique is implemented at $f_{ch} = 2B_W$, replacing the standard integrator model with the FCI model shown in Fig. 2.25-a. The effective resolution of the chopped modulator is 17.33 (from the analytical model it is 17.5 bits), while the residual offset is lower than the Least Significant Bit. Even if the CHS is applied at low frequency, the increase of resolution and accuracy is evident also from Fig.2.26: the PSD of the output bitstream applying CHS results to be flat and lower than the PSD of the standard modulator. The ripple offset at f_{ch} and at odd-order harmonics is rejected by the notch response of the CIC filter. Fig. 2.27-a shows the ENOB of a standard Δ-Σ modulator estimated from MS simulations performed at different flicker corner frequencies, compared with the theoretical curve. Fig.2.27-b shows the converter effective resolution as a function of the chopper frequency: for high frequencies, we obtain the same resolution (18.55 bits) as in Fig. 2.27-a without flicker noise, i.e. flicker noise is effectively rejected. It is worth noting that the resolution growth, thanks to system-level CHS, is evident even for low chopper frequencies, avoiding a significant onset of residual offset due to the charge injection from the modulator switches and making it feasible as stand-alone technique. Preliminary measurements on a silicon prototype confirm the effectiveness of the System-Level Chopper technique for offset rejection (see paragraph 2.4).

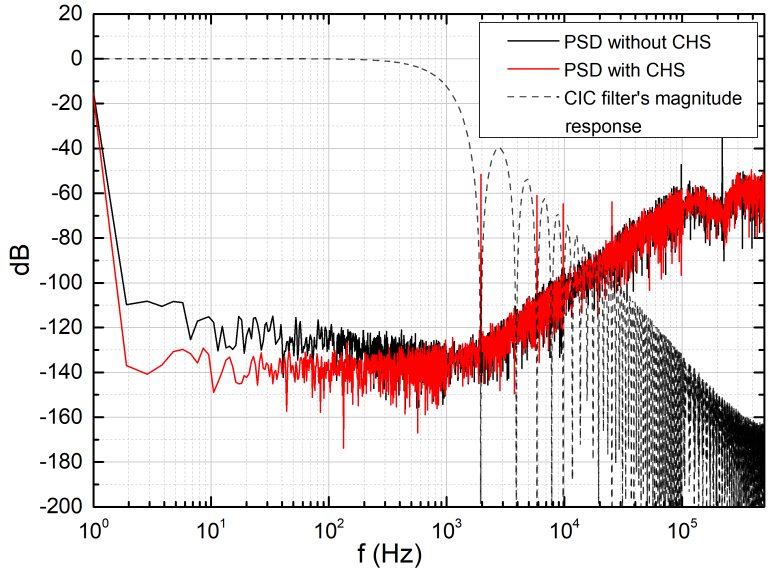


Figure 2.26: *PSD of the modulator output applying system-level CHS at f_{ch}=f_S/OSR, without CHS and magnitude response of the employed CIC filter.*

System-Level Chopper for Electrochemical Impedance Spectroscopy

The proposed Δ-Σ is designed for sensor interfacing applications. In particular, it is optimized for low-frequency signal conversions, as required for the acquisitions from thermal sensors [59], sensors based on thermal principles [60] or electrochemical/biomedical sensors [61]. For the latter categories, the typical acquisitions techniques are potentiometric sensing [62], amperometric sensing [63] or (EIS) [64]. While the first two are related to the readout of dc signals, EIS is based on the sinusoidal stimulus of a Device

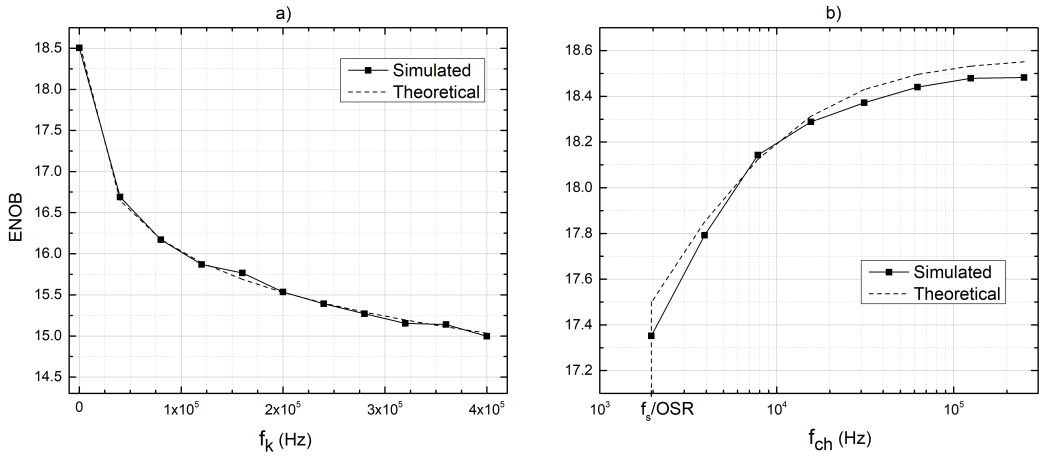


Figure 2.27: *Comparison between simulated and theoretical ENOB varying: a) flicker noise corner frequency of the amplifier; b) chopper frequency.*

Under Test in order to measure the real and imaginary part of its impedance. For example, applying a sinusoidal differential voltage at a fixed frequency on the DUT, from the readout of the current flowing in the DUT, we can obtain the amplitude and the phase shift related to the DUT impedance at the stimulus frequency. Sweeping the frequency of the sinusoidal stimulus in the interested range, we will obtain the information on the frequency behaviour of the DUT impedance. A typical approach in EIS consists in two lectures after the stimulus of the DUT at a certain frequency. Demodulating the sensed current with a square-waveform at the same frequency of the input stimulus, first in phase and then in quadrature, it is possible to obtain the information on the real part and imaginary part of the generic impedance from the mean value of the demodulated signals. A block diagram of the described EIS interface is shown in Fig.2.28. A high-resolution low-pass ADC (typically a Δ-Σ ADC) is employed, preceded by an anti-alias filter, in order to remove the even-order harmonics generated after the demodulation and extracting only the information about the mean value. Depending on the frequencies of interest for the impedance analysis, the design of the anti-alias filter can be extremely expensive in terms of area consumption. Furthermore, offset and low-frequency noise of the ADC can heavily affect the resolution of the whole system.

Introducing the above mentioned system-level CHS to reject offset and flicker noise of the converter, the modified block diagram of the EIS readout interface is the one shown in Fig.2.29-a. If the chopper signal Ch of the ADC coincides with the demodulation signal m(t), it is possible to suppress the first two demodulators (Fig.2.29-b) and send the sinusoidal signal directly to the modified Δ-Σ modulator, implementing the FCIs. The demodulation is fulfilled in the digital domain after the conversion. This technique allows the reduction of the system complexity, removing the input demodulation in the analog domain, which may introduce undesired artefacts, and relaxing the specifications of the analog anti-alias filter.

Fig.2.30 shows the effectiveness of the proposed solutions by means of electrical simulation with Spectre in Cadence environment on the designed converter. Simulations with two different input signal frequencies and different amplitudes are performed, in the case of in-phase demodulation. The output of the CIC filter represents

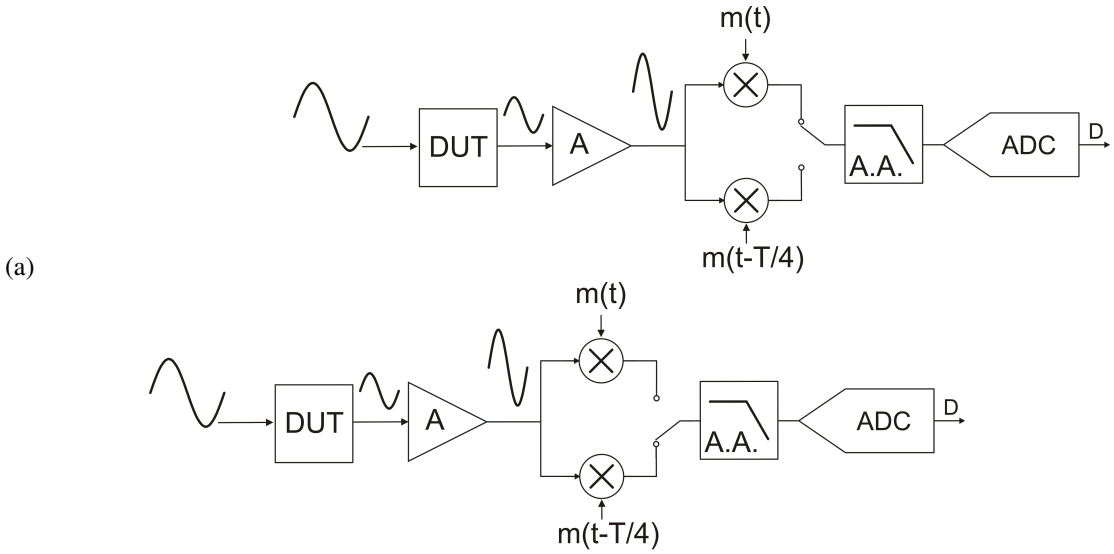


Figure 2.28: *Block diagram of the impedance spectroscopy readout to measure the DUT a) phase-component and b) quadrature component.*

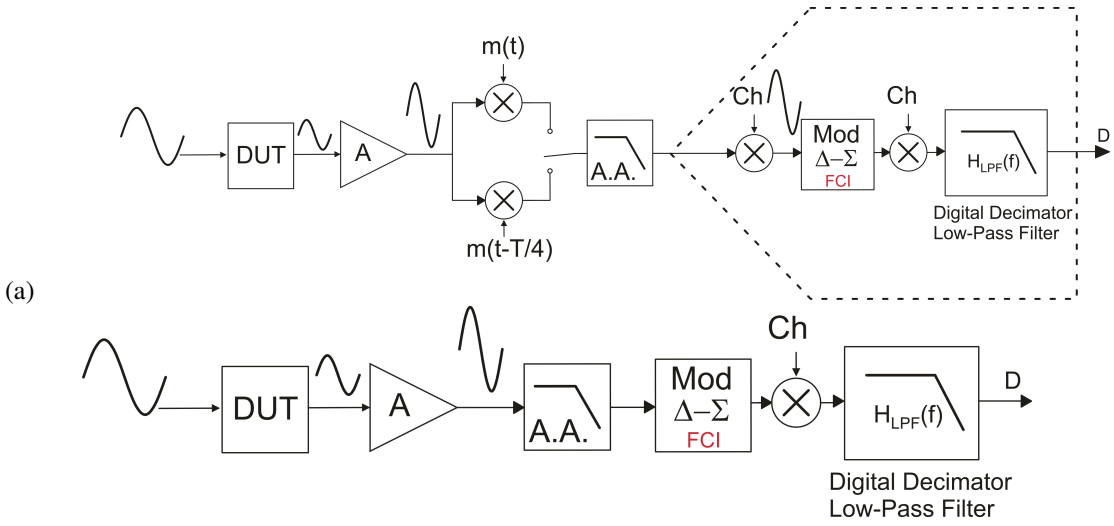


Figure 2.29: *a) Impedance spectroscopy readout with system-level chopper technique applied to the Δ-Σ. b) Impedance spectroscopy readout embedded with system-level chopper technique*

correctly the amplitude of the input signals (multiplied for a factor $2/\pi$, which is the first coefficient of the Fouries series of the square waveform used for demodulating the sinusoidal signal), not affected by converter offsets.

2.3.5 Slew-rate enhancement

Another error not discussed so far is the settling time error of the first integrator. Due to the limited gain-bandwidth product and slew-rate of the amplifier, detrimental effects

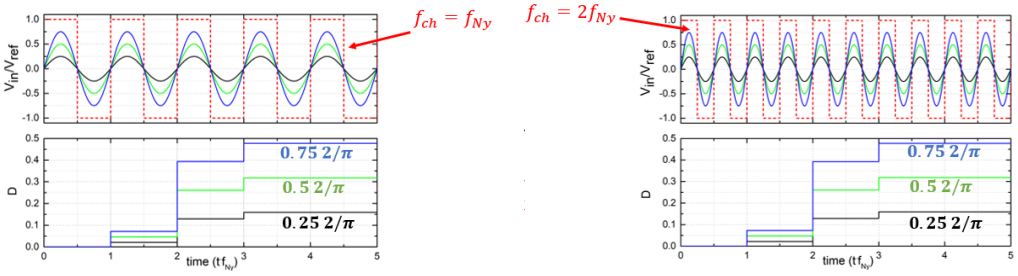


Figure 2.30: *(a) In the upper graph: input sinusoidal signals at $f_{in} = f_{ch} = f_{Ny}$ with different amplitudes. In the lower graph: relative output codes from the converter. (b) In the upper graph: input sinusoidal signals at $f_{in} = f_{ch} = 2f_{Ny}$ with different amplitudes. In the lower graph: relative output codes from the converter.*

on the converter resolution could arise. Several works try to analyse this effect ([41, 65–67], mainly with high-level descriptions and behavioural simulations. As for noise and offset contributions, also non-linearities of the integrator affect the whole converter performances, while contributions from the other blocks result in second order effects.

Depending on the amplitude of the differential signal that has to be integrated, the amplifier could present a linear behaviour (i.e. with the typical exponential transient, as for pole dominant amplifier) or non-linear behaviour, with part of the transient in slew-rate regime. If the amplifier would not suffer of finite slew-rate, then the problem of finite gain-bandwidth product would be reflected only in an attenuation of the coefficient a_1 with respect to the nominal value, due to the incomplete settling of the output voltage. In this case, no distortions would be added, but only a variation of the effective coefficient, which typically leads to slight modifications of the NTF, i.e. to small increase of the final quantization noise power. A more critical effect is present when also slew-rate transients are present (depending on the amplitude of the input voltage), which introduce converter distortions.

To better understand this behaviour, it is worth looking at the commutation from phase 1 to phase 2 depicted in Fig.2.31. Passing from a certain input voltage to the feedback voltage, the left nodes of the sampling capacitors are affected by an instantaneous variation of the voltage (assuming ideal switches and transitions), which is reflected at the input and at the output of the amplifier, due to the high-frequency feedforward path represented by the capacitor $C_S^{+,-}$ and $C_F^{+,-}$. The amplifier will respond, depending on the amplitude of the input voltage variations, either with an initial slew-rate transient followed by an exponential settling, or a whole exponential or a complete slew-rate settling.

The following analysis aims to obtain a general expression of the integrator settling time as a function of the main design parameters of the operational amplifier. The effects of not completed settling on the Δ-Σ converter performances can be evaluated by means of behavioural simulations of the modulators, once obtained the expression of the settling error as a function of the input voltage. For a simpler analysis, it is worth considering a single-ended implementation of the parasitic-insensitive integrator (the results can be easily generalized for the fully-differential circuit), as the one in Fig.2.32.

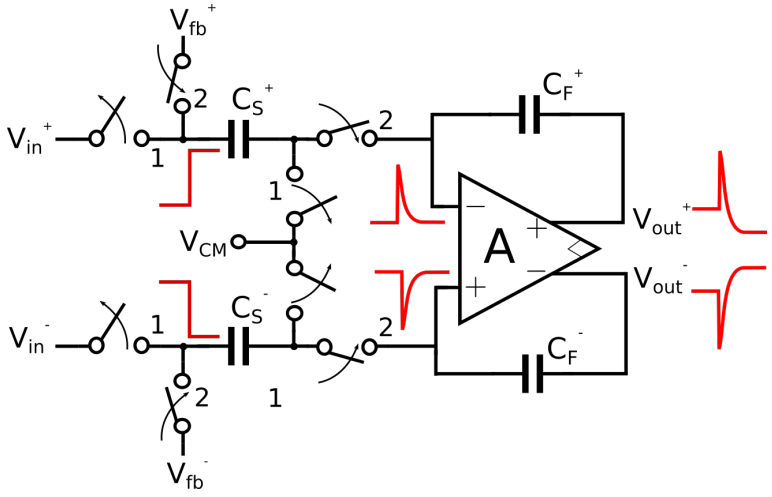


Figure 2.31: *Example of a commutation from phase 1 to phase 2, with the relative waveforms at the input of the integrator, the input of the operational amplifier and at the integrator output.*

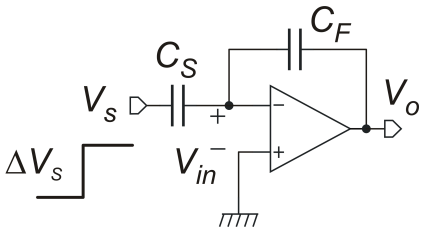


Figure 2.32: *Schematization of the problem as a voltage input step for the inverting amplifier with a capacitive feedback network.*

The circuit represented in Fig.2.32 can be used to model the transient corresponding to a charge transfer operation from capacitor C_S to capacitor C_F. We consider that at the instant $t = 0$, the input voltages is subjected to a step of magnitude ΔV_S.

The initial condition for $t < 0$ is:

$$\begin{cases} V_S = 0 \\ V_{in} = 0 \\ V_o = V_{oQ} \end{cases} \tag{2.22}$$

In the instant just after the commutation from phase 1 to phase 2, i.e. after the application of the step at $t = 0$ in Fig.2.32, we have:

$$\begin{cases} V_S \equiv V_S(0) = \Delta V_S \\ V_{in} = V_{in}(0) = \Delta V_S \\ V_o = V_o(0) = V_{oQ} + \Delta V_S \end{cases} \tag{2.23}$$

For charge conservation:

$$\{[V_o(t) - V_o(0))] - [V_{in}(t) - V_{in}(0)]\} C_F = \{[V_{in}(t) - V_{in}(0)] - [V_S(t) - V_S(0))]\} \tag{2.24}$$

Since $V_S(t)$ does not vary for any $t > 0$, then $V_S - V_S(0) = 0$. Solving 2.24 with this consideration and taking into account 2.23 for $V_o(0)$ and $V_{in}(0)$ we find:

$$[V_o(t) - V_{oQ} - V_{in}(t) - \Delta V_S]\, C_F = [V_{in}(t) - V_{in}(0)]\, C_S \tag{2.25}$$

which becomes:

$$V_o(t) - V_{oQ} = -\Delta V_S \frac{C_S}{C_F} + V_{in}(t) \frac{C_S + C_F}{C_F} \tag{2.26}$$

Note that the term:

$$\Delta V_o(\infty) = -\Delta V_S \frac{C_S}{C_F} \tag{2.27}$$

Is the asymptotic voltage increment that V_o undergoes, with respect to the initial value of V_{oQ}, after an infinite time. Therefore, we can write the residual error on the output voltage as:

$$V_{\epsilon o}(t) = V_o(t) - V_{oQ} - \Delta V_o(\infty) = V_{in}(t) \frac{C_S + C_F}{C_F} \tag{2.28}$$

Since the input voltage asymptotically sets to zero (virtual short circuit), at any time we can relate the residual error on V_{in} ($V_{\epsilon in}$) to the residual error on V_o:

$$V_{\epsilon in}(t) = V_{\epsilon o}(t) \frac{C_F}{C_S + C_F} \tag{2.29}$$

The transient in V_{in} and V_{out} are represented in Fig.2.33.

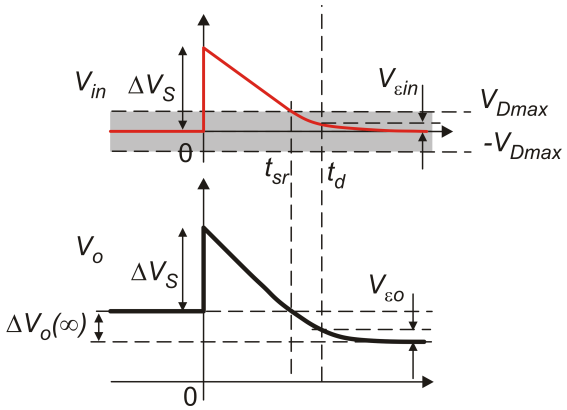


Figure 2.33: *Amplifier input and output voltage during transient. First, the slew-rate behaviour (for $t < t_{sr}$) and then the exponential transient (for $t > t_{sr}$) can be noticed.*

The interval up to t_{sr} is spent by the amplifier in slew rate, i.e. its output current saturates at a constant value indicated with I_{omax}. In the slew rate period, we can write:

$$\frac{dV_o}{dt} = \frac{I_{omax}}{C_L} = I_{omax} \frac{C_S + C_F}{C_F C_S} \tag{2.30}$$

where C_L is the series of C_F and C_S. Relating to V_{in} through 2.28, we get:

$$\frac{dV_{in}(t)}{dt} = \frac{dV_o(t)}{dt}\frac{C_F}{C_F + C_S} = \frac{I_{omax}}{C_S} \tag{2.31}$$

We suppose that the amplifier instantaneously re-enters in linear region when V_{in} gets lower than V_{Dmax}. Then, t_{sr} can be approximated by:

$$t_{sr} = (\Delta V_S - V_{Dmax})\frac{C_S}{I_{omax}} \tag{2.32}$$

As far as the linear part of the settling time is concerned (t_{lin}), we can consider that, just after the slew rate period, the amplifier starts a linear transient marked by a single pole $\omega_{op} = 1/\tau$, that coincides with the zero-db angular frequency of the feedback loop. Then:

$$\omega_{op} = \frac{1}{\tau} = \frac{G_m}{C_L}\frac{C_F}{C_S + C_F} = \frac{G_m}{C_S} \tag{2.33}$$

where G_m is the effective transconductance of the single-stage amplifier, defined as the ratio of the output current (I_o) over the input voltage (V_{in}). The linear component of the settling time is then given by:

$$t_{lin} = \tau ln\left(\frac{V_{Dmax}}{V_{\epsilon in}}\right) \tag{2.34}$$

where $V_{\epsilon in}$ is the tolerable residual error at the amplifier input at the end of the clock phase ($t = T_S/2$), which is tied to the tolerable output error by 2.28. We can conveniently express the residual output error $V_{\epsilon o}$ through the relative error (ϵ_R) with respect to the ideal integrator increment given by 2.27. Then we can write:

$$t_{lin} = \tau ln\left(\frac{V_{Dmax}}{V_{\epsilon o}}\frac{C_F + C_S}{C_F}\right) = \frac{C_S}{G_m} ln\left(\frac{V_{Dmax}}{\Delta V_S}\frac{1}{\epsilon_R}\frac{C_F + C_S}{C_F}\right) \tag{2.35}$$

The linear time constant can be related to the amplifier properties by 2.33, where the G_m can be written as a function of the input MOSFET transconductance g_{m1} through the parameter k_G.

$$G_m = k_G g_{m1} = k_G \frac{I_{D1}}{V_{TE1}} \tag{2.36}$$

where I_{D1} and V_{TE1} are the drain current and the effective thermal voltage[4] of the input MOSFETs, respectively. We can introduce the following parameters:

$$r = \frac{I_{supply}}{I_{D1}} \qquad \alpha = \frac{I_{omax}}{I_{supply}} \qquad \gamma = \frac{V_{Dmax}}{V_{TE1}} \tag{2.37}$$

And write the total time $t_{tot} = t_{lin} + t_{sr}$ as:

[4]The effective thermal voltage of a MOSFET is defines as the inverse of its g_m/I_D ratio. A MOSFET biased in saturation region has an effective thermal voltage equal to:

$$V_{TE} = \frac{I_D}{g_m} = \begin{cases} \frac{V_{GS}-V_{th}}{2} & \text{strong inversion} \\ nV_T & \text{weak inversion} \end{cases}$$

where n is the subthreshold slope factor.

$$t_{tot} = \frac{C_S}{I_{supply}} \frac{rV_{TE1}}{k_G} ln\left(\frac{V_{Dmax}}{\Delta V_S} \frac{1}{\epsilon_R} \frac{C_F + C_S}{C_S}\right) + \frac{C_S}{I_{supply}} \frac{1}{\alpha} (\Delta V_S - V_{Dmax}) \quad (2.38)$$

It is useful to define the following parameters:

$$k_V = \frac{\Delta V_S}{V_{Dmax}} \quad (2.39)$$

In this analysis it is implicit that the input step ΔV_S is large enough to make the amplifier leave the linear operating region, thus $\Delta V_S > V_{Dmax}$ and $k_v > 1$. If $\Delta V_S < V_{Dmax}$ ($k_V < 1$), only linear settling will be present and expression 2.35 can be employed. Then, using 2.39, the total settling time expression can be written as:

$$t_{tot} = \frac{\Delta V C_S}{I_{supply}} \frac{r}{\gamma k_V k_G} \left[ln\left(\frac{1}{k_V} \frac{1}{\epsilon_R} \frac{C_F + C_S}{C_S}\right) + \frac{1}{\alpha}\left(1 - \frac{1}{K_V}\right)\right] \quad (2.40)$$

It is worth recaping all the parameters introduced, with a brief description of their meaning:

- α is the main parameter to model the slew rate efficiency of the amplifier. The larger is α, the larger is the maximum output current for a given static supply current.

- k_V measures the magnitude of the input step with respect to the input linearity range of the amplifier (V_{Dmax}). For quick evaluations of the integrator settling time, it can be set equal to the worst case value: $max(\Delta V_S)/V_{Dmax}$. Note that k_V is affected also by the amplifier sizing (in particular, of the input devices), through the parameter V_{Dmax}.

- k_G measures the effectiveness of the amplifier topology in delivering high G_m from the same transconductance of the input devices. Multiplying current mirrors or recycling topologies result in $k_G > 1$.

- r takes into account the overhead of supply current with respect to the sole contribution of the input devices. Multiplying current mirrors increases k_G and r together, so that the final effect in terms of linear settling times is negligible. Recycling topologies are more effective in this respect [68].

- γ relates the linear input range (V_{Dmax}) to the effective thermal voltage V_{TE}, defined as the reciprocal of the transconductance efficiency (g_m/I_D) of the input devices.

- $(C_S + C_F)/C_S = 1 + A^{-1}$, where $A = C_S/C_F$ is the discrete time integrator gain $=|\Delta V_{out}/\Delta V_S|$. In Δ-Σ modulators, we can have $A << 1$ (e.g. A=0.1), then the $(C_S + C_F)/C_S$ factor can be rather larger than 1, resulting in longer settling times.

Behavioural simulations

The following simulations have been performed for a FD amplifier with $k_G = 1$ (typical case) and $k_G = 2$ [68]. Residual error was set to $2 \cdot 10^{-5}$ (20 ppm), which has been verified (through MS simulations) to be low enough to guarantee 17 bit of ENOB for a 2nd order Δ-Σ modulator. In Fig.2.34, we have investigated the effect of k_v. We imagine starting with a (large) input voltage step ΔV_S (e.g. 2 V) and then imagine varying V_{dmax}, changing the V_{TE} of the input devices. A large k_V means small V_{Dmax} (and then, since γ is fixed, small V_{TE}, i.e. a large transconductance effectiveness). With $\Delta V_S = 2V$, a maximum k_V of 20 (V_{Dmax}=100 mV) can be considered feasible. Results are normalized to the time $\Delta V_S C_S / I_{supply}$, which appears in 2.40. Note that, with fixed I_{supply}, C_S and input step magnitude, larger k_V (i.e. small V_{Dmax}) are always convenient. This seems in contrast with the common opinion that a large input range mitigates the problem related to the slew rate. In fact, in single-stage amplifiers, the higher transconductance effectiveness associated with a small input range dominates.

Fig.2.35 shows the effect of the current efficiency (parameter α) on the settling time. For very high α values, the slew rate time becomes more and more negligible and the settling time is dominated by the linear time. The asymptotic value is just the normalized linear time (first term in the square bracket of 2.40). It is important to observe that, to obtain a settling time only 30 % larger than the asymptotic value (max. operating frequency 30 % slower) it is sufficient $\alpha = 2.3$ for k_G=1, while $\alpha = 3.5$ is necessary for $k_G = 2$.

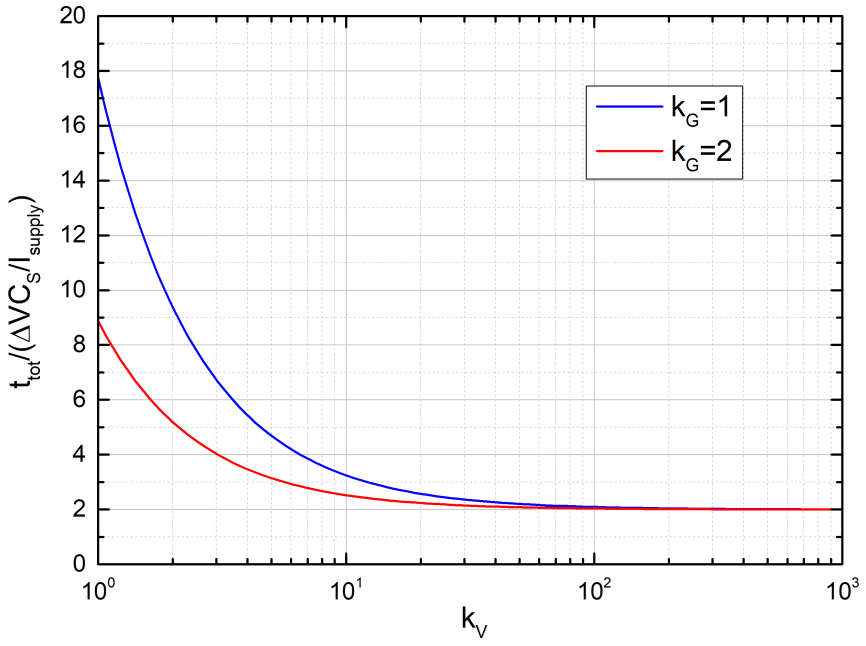


Figure 2.34: *Settling time as a function of the parameter k_V*

Popular solutions present in the literature ([68–72]) implements several techniques as current-recycling, flipped-voltage follower, current starving, non-linear current mirrors and dynamic biasing in order to reach improvements both for the slew-rate settling and the linear settling. All these techniques require modifications of the basic amplifier topology, acting on the same transistors which are crucial for offset and noise

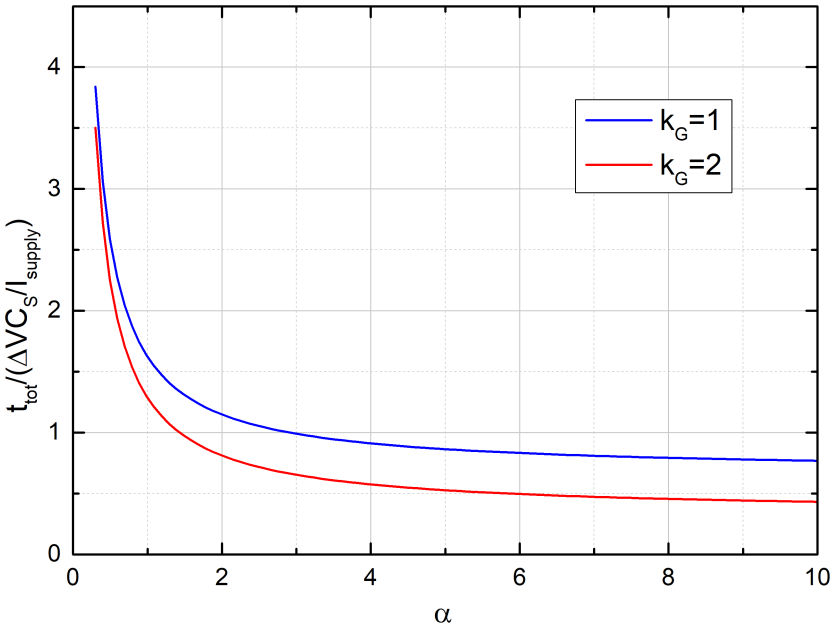


Figure 2.35: *Settling time as a function of the parameter* α

optimizations. The proposed solution, instead, employs an auxiliary circuit to enhance the amplifier slew-rate, without modifying the amplifier topology or transistor sizing, optimized for high dc gain and low noise.

Slew-rate enhancement circuit

We can assume the presence of an auxiliary circuit called Slew-Rate Enhancement (SRE), connected in parallel to the main amplifier and capable to supply a constant current I_{o-SRE} only during the slew-rate transient of the main amplifier and which turns off when the main amplifier is in the linear region. A possible schematization is the one of Fig.2.36.

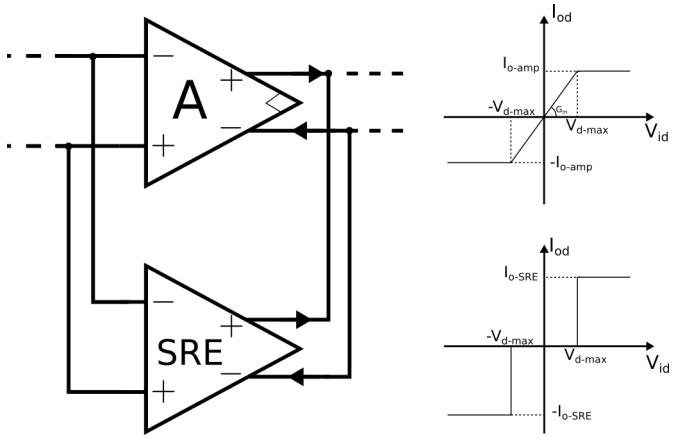


Figure 2.36: *Schematic view of the SRE circuit in parallel to the main amplifier A. On the right, the characteristics of differential output current as a function of the input differential voltage for the two blocks are represented.*

The insertion of SRE will reduce the slew-rate time, depending on its slew-rate efficiency (α_{SRE}) and its supply current ($I_{sup-SRE}$), with respect to the overall current consumption ($I_{sup-tot}$). It is worth defining the following parameters:

$$\alpha_{SRE} = \frac{I_{o-SRE}}{I_{sup-SRE}} \quad \eta = \frac{I_{sup-amp}}{I_{sup-tot}} \quad I_{sup-tot} = I_{sup-amp} + I_{sup-SRE} \tag{2.41}$$

α_{SRE} represents the equivalent of the parameter α previously defined for the main amplifier, here adapted for the SRE circuit. η represents the current budget allocated to the amplifier with respect to the overall current consumption.

In the next analysis, we will start from 2.40, replacing I_{supply} with $I_{supp-tot}$. The overall current consumption is the same as before, but the current consumption for the amplifier results lower, because of the addition of the SRE. The ratio between $I_{sup-tot}$ and I_{D1} is then simply r/γ, with r and γ the same as before.

The slew-rate efficiency of the overall circuit (main amplifier plus SRE) can be defined as:

$$\alpha_{tot} = \frac{I_{o-amp} + I_{o-SRE}}{I_{sup-tot}} = \eta \left[\alpha + \alpha_{SRE} \left(\frac{1}{\eta} - 1 \right) \right] \tag{2.42}$$

Note that if $\eta = 1$, then $\alpha_{tot} = \alpha$ and the following analysis converges to the previous one.

The expression of the total settling time of 2.40 can be briefly expressed as:

$$t_{tot} = \frac{\Delta V C_S}{I_{sup-tot}} (a + b) \tag{2.43}$$

Where a represented the contribution related to linear transient, while b the contribution related to the slew-rate transient (both parameters are easily obtained from expression 2.40). With the insertion of the SRE, the expression of the total settling time becomes:

$$t_{tot-SRE} = \frac{\Delta V C_S}{I_{sup-tot}} \left(\frac{a}{\eta} + b \frac{\alpha}{\alpha_{tot}} \right) = \frac{\Delta V C_S}{I_{sup-tot}} \left[\frac{a}{\eta} + \frac{b}{\eta} \frac{1}{1 + \frac{\alpha_{SRE}}{\alpha} \left(\frac{1}{\eta} - 1 \right)} \right] \tag{2.44}$$

Considering that $I_{sup-tot}$ is equal to I_{supply} of 2.40 in the case of no SRE employed, it is possible to compare 2.44 with 2.40. The linear time is increased by a factor $1/\eta$ (η is lower than 1), because part of the previous I_{supply} is now budgeted to the SRE circuit, while a straightforward conclusion about the slew-rate time cannot be drawn. For $\eta = 1$, we have the same conditions of 2.40. For $\eta = 0$, we have infinite linear time and a slew-rate time decreased by the factor α_{SRE}/α. The SRE circuit can be designed to have α_{SRE} on the order of few tens (as in [73]), while it does not need to be designed for noise, gain or offset optimization. Typical single-stage amplifiers as folded-cascode or telescopic cascode, for example, shows $\alpha <= 1$. In this way, it could be very easy to obtain values of b higher than a, i.e. the slew-rate time is longer than the linear one. Once known the values of a and b, and chosen the SRE circuit with the proper α_{SRE},

the total settling time with SRE is lower than without SRE, if the following condition is verified:

$$\frac{1-\eta}{\eta\left[1+\frac{\alpha_{SRE}}{\alpha}\left(\frac{1}{\eta}-1\right)\right]-1} < \frac{b}{a} \tag{2.45}$$

If this condition is true, it is possible to find an optimum value of η depending on b,a and α_{SRE}/α.

One possible implementation of a slew-rate enhancement circuit is the one proposed in ([73]) and depicted in Fig.2.37. In order to have no differential current for small input differential voltages and very high output currents for a differential voltage larger than a certain value, the following operating principle is exploited. The tail MOSFET M0 is sized with a current $2I_1$. For a zero differential input signal, half of the tail current flows in M1 and half in M2. Bias voltage V_a and sizing of M3-M4 is such that their nominal current should be I_2, with the condition: $I_2 > I_1$ and $I_2 < 2I_1$. Because of these conditions, in the bias point (with no differential input signal), M3 and M4 are in triode regions and their drain voltages are close to V_{dd}. Then, M5 and M6 are off and no output current flows. When a differential input signal large enough to unbalance completely the input differential pair is present, all the tail current $2I_1$ flows in one of the two branches (depending on the sign of the input of the differential pair). As a result, M3 or M4 enters in the saturation region and the drain voltage decreases, turning on the relative output devices and sinking or sourcing a certain output current, depending on their sizing.

Sizing the input pair of the SRE such that their V_{dmax} is the same as for the main amplifier, the SRE increases the overall current and it turns off during linear operations of the main amplifier. In this way, no effects of the SRE on the final value are present, so that only accuracy and noise of the main amplifier affects the system performances.

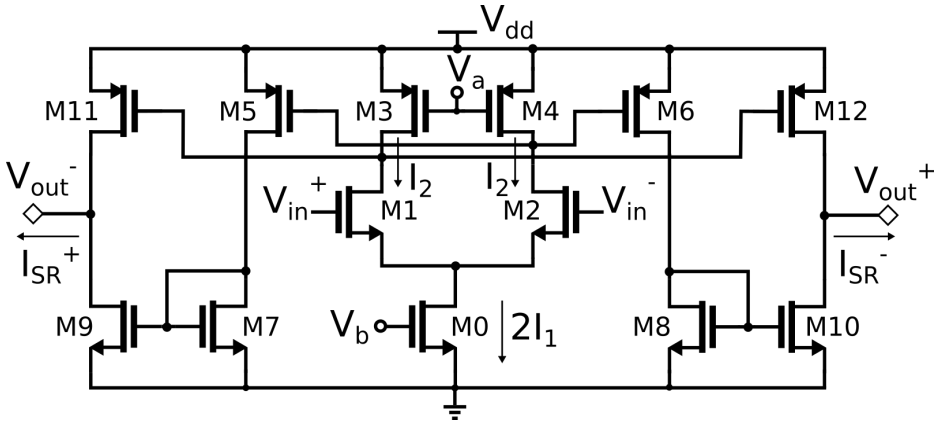


Figure 2.37: *Schematic view of the slew-rate enhancement circuit proposed in [73].*

The circuit of Fig.2.37 presents some drawbacks during the turn-on and turn-off transients, due to the speed of the mirroring operations through M7-M9 and M8-M10. A delay in the turning-on of the SRE circuit will reduce the benefits of this additional circuit because of the delay in providing an higher current. On the other hand, a delay in turning-off may cause overshoot of the output current and then additional delay in

the settling time. A possible modification presented in [73] employs two different input pairs to detect the two different possible crossing of the input differential voltage, removing the mirror path present in Fig.2.37. Additional diode connected MOSFETs as M5,M6 and M14,M15 (Fig.2.38) limit the maximum swing of the output current, limiting also the possible overshoot of the output voltage. Anyway, the presence of the mirroring of M5-M7, M6-M8, M14-M16 and M15-M17 can slow down the turning on transients, especially for high current mirror ratios. For this reason, a capacitor C has been added between the sources of the two input differential pairs, as depicted in Fig.2.38. When a fast variation of the input differential voltage is present, as the one shown in Fig.2.31, also a rapid variation on the voltage across the capacitor will generate a large current flow C, which will turn on quickly the mirror branches and the output devices, reducing the turn-on transient. Large values of the capacitor C will increase the instantaneous current, but they will also require a greater time to recharge the capacitor during the steady-state period. A careful sizing of the capacitor C, verified by eans of electrical simulations, is then requested.

Electrical simulations performed on the parasitic-insensitive integrator for very large input swing, with and without the slew-rate enhancement circuit, are shown in Fig.2.39. It is possible to appreciate the benefits in slew-rate increasing thanks to the additional SRE circuit, especially with the proposed modification. The slew-rate improvement in the case of SRE of [73] compared to case with only folded-cascode, is around 1.6 times, at the cost of an increase of current consumption of 10%. The proposed solution increases the slew-rate with respect to [73] of 3.3 for the same power consumption, thanks to the additional capacitor which is able to provide a large impulsive current at the very transitions, reducing heavily the turn-on transient of the SRE circuit.

Fig.2.40 shows the robustness of the proposed technique to Monte Carlo variations, including both global and local variations. With this kind of circuit, it is pivotal to guarantee the proper starting of the circuit in presence of large input signal, as well as the correct turning off when the circuit has almost reached the final steady-state. The slope of the output voltage is always very steep in all the Monte Carlo realizations; the difference among the initial and the final values of the different runs depend on the presence of a different initial state of the integrator.

2.4 Measurement results

A prototype of the described Δ-Σ converter has been realized with the 0.18 μm CMOS process of UMC. The final layout is shown in Fig.2.41, where the dimensions of the whole modulator are highlighted. The test-chip is a 1525 μm x 1525 μm miniASIC, which includes several auxiliary blocks to improve the accuracy of the characterization. First, there is a digital finite state machine (FSM) to increase the programmability of the ADC. The clock signals are all generated as a division of the relaxation oscillator present on the chip, working at 11 MHz. The dividers for the different clock signals (the oversampling clock, the chopper clock, the CMFB clock), as well as the different enable signals, are programmable by the user. A Python-based software sets the registers of the FSM of the chip by means of an additional USB-to-SPI/I2C interface. All the bias voltages and the reference voltages for the ADC are generated internally. The third order CIC filter is embedded in the digital machine and the filter output data have been

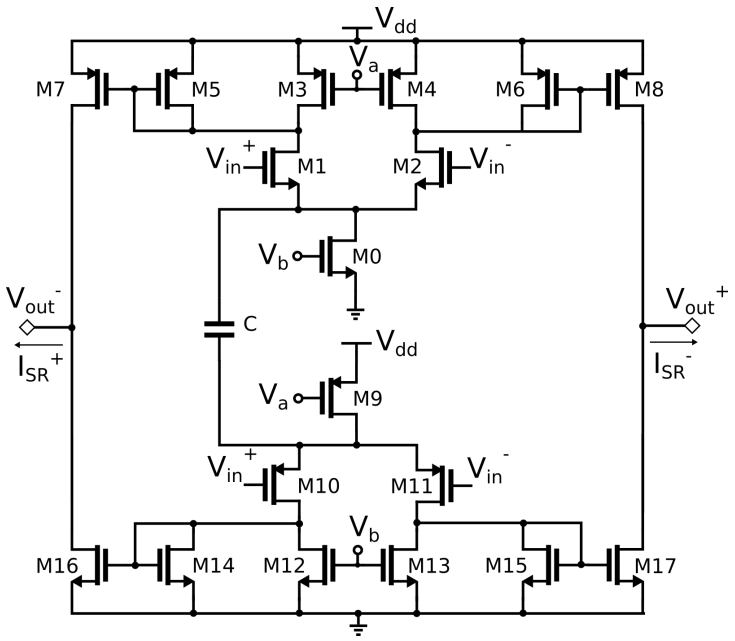


Figure 2.38: *Schematic view of the proposed slew-rate enhancement circuit.*

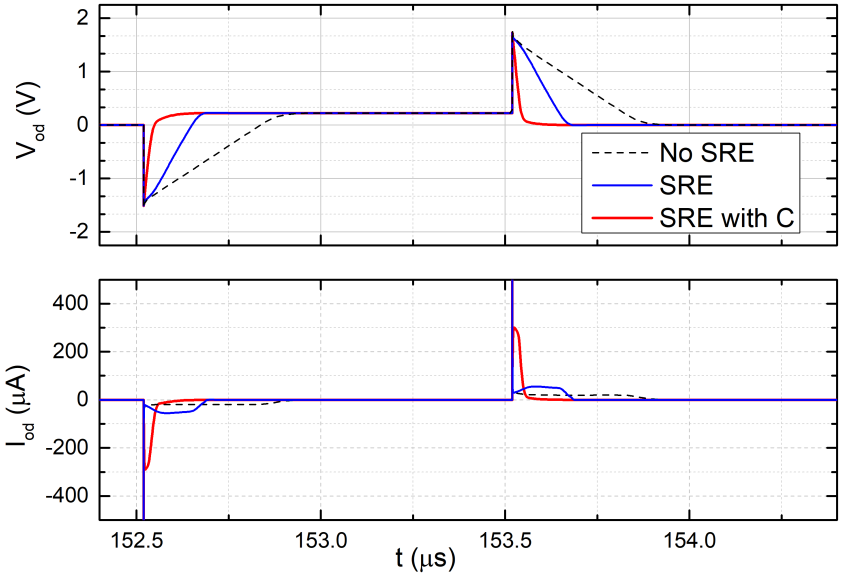


Figure 2.39: *Comparison of differential output voltage (upper graph) and differential output current (lower graph) without SRE circuit (only folded-cascode amplifier), with SRE circuit of [73] and with the proposed modification of Fig.2.38.*

used for the dc characterization; the oversampling ratio is programmable via software. The output bitstream of the modulator has been routed to an external pad, together with the oversampling clock, and acquired by means of a digital oscilloscope. The data are then processed by a MATLAB software used to calculate the spectra and the dynamic

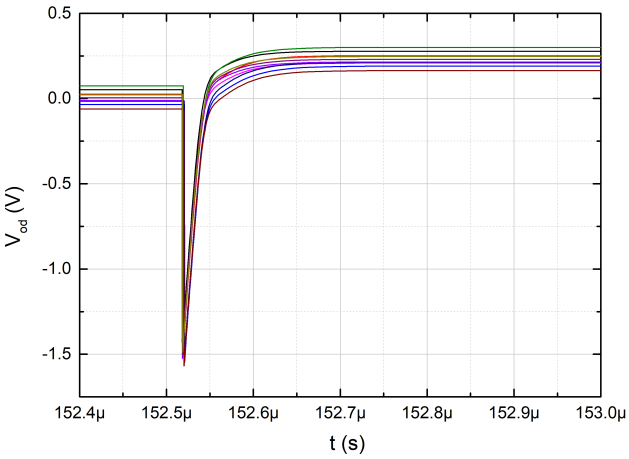


Figure 2.40: *Differential output voltage of 10 Monte Carlo runs of the proposed SRE circuit.*

parameters as SNR, SINAD, THD...

The chip has been placed in a JLCC44-holder in a general-purpose PCB designed with KiCad free software and fabricated by means of a consolidated production stream of FR4 substrate. Fig.2.42 is a picture of the basic measurement set-up. The board on the left is responsible for the communication with the personal computer (from USB to SPI/I2C). It provides also the supply to the board on the right, which is the general purpose board with the holder for the test-chip.

For the specific characterization of the proposed ADC, because of the differential input of the ADC, a custom electronic system for the conversion from the single-ended signals provided by the bench instrumentations has been used.

Preliminary measurements have been done in order to estimate the performances of the circuit, focusing on the characterization of the dc performances. Further measurements will be done to fully-characterize the converter in all the possible configurations.

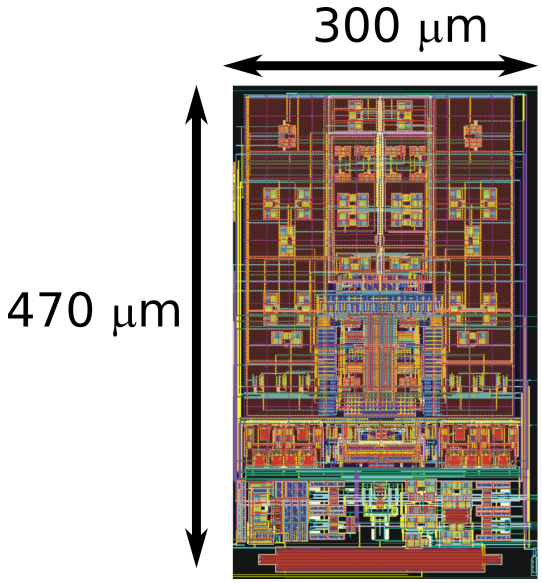


Figure 2.41: *Layout of the converter prototype designed in UMC 0.18* µm *CMOS process.*

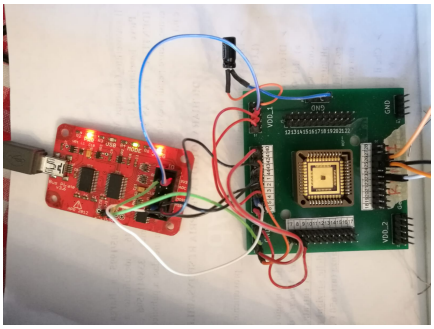


Figure 2.42: *Picture of the test-chip measurement setup.*

2.4.1 Dc Characteristics

The first measurements concern the dc characterization for different configurations, with a supply voltage of 3.3 V and $V_{ref} = V_{dd}$. First, the dc characteristic with a sampling frequency of 1 MHz, an OSR of 1024, without any chopper technique is shown in Fig.2.43. A comparison with the dc characteristics with the internal chopper on and with the system-level chopper on are shown in figs. 2.44 and 2.45, using for both techniques a chopper frequency of 3.9 kHz. Not very useful information can be obtained from the full-scale range characteristic, due to the high number of bit that we are targeting. For this reason, more details about the converter offset, gain and integral non-linearities are shown in the next paragraphs.

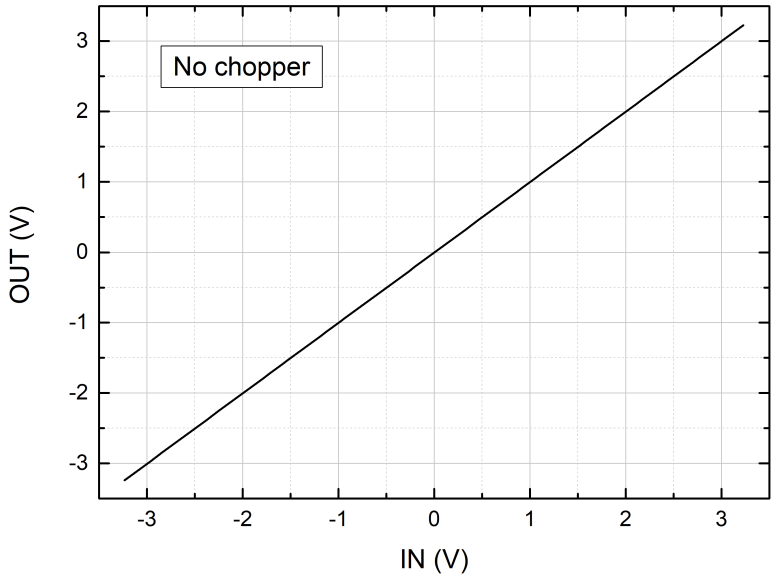


Figure 2.43: *Converter DC characteristic without any chopper technique.*

Offset and noise

In order to deeply characterize the offset performance of the converters, the short-circuit of the input differential voltage has been implemented directly on chip, providing the proper common-mode equal to half of the supply voltage. In Fig.2.46, the variation of

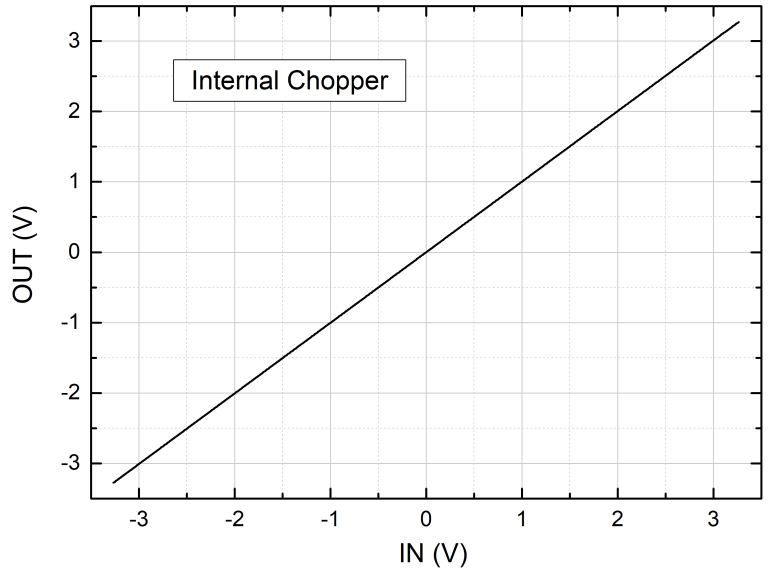


Figure 2.44: *Converter DC characteristic with the internal chopper on.*

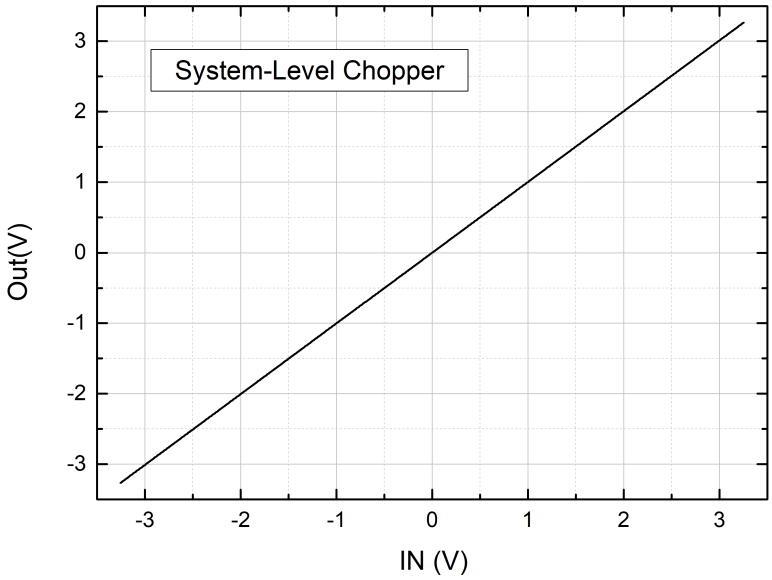


Figure 2.45: *Converter DC characteristic with the system-level chopper on.*

the offset and the noise standard deviation of the output voltage after multiple acquisition has been plotted, sweeping the OSR. The output code is converted in voltage, multiplying it for the quantization step Δ. The offset of the modulator is quite large, on the order of -2.5 mV, without turning on any chopper technique. It is worth noting how the noise standard deviation initially decreases very sharply every doubling of OSR. In that regime, quantization noise is limiting the converter resolution, and a doubling of the OSR means an increase of the resolution of 2.5 bit (due to the second order noise shaping), i.e. a decrease of σ of a factor 5.6. For further increase of the OSR, a smoother decrease of the σ is present, being in the region where the resolution is limited by the thermal noise. There, every doubling of OSR, only a resolution increase of

0.5 is gained, due to the oversampling effect. Converter offset, obviously, does not vary with the oversampling ratio, a part from statistical fluctuations.

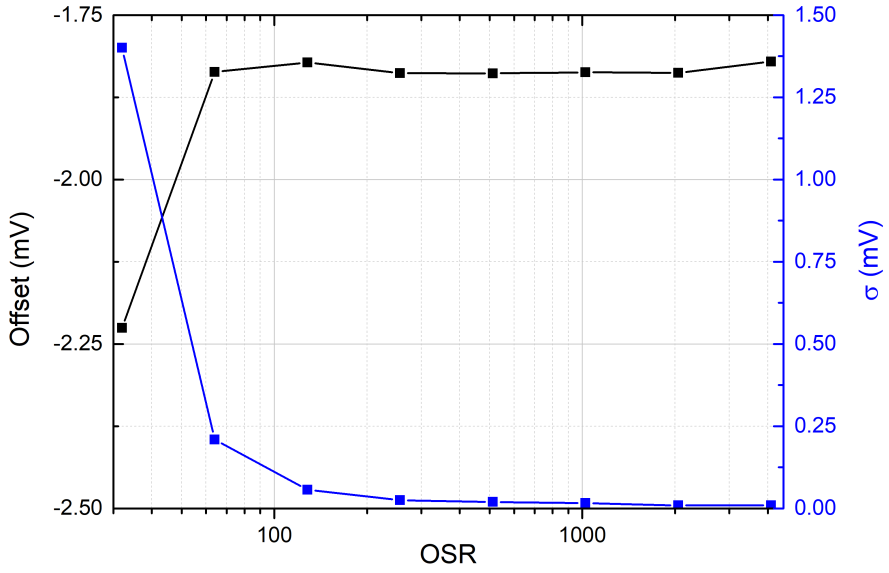


Figure 2.46: *Converter offset and noise standard deviation, sweeping the OSR.*

In Fig.2.47, the performances of the internal chopper modulation technique are shown. The comparison of offset and noise standard deviation, varying the ratio k between the oversampling frequency and the chopper frequency (keeping the oversampling frequency constant, i.e. sweeping the chopper frequency), for different oversampling ratios are plotted. A value of offset around 250 µV shows the effectiveness of the chopper technique, even if that value of residual offset could be still limiting in high-accuracy applications. A $\sigma = 20\mu V$, for high values of k, guarantee an effective resolution[5] of 16 bits.

Similar measurements have been repeated also for the system-level chopper technique and plotted in Fig.2.48. An offset lower than 20 µV is guaranteed for every chopping frequency, proving the better performances of the system-level chopper technique, compared with the traditional CHS. Also the standard deviation noise approaches 15 µV with an OSR of 4096, which means an effective resolution higher than 16.5 bit.

Graphs in figs. 2.49 and 2.50 show the comparison of converter offset and noise standard deviation with and without the implementation of the two chopper techniques, for different factor k and two different OSR. The proposed system-level chopper technique shows better performances in terms of residual offset and almost comparable noise reduction, leading to the fulfilment of the target requirements. However, the arising of dead-zones have been measured for high chopper frequencies, as shown in Fig.2.51. The cause of this phenomenon is related to the parasitic capacitances of the switches which effectuate the periodic swapping of the integrating capacitors in the PI integrators. With high chopper frequencies, the equivalent resistance of the chopper demodulators affects heavily the amplifier dc gain of both the integrator, increasing the dead-zone amplitude. However, we need to investigate further this effect, because a

[5]For these dc measurements, the definition of noise-free resolution has been used to evaluate the effective resolution: $log_2(V_{FS}/(k\sigma_n))$, where k is two times the crest factor.

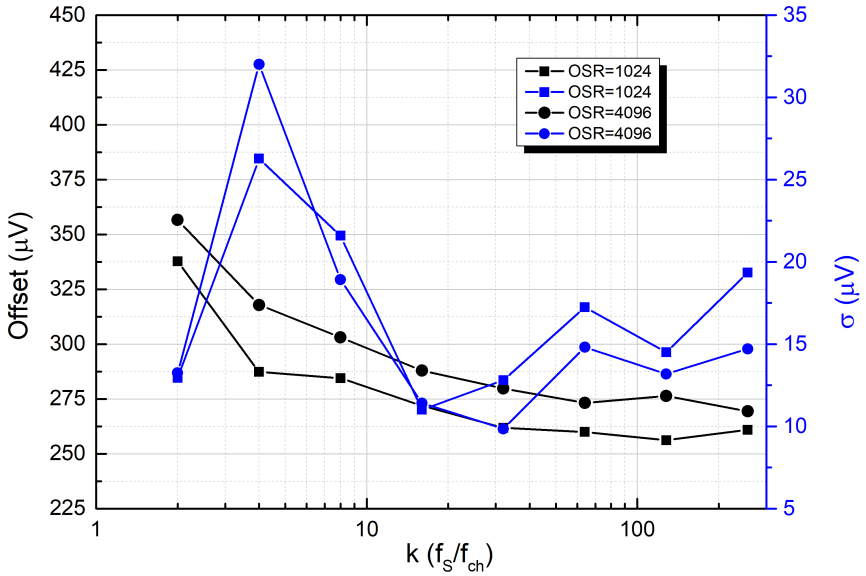


Figure 2.47: *Converter offset mean and standard deviation with internal chopper on, sweeping the chopper frequency, for two different OSR.*

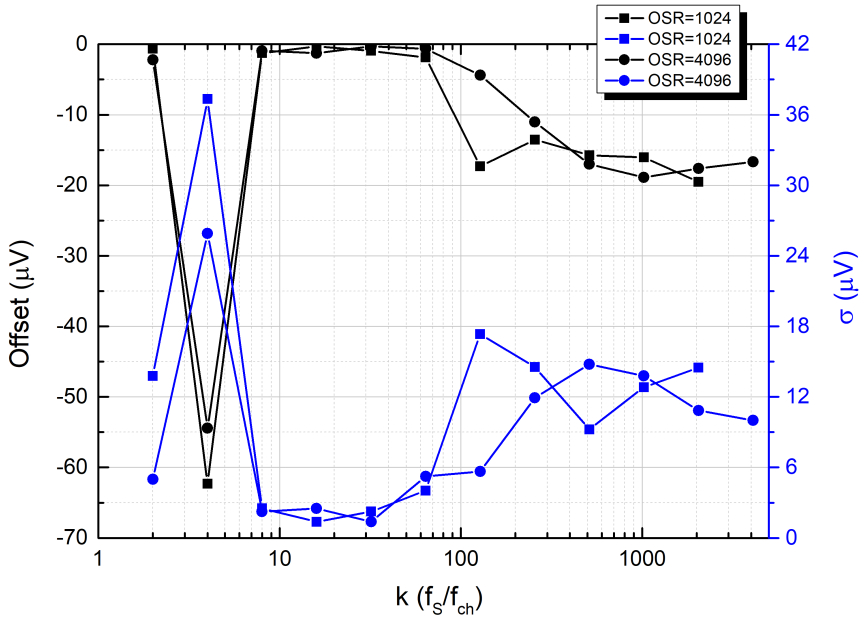


Figure 2.48: *Converter offset mean and standard deviation with system-level chopper on, sweeping the chopper frequency, for two different OSR.*

smaller dead-zone amplitude has been measured with the highest chopper frequency. The effect of dead-zones may also be recognized in Fig.2.48, where for values of k lower than 64, the converter offset and noise standard deviation appear artificially close to zero. Nevertheless, with system-level chopper frequencies lower than 60 kHz, no dead-zones have been observed. Further improvements will concern the mitigation of this phenomenon, even if the range of chopper frequencies which do not cause the arising of dead-zones is already fine for most of the targetted applications.

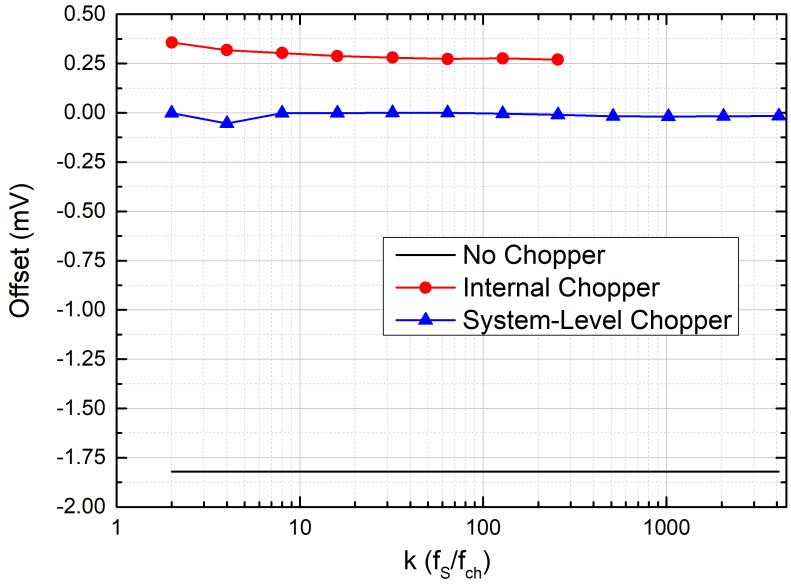
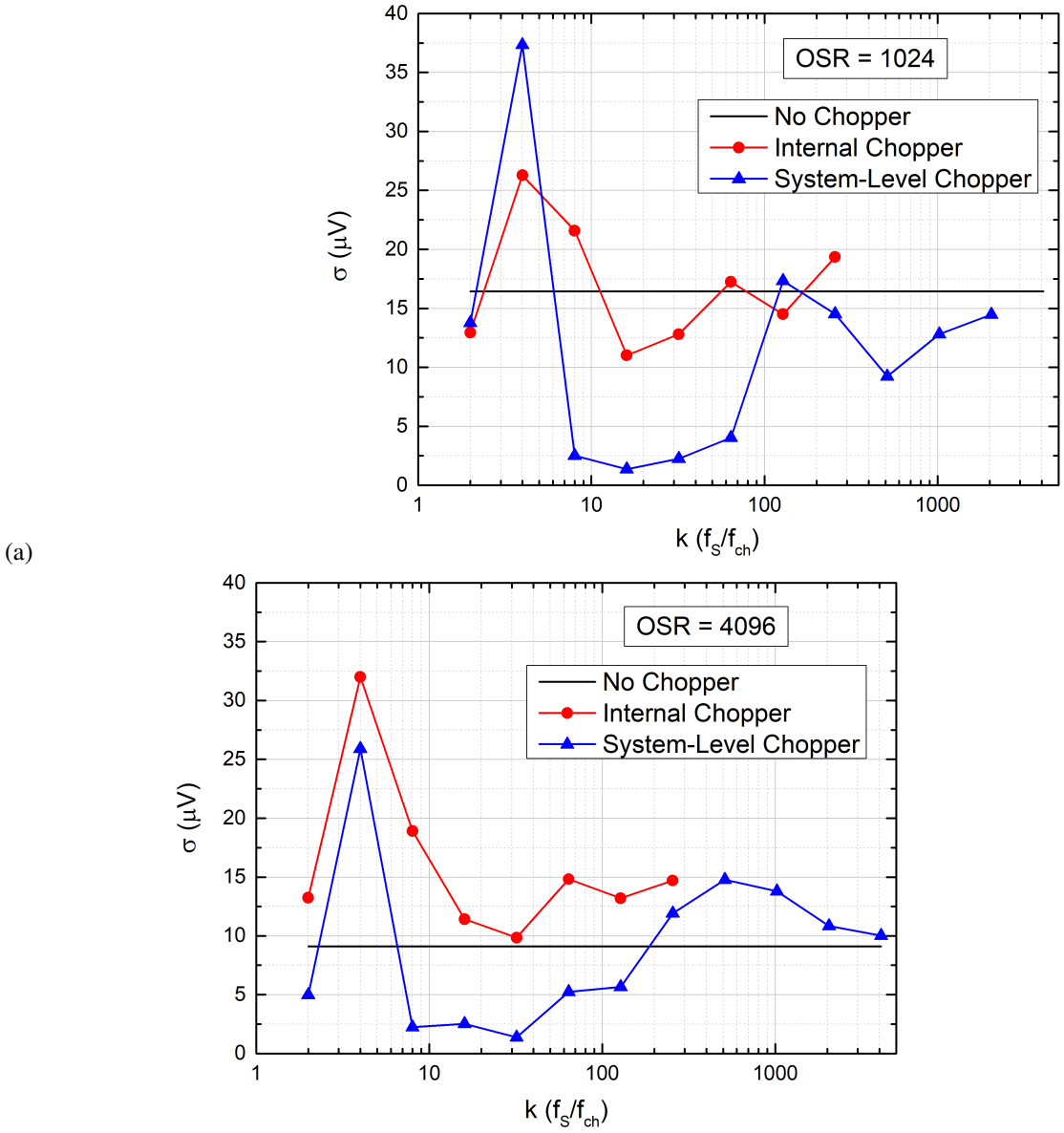


Figure 2.49: *Comparison of converter offset without chopper techniques, with internal chopper on and with system-level chopper on.*

Measurements have been replicated also with reference voltage equal to 1.2 V (provided by a bandgap voltage reference), and with the converter supplied at 1.8 V and 1.5 V, both with ratiometric and bandgap reference voltages. Measurement results confirm the functionality at lower supply voltages, especially concerning offset suppression and low noise.

Gain error and INL

From the dc characteristics previously shown, it is possible to extrapolate information on the gain error and the non-linearities of the converter in the different configurations. In the next graphs in figs. 2.52 to 2.54, the converter INL for the whole dc input range is shown. A maximum INL of around 250 µV in the three different configurations have been measured, a value higher than the one expected from simulations. Problems of non-linearities and harmonic distortions have been measured also in the spectrum analysis of the output bitstream (see next paragraph). Further investigations will try to better understand the cause of these distortions in order to improve the next version of the converter design. Table 2.4 recaps the performances in terms of offset, gain error and maximum INL for the converter without chopper techniques, with internal chopper on and with system-level chopper on, respectively. System-level CHS shows the best offset rejection, while it shows worse gain error, probably due to the amplifier dc gain reduction witnessed also by dead-zones arising.



(a)

(b)

Figure 2.50: *Comparison of converter noise standard deviation without chopper, with internal chopper and with system-level chopper, for a) OSR = 1024; b) OSR = 4096.*

2.4.2 Spectrum analysis

In this section, an analysis of the dynamic performances of the converter has been addressed. In Fig.2.55, a sinusoidal input of 3.3 V-pp with a frequency of 80 Hz has been fed into the converter, and the spectrum analysis of the output bitstream has been made through the Fast Fourier Transform (FFT) analysis of the output bitstream. $THD = -80.52dB$ limits the effective resolution of the converter, confirming the non-linearity problems already seen with the INL. Table 2.5 recaps the performances from the spectrum analysis, for different OSR. Considering the DR of the converter and the definition of noise-free resolution, we obtain a resolution of 15.38 bit and 16.56 bit for

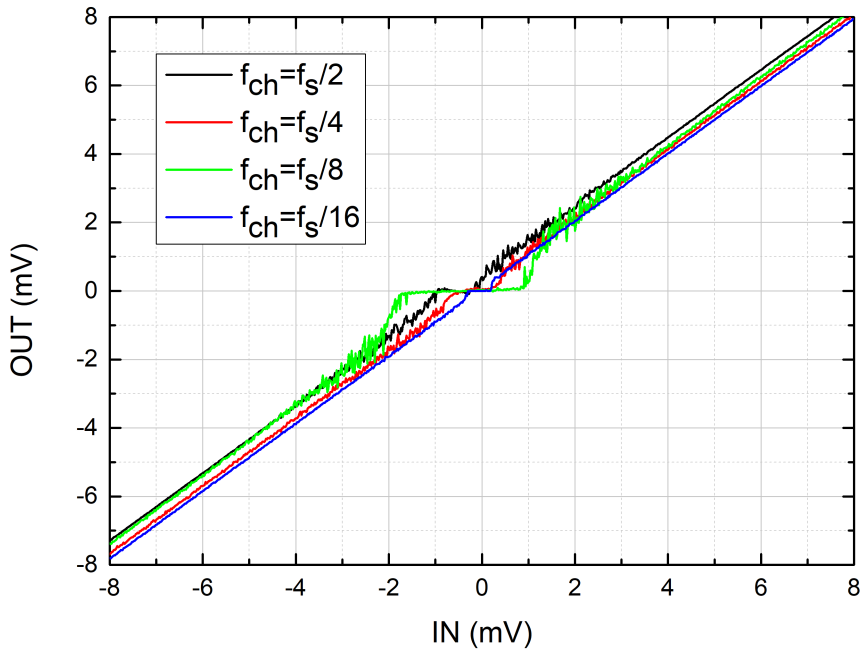


Figure 2.51: *Zoom of the dc characteristics around zero differential input, for different frequencies of system-level chopper.*

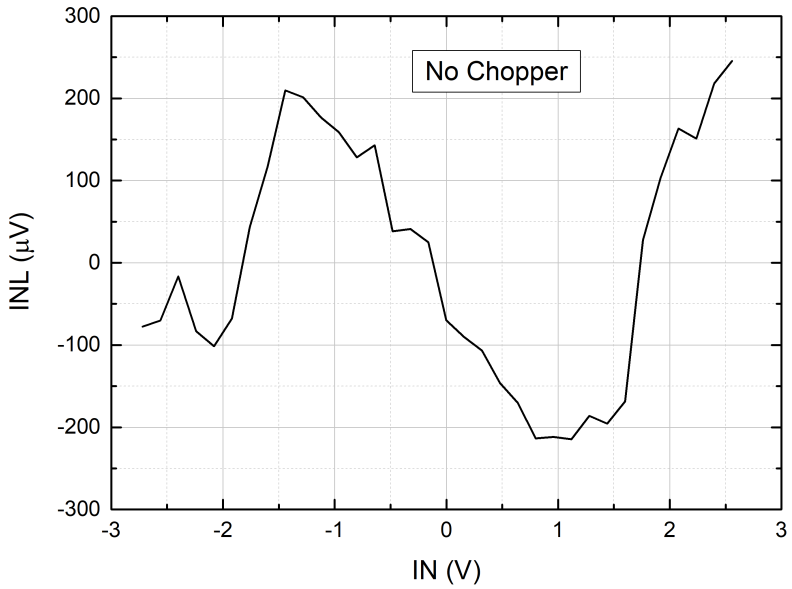


Figure 2.52: *Converter INL without chopper technique applied.*

OSR = 1024 and 4096, respectively with $FoM_S = 155.3dB$ and $FoM_S = 156.34dB$. Spectrum analysis have been repeated also with internal chopper enabled and system-level chopper enabled, observing analogous performances, except for a slight worsening of the THD in the case of system-level chopper technique ($THD = -79.22dB$). Considering the sampling frequency and the sizing of the amplifier, flicker noise does not appear to be dominant in the bandwidth considered in these spectrum analysis.

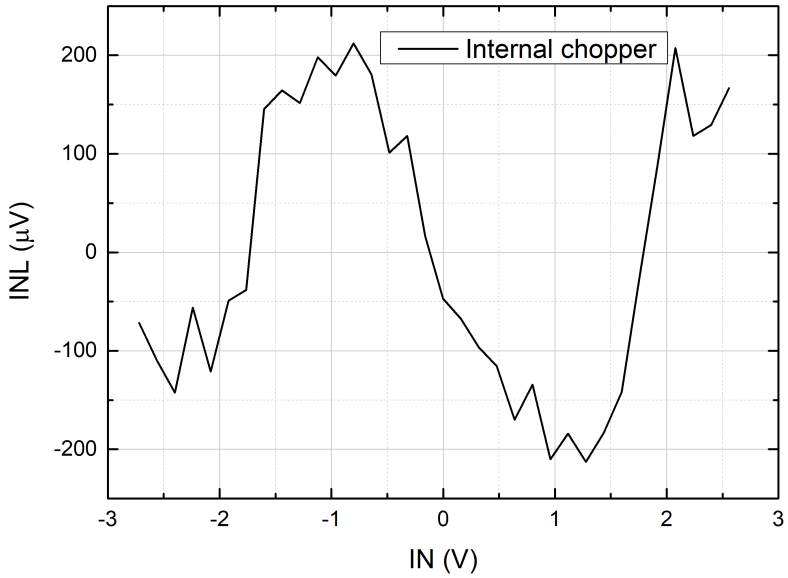


Figure 2.53: *Converter INL with internal chopper technique applied.*

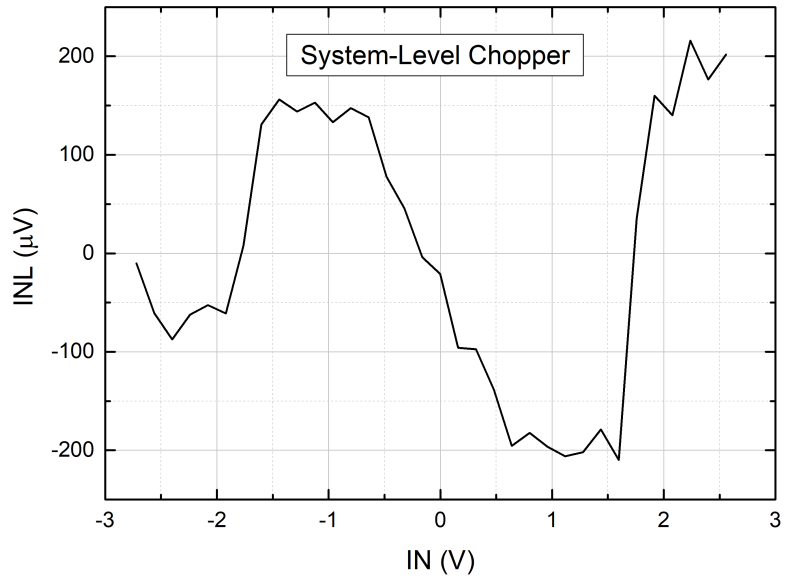


Figure 2.54: *Converter INL with system-level chopper technique applied.*

2.5 Discussion and conclusion

At the beginning of this chapter, a brief overview about the wide world of Delta-Sigma Analog-to-Digital Converters is provided, focusing on the implications of the transistor-level designs of each different topology. Targeting high-resolution and high-accuracy for digitizing low-frequency input signals, a 2^{nd} order discrete-time modulator has been choice. After the high-level and the transistor-level descriptions, especially concerning the first integrator, the description of two novel techniques has been developed. The system-level chopper technique is described, supported both by numerical simulations in Matlab environment and electrical simulations with Spectre. The described tech-

Table 2.4: *Summary of static performance of the 2nd order Δ-Σ, with the different chopper techniques implemented*

	Offset (mV)	Gain error (%)	Max INL (μ V)
No Chopper	-3.76	0.066	246
Internal Chopper	0.286	0.046	213
System-Level Chopper	0.005	0.568	216

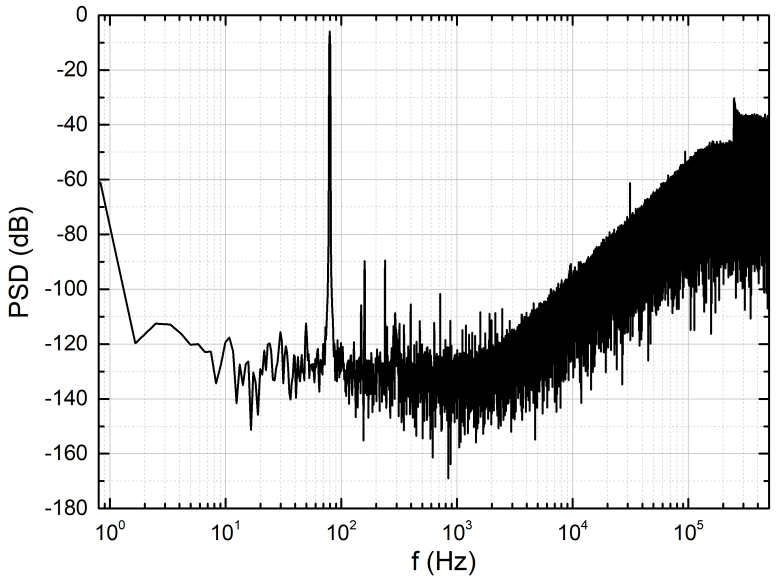


Figure 2.55: *Output bitstream spectrum, with a sinusoidal input at 80 Hz with 3.3Vpp.*

nique can also be exploited in impedance spectroscopy readout interfaces with several advantages compared to traditional systems. In order to face settling time errors in the discrete-time integrator, a power efficient slew-rate enhancement circuits has been proposed. Measurements effectuated on a silicon prototype in UMC 0.18 μm CMOS process, confirm the effectiveness of the proposed converter for high-resolution and high-accuracy sensor applications, even if the presence of harmonic distortions, not detected during the verification by means of electrical simulations, has been measured. Thanks to the proposed system-level chopper technique, offset is reduced to values lower than the LSB, two orders of magnitude lower than the residual offset after the standard CHS technique.

Table 2.5: *Summary of the dynamic performances of the 2nd order Δ-Σ.*

OSR	Nyquist Rate (Hz)	P_d (W)	SNR (@OSR=128) (dB)	SINAD (dB)	FoM_S (dB)
128	1M	396 µ	82.3	78.17	148.1
256	1M	396 µ	88.97	79.74	146.67
512	1M	396 µ	90.84	79.98	143.9
1024	1M	396 µ	91.77	80.2	141.1
2048	1M	396 µ	95.07	80.44	138.3

CHAPTER 3

Design of ultra-low voltage delta-sigma converter for energy harvesting applications

3.1 Introduction

As already described in paragraph 1.5, technology scaling has driven the analog/mixed design towards new horizons and new challenges. Together with newer technology nodes, reduction of the supply voltages have followed the shrinking of the channel lengths. While both the two phenomena have enhanced the performances of digital circuits in terms of speed and power consumption, analog designers have not obtained similar benefits. Technology nodes of the last two decades have been started showing non-ideal effects of MOSFET behaviour, such as short-channel effect, well proximity effect, gate leakage, etc., all detrimental for analog design. Basically, lower channel lengths mean lower MOSFET intrinsic gains, and smaller dimensions also imply higher device mismatches and process variations. Furthermore, the lower supply voltage has not been followed by a proportional scaling of the threshold voltages, reducing the available voltage headroom for each transistor.

For all these reasons, technology scaling is typically not worth for analog-centric ICs. However, in complex SoCs where the digital core typically occupies the dominant part of the silicon area and impacts the most the IC performances, it is unavoidable to scale also the analog blocks. As widely discussed in the first chapter, Analog-to-Digital Converter is one of the most crucial analog/mixed-signal block in several applications. Thus, the design of ADCs with modern CMOS processes and low supply voltages has become mandatory.

Apart from the technology scaling, other important factors moved the designers towards low-voltage and ultra-low voltage designs. While for the definition of low-power (LP) and ultra-low power (ULP) designs we can take [74] as a reference, for low-

voltage (LV) and ultra-low voltage (ULV) designs it is trickier to define a boundary between the two regimes. The continuous updates of the definitions due to technology scaling and the different declinations that we can find, depending on the particular application, can be often confusing. In this work we will consider as LV designs those suitable with supply voltages of digital cores of the modern CMOS processes (0.7 - 0.8 V). With ULV designs, instead, we will consider the ones capable of working with lower supply voltage, down to 100 mV.

In the last years, emerging technologies have start requiring electronic interfaces compatible with lower and lower supply voltages. Energy harvesting devices, for example, are able to derive energy from external sources to power wireless sensor nodes or wearable devices. Energy harvesters exploit many different physical principles, such as piezoelectric effect with MEMS resonators, Seebeck and Peltier effects for thermoelectrics, wireless energy from ubiquitous radio transmitters or deliberate RF energy sources (as in passive RFID), photovoltaic effect for solar energy harvesting, etc. The power available from these devices are typically reduced: from tens of mW from solar and kinetic harvesting, to fractions of mW from electromagnetic and thermoelectric harvesting. Also the supply voltages generated are reduced, typically on the order of few hundreds of millivolts [75].

Among energy-harvesting devices, biofuel cells deserve a special mention. They are devices able to convert chemical energy to electrical energy, exploiting redox reactions inside living organisms. There are two main categories of biofuel cell: (i) microbial fuel cells, which exploit bacteria or try to mimic bacterial interactions; (ii) enzymatic biofuel cells, which exploit enzymes as catalyst to oxidize its fuel. Typical examples of enzymatic biofuel cells use the reaction between glucose and oxygen [76–78]. [76], for example, generates a power density of 129 $\mu\mathrm{W cm}^{-2}$ at 0.38 V, exploiting glycaemia of human blood. These devices are extremely interesting in the optic of developing self-powered biosensors. The increasing improvements in this field has leaded to a great interest for wearable devices [24], which may have remarkable impacts on several aspects of everyday life, from healthcare to defence and security applications.

Once a certain supply voltage is generated by the energy harvester, several alternatives could be adopted to power the electronics. The simplest one consists in providing (more or less) directly the generated supply voltage to the electronics. This supply voltage, depending on the kind of harvesting source, is usually not high enough to power conventional monolithic ICs and the fabrication of a full-custom electronic interface capable of working with such supply is not straightforward to design. An alternative solution is to effectuate a step-up DC-DC conversion [79, 80], providing a supply voltage sufficiently high to power conventional electronics. The problem with the employment of a DC-DC converter is the lost of efficiency, considering the possible variations of the voltages generated by the harvesters. Another solution requires the presence of a device of energy storage: the energy derived by the harvester is accumulated until it is sufficient to power the electronics for a short period, called burst.

In the perspective of InternetOfThings, InternetOfEverything and InternefOfWearable [24], a huge amount of sensor nodes or biosensors will be spread in the environment, more or less easily accessible for the human operator. In this optic, energy harvesting could provide almost infinite power supply, taken it directly from the environment, guaranteeing longer life to the node sensors and reducing the dependency

from battery power. Furthermore, reduced installation and maintenance cost due to the absence of cables and batteries would also increase the cost effectiveness of these devices, as well as reducing the environmental impact. The presence of a low power electronic interface, in order to properly condition the signal before the conversion in the digital world, is essential. The digital data can be acquired periodically with a very low power transmission, also with a long interval, or when a certain threshold of the measured signal is reached.

In this chapter, the design of an ultra-low power and ultra-low voltage ADC optimized for sensor interfacing and supply voltages compatible with energy harvesting and bio-applications (as [81]), is described. The proposed converter takes advantage of an innovative switched-capacitor integrator suitable for inverter-like designs. Measurements on a prototype designed in the $0.18\ \mu\mathrm{m}$ CMOS process of UMC prove the effectiveness of the proposed ADC.

3.2 ULV CMOS design

Working with very low supply voltages, several issues come from the design of CMOS integrated circuits [82]. In the digital world, a reduction of the supply voltage means a reduction of the dynamic power consumption ($P_{dynamic} \alpha V_{dd}^2 f_{ck}$) and of the maximum speed. Technology scaling, on the other hand, moves towards the increase of the transition frequency and the decrease of the threshold voltage in order to allow faster switching frequencies. The limit on the threshold voltage scaling is dictated by the increase of the leakage gate current, that does not make worth the supply voltage scaling any further. As a result, low voltage headroom for the CMOS devices represents a critical issue, especially for analog/mixed designs. The low voltage headroom, in fact, penalises the implementation of several circuit topologies. The number of stacked transistors from the two rails ground and V_{dd} (in the case of single supply), is limited. Cascode structures, for example, are difficultly implementable with supply voltages lower than $V_{th} + 2(V_{GS} - V_{th})$; the output range of an amplifier with a cascode output stage, for example, is reduced of $4(V_{GS} - V_{th})$ respect to the maximum available range of V_{dd}.

The interest for low-power and low-voltage design is related not only to the advancing in modern CMOS processes. Also in older technology nodes, LV and ULV designs have become appealing for "more-than-Moore" applications. Wireless sensor networks for IoT or wearable devices demands more and more compact and low-power electronics for sensor interfacing. If powered by energy-harvesting devices as bio-fuel cells, ULV design techniques become mandatory to achieve the required performances. Just to contextualise the main issues of this kind of design, we can refer to typical switched-capacitor circuits. As already mentioned, several blocks of data acquisition systems are implemented with SC circuits, from the analog front-end to the ADC. They require switches with small on-resistances and operational amplifier with sufficiently high dc gain and input impedance. Both these circuits suffer from the reduced supply voltage, and more in general all the analog/mixed signal blocks require additional cares.

Working with ultra-low supply voltages implies the biasing of MOSFETs with gate-source voltages close to their threshold voltage. MOSFETs biased in subthreshold region ($V_{GS} < V_T$) or weak inversion ($V_{GS} - V_{th} \ll 4V_T$) has an exponential dependence

of their drain current to the gate-source voltage, as expressed in [83, 84]:

$$I_D = I_{SM} e^{\frac{V_{GS}-V_{th}}{nV_T}} \left[1 - e^{-\frac{V_{DS}}{V_T}}\right] \tag{3.1}$$

$$I_{SM} = 2n\mu_n C'_{ox} \frac{W}{L} V_T^2 \tag{3.2}$$

where n is the slope factor (typical value are around 1.5-2), C'_{ox} is the gate oxide capacitance per unit area, μ_n is the electron mobility in the channel (for the NMOS devices) and V_T is the thermodynamic voltage, defined as KT/q (where K is the Boltzmann constant, T the absolute temperature and q the charge of the electron). For $V_{DS} > 4V_T$, the dependency on the drain-source voltage is typically negligible. The exponential dependency of the drain current with the gate-source voltage recalls the expression of the collector current of a bipolar and its exponential dependency with the base-emitter voltage. No coincidence, in fact, that MOSFETs in weak-inversion are recently used to realize bandgap voltage references, replacing bipolar transistors and realizing all-MOSFETs, sub-1V voltage reference [85, 86]. Working with MOSFET devices in weak inversion is advantageous in terms of transconductance, compared to strong inversion region. The expression of the transconductance in saturation and weak-inversion region is:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nV_T} \tag{3.3}$$

It is possible to compare weak inversion and strong inversion regions in terms of effective thermal voltage (the inverse of the ratio g_m/I_D):

$$V_{TE} = \frac{I_D}{g_m} = \begin{cases} \frac{V_{GS}-V_{th}}{2} & \text{strong inversion} \\ nV_T & \text{weak inversion} \end{cases} \tag{3.4}$$

Working with MOSFETs biased in weak inversion or in subthreshold region is more efficient in terms of trade-off between current consumption and speed/noise. Also the design with regular supply voltages often exploits MOSFETs biased in weak inversion, e.g. the devices of input differential pairs, to reduce their noise contributions in differential amplifiers, keeping the bias current unchanged.

Even the implementation of MOSFET switches can be critical: if the threshold voltage is on the same order of supply voltage, NMOS devices are in subthreshold region for whatever input signal, even with an high level gate signal (analogous behaviour also for the PMOS switches). Unless of sizing the devices with very large W/L, the on-resistance of subthreshold MOSFETs may be very high and not feasible for practical SC circuits. Even implementing pass-gates do not mitigates this effect. Bootstrapping [87] or clock boosting [88] techniques become mandatory in order to reach lower on-resistances without large areas. A part from the area consumption, reducing dimensions of the switches also lowers the parasitic capacitances related to them, which may be detrimental in terms of non-linearities, charge injections and equivalent resistive load in SC circuits.

Also the design of amplifiers become particularly challenging, mainly due to low voltage headroom for each transistor. Several amplifier topologies have been specifically proposed for low-voltage supplies [89, 90]. Another critical problem is related to

the low intrinsic gain of MOSFET devices. Increasing the number of amplifier stages increases also the power consumption and compensation complexity, while stacking too many devices is not compatible with the supply rails. Longer channel length devices are preferred to increase the voltage gain; however, high W/L are required to reach sufficiently high bandwidths. Combined with long L, large device areas, with consequent larger parasitic capacitances, have detrimental effects on the frequency response. Alternative techniques as bulk-driven topologies ([91, 92]), DTMOS devices [93–95] or dynamic biasing [96, 97], allow the fulfilment of amplifier requirements for ULV design. However, as far as supply voltages lower than 0.5 V are approached (as 0.3 V of supply voltage provided by biofuel cell [81]) and not all the above mentioned techniques are straightforwardly implementable, inverter-like amplifiers [98, 99] become unavoidable. Also the cascade of more inverter-like stages is not an easy way to go: two inverter stages realizes a positive voltage gain, that is not suitable for traditional feedback amplifier configurations; three inverter stages, instead, realizes the well known ring oscillator, that is not employable as an amplifier without proper modifications as in ring amplifiers [100]. Fully-differential inverter-like amplifiers require additional circuitry for the common mode control, not always easily implementable at very low supply voltages. Of course, the several benefits of FD systems in terms of common-mode disturb rejection and enhanced linearity can represent a worth incentive to explore that kind of circuits. In this chapter, only single-ended implementations will be described.

Two main topologies of single stage amplifiers can be distinguished: class-A inverter (common-source stage) and class-AB inverter (standard CMOS inverter) [101], depicted in Fig.3.1. Both the amplifiers have a single inverting input and they cannot replace one to one an operational amplifier. However, in SC circuits, the non-inverting terminal is typically connected to a reference voltage (half of the supply rail in single-ended circuits) and it is not effectively connected to any input or any passive device. In such cases, inverters may replace traditional operational amplifiers. Fig.3.2-a shows the equivalence between a traditional inverter CMOS and a differential voltage amplifier. The output voltage of the amplifier is referred to V_{inv}, the inversion voltage, that is defined as the voltage that, put as an input of the inverter, gives the same voltage at the output. In CMOS NOT gate for logic circuits, it is called switching threshold voltage, here it will be called inversion voltage to not be confused with the MOSFET threshold voltage.

Around that value, the inverter shows the higher value of the voltage gain (also identifiable from the slope of the input-output characteristic shown in Fig.3.2-b). The inverter, then, is perfectly schematized by the differential voltage amplifier, with the non-inverting input terminal of the op-amp connected to V_{inv} and the output voltage referred to V_{inv}, as in Fig.3.2. Thus, the inversion voltage could be considered as a virtual ground of the circuit, without any loss of generality. With the typical sizing of a CMOS inverter (i.e. with the aspect ratio of the PMOS sized to compensate the different mobility compared to the NMOS), the inversion voltage is around the middle-rail, that is a good value to maximize the linearity region of the amplifier. The just mentioned considerations for the class-AB inverter are perfectly generalizable also for the class-A inverter.

Table 3.1 recaps the main difference between the class-A and the class-AB inverter

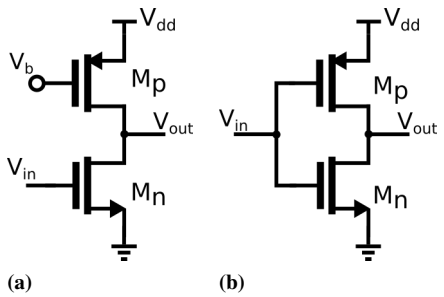


Figure 3.1: *a) Schematic view of the class-A inverter. b) Schematic view of the class-AB inverter.*

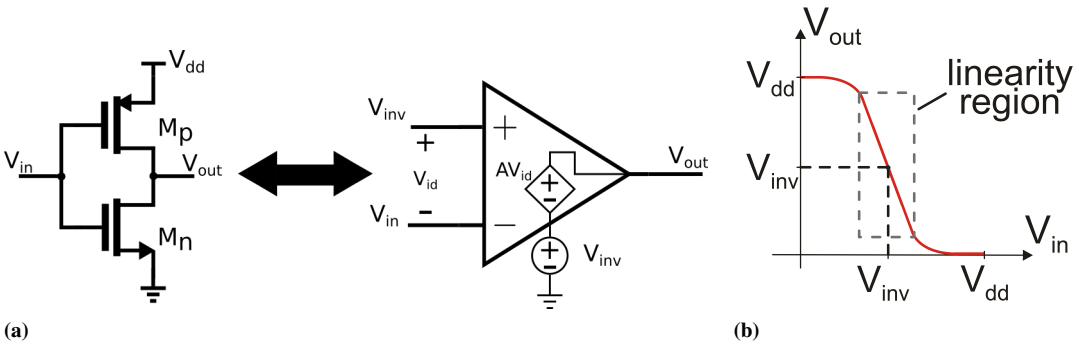


Figure 3.2: *a) Equivalence between an inverter and an amplifier. b) Dc characteristic of an inverter.*

shown in Fig.3.1, designed in UMC 0.18 µm process, sized to have the same nominal bias currents, with a supply voltage of 0.3 V. The main parameters taken into account are:

- the dc gain A_0;
- the gain bandwidth product GBW (with a load capacitance of 100 fF);
- the square root of the broadband power spectral density $S^{1/2}_{BB-RTI}$;
- the flicker noise corner frequency f_k;
- the ratio between the maximum output current that the amplifier is able to sink and source $I_{o-sink}/I_{o-source}$;
- the PSRR;
- the standard deviation of the inversion voltage σ_{os} with respect to process variations and device mismatches;
- the quiescent currents in the case of corner SS and FF $I_{SS} - I_{FF}$;
- the quiescent currents in the case of -55 °C and 80 °C $I_{-55°C} - I_{80°C}$.

Class-A inverter takes the advantage of a fixed bias current. Variations of its bias current with respect of PVT variations are reduced. However, less current efficiency with respect of gain, bandwidth, offset and noise is present. In class-A inverters, in

Table 3.1: *Comparison between the performances of class-A and class-AB inverters, simulated in UMC 0.18* µm *CMOS process with* $V_{dd} = 0.3V$.

	A_0 (dB)	GBW (Hz)	$S^{1/2}_{BB-RTI}$ $(nVHz^{-1})$	f_k (Hz)	$I_{o-sink}/I_{o-source}$ (A)
Class-A Inverter	21.8	51.4 k	243	1.87 k	2.4 n / -220.5 n
Class-AB Inverter	27	93.83 k	136	1.89 k	101.9 n / -222.8 n

	PSRR (dB)	σ_{os} (mV)	$I_{SS} \div I_{FF}$ (A)	$I_{-55°C} \div I_{80°C}$ (A)
Class-A Inverter	30.5	16.2	[2.25 n ÷ 2.7 n]	[1.47 n ÷ 3.2 n]
Class-AB Inverter	6	8.2	[593 p ÷ 9 n]	[8.5 p ÷ 3.2 n]

fact, only Mn amplify the input signal. For this reason, only its transconductance contributes for the dc gain and the gain-bandwidth product. Both the devices, instead, contribute to the output resistance, that is the parallel of their differential output resistance. Moreover, both devices generate noise and contribute to the variation of the inversion voltage with respect to process mismatches. Concerning RTI noise and offset, both contributions will result in higher errors than in a class-AB inverter. Eventually, only sinking (with NMOS active device, as in the case-study here analysed) or sourcing (with PMOS active device) capability of the output current is present.

Class-AB inverter, without a fixed bias current, shows larger fluctuations due to PVT variations. In the process corner SS and/or at very low temperatures, the bias current is very low and the inverter cannot work properly. More attention has to be spent on the class-AB inverter sizing, in order to guarantee the minimum allowed performances in all the possible corners. On the other hand, in the corner FF and with high temperatures, the amplifier dissipates more static current but it will also show better speed performances. Despite the low robustness of the circuit, it is often preferred to class-A stages for its better efficiency. A_0 and GBW are almost double compared to the class-A stage, because of both Mn and Mp are active devices, acting in the signal amplification. For this reason, RTI offset, thermal noise and flicker are lower (the corner frequency is actually the same, but showing lower broadband noise, it will also show lower flicker noise). Furthermore, because of its class AB operations, it is able to sink and source almost the same amount of output current, much higher than its quiescent current.

In the following sections, we will consider inverter-based circuits exploiting only class-AB inverter stages, due to their better efficiency. Fig.3.3 shows some interesting behaviours of the inverter bode diagram, biased with V_{in} around V_{inv} to use it as a voltage amplifier. Fig.3.3-a,b show respectively the variations of the transfer functions with respect of the channel length and the aspect ratio. Longer channel lengths impact mainly only on the voltage gains, while higher aspect ratios allow the achievement of higher gain-bandwidth products, at the cost of higher bias currents. Finally, Fig.3.3-c shows the variation with respect of the supply voltage. It is worth noting how the dc gain, excluding the case with V_{dd} = 0.2 V, does not vary consistently with the supply voltage, while the GBW varies of several orders of magnitude due to the exponential behaviour of the drain current. For V_{dd} above 1 V, the GBW variations are limited due to the passage from weak inversion to strong inversion (i.e. from an exponential

dependency of the bias current with the supply voltage, to a quadratic dependency).

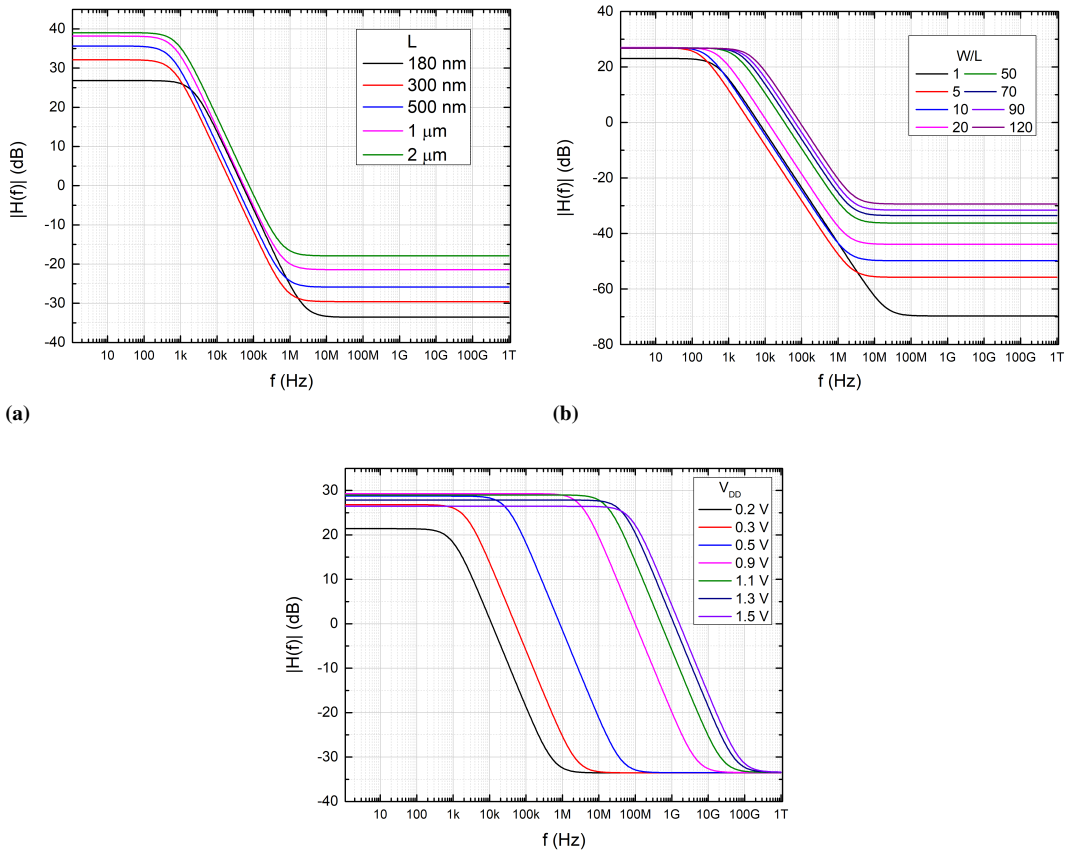


Figure 3.3: *a) Inverter amplitude bode diagram sweeping the channel length of both devices, with W/L=70, C_L=100 fF and $V_{dd} = 0.3V$. b) Inverter amplitude bode diagram sweeping the aspect ratio W/L of both devices, with L=180 nm, C_L=100 fF and $V_{dd} = 0.3V$. c) Inverter amplitude bode diagram sweeping the supply voltage, with L=180 nm, W/L=70 and $C_L = 100fF$.*

3.3 Proposed building block for ULV applications

After the brief introduction about the ULV CMOS design, a novel inverter-like switched-capacitor integrator will be described, by referring to [102]. Thanks to the novel two-stage topology, the integrator shows a finite dc gain proportional to the cube of the gain of a single amplifier, employing only two amplifiers. For this reason, this architecture is suitable for low-voltage and ultra-low voltage designs, using inverter-like amplifiers. In fact, even if the inverter gain is on the order of few tens at very low supply voltages and minimum channel lengths, the overall dc gain can easily reach several thousands. Furthermore, it implements a novel CDS technique that rejects offset and flicker noise components of the amplifiers. Both features encourage the employment of minimum channel length devices for the inverter like amplifiers. Despite of the CDS technique, the output voltage is always valid, in a sort of time-continuous fashion. After a brief description of the discrete-time behaviour of the proposed circuit (more details will be

provided in Appendix A), a description of the possible employment in continuous-time application is given. Obviously, the validity of the employment of a discrete-time circuit for continuous-time applications requires the fulfilment of the Nyquist-Shannon condition, and more often that the input signal bandwidth should be much lower than the sampling frequency.

3.3.1 Circuit topology and operating principle

The proposed discrete-time integrator (DTI) is shown in Fig.3.4. Differently from previous solutions, the circuit uses two amplifiers, indicated with A_1 and A_2. This is not a significant complexity increase in the case that A_1 and A_2 are simple CMOS inverters. The integrator output is V_{o2}, while V_1 and V_2 are its inverting and non-inverting inputs. Labels "1" and "2" in Fig.3.4 indicate the switch state in the two corresponding operating phases. In single supply implementations, the reference node (indicated with a small downward triangle) is generally a floating rail distinct from either V_{dd} or the power supply ground (gnd). The circuit consists of two stages, indicated in Fig.3.4. In phase 1, the first stage stores a charge proportional to $V_2 - V_1$ into C_T. In phase 2, this charge is transferred to the second stage (i.e. into capacitor C_F) producing a proportional increment of the output voltage V_{o2}. The first stage uses the topology of [103] to perform the mentioned voltage-to-charge conversion with reduced sensitivity to A_1 gain and offset voltage.

The overall dc gain of the integrator is proportional to the product of the dc gain A_1 squared and the dc gain A_2. The first contribution is due to the topology of the first stage, similar to [103]. Also [104, 105] exploit the holding capacitor to close the negative feedback of the amplifier during the phase that is not the integration phase, obtaining a sensitivity to the square of the finite gain of the op-amp. The adding of the second stage in Fig.3.4 boosts additionally the finite dc gain of the integrator of a factor equal to the dc gain of A_2. This increments is very important when working with inverter-like amplifiers for ULV design, when the voltage gain of the single inverter may be as low as few tens. Furthermore, the addition of the second stage makes the output voltage always valid in both phases, differently from other topologies [105], increasing the flexibility of this architecture.

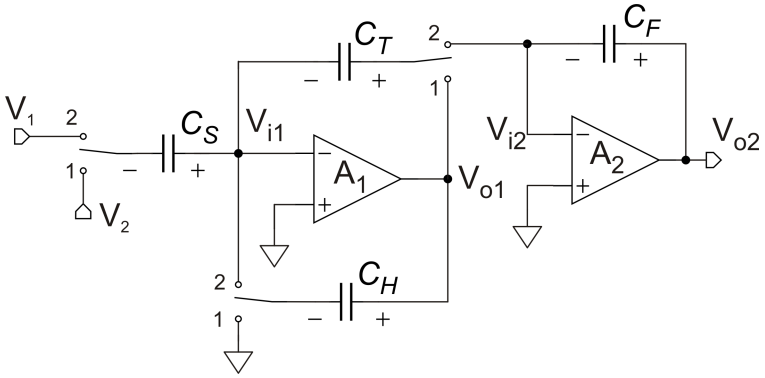


Figure 3.4: *Schematic view of the proposed integrator. V_{o2} is the integrator output. Other relevant voltages are indicated.*

3.3.2 Detailed circuit analysis

The analysis described in this section does not take into account the effects of parasitic input capacitances, amplifier non-linearity, finite bandwidth and switch non-idealities. Finite gain effects and input offset voltages are intrinsically included by the presence of non-zero amplifier input voltages, V_{i1}, V_{i2} (imperfect virtual ground). Fig.3.5 shows the convention used in the following part of this document to indicate the clock phases. All phases have a duration of T/2, where T is the clock period ($f_{ck} = 1/T$ is the clock frequency). Voltage polarities are specified in Fig.3.5 by +,- symbols. With $V_x^{(i)}$ we indicate generic voltage V_x at the end of phase "i".

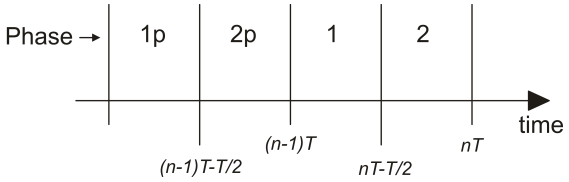


Figure 3.5: *Conventions used to indicate the phase sequence across two clock periods.*

Let us start by considering the transition from phase 2p to phase 1. By standard analysis based on charge conservation, voltage V_{o1} can be expressed by:

$$V_{o1}^{(1)} = V_{i1}^{(1)} + V_{i2}^{(2p)} - V_{i1}^{(2p)} + \frac{C_S}{C_T}(V_1^{(2p)} - V_2^{(1)}) + \frac{C_S}{C_T}(V_{i1}^{(1)} - V_{i1}^{(2p)}) \tag{3.5}$$

In the following $1 \rightarrow 2$ transition, voltage V_{02} becomes:

$$V_{o2}^{(2)} = V_{i2}^{(2)} + V_{C_F}^{(1)} + \frac{C_T}{C_F}(V_{C_T}^{(2)} - V_{C_T}^{(1)}) \tag{3.6}$$

where V_{C_F} and V_{C_T} are voltages across capacitors C_F and C_T, respectively. Considering that no charge flows across C_F in the $2p \rightarrow 1$ transition, then it can be simply found that:

$$V_{o2}^{(2)} = V_{i2}^{(2)} + V_{o2}^{(2p)} - V_{i2}^{(2p)} + \frac{C_T}{C_F}\left[\left(V_{i2}^{(2)} - V_{i1}^{(2)}\right) - \left(V_{o1}^{(2)} - V_{o1}^{(1)}\right)\right] \tag{3.7}$$

Using 3.5, the following expression for the integrator output in phase 2 can be finally found:

$$\begin{aligned} V_{o2}^{(2)} = V_{o2}^{(2p)} + \frac{C_S}{C_F}(V_2^{(1)} - V_1^{(2p)}) + (1 + \frac{C_T}{C_F})(V_{i2}^{(2)} - V_{i2}^{(2p)}) - \frac{C_T}{C_F}(V_{i1}^{(2)} \\ - V_{i1}^{(2p)}) - \frac{C_S}{C_F}(V_{i2}^{(1)} - V_{i1}^{(2p)}) \end{aligned} \tag{3.8}$$

Notice that V_{i1} and V_{i2} are present only as difference of samples taken at different instances. As a result, flicker noise and offset contributions that contaminate V_{i1} and V_{i2} are reduced by a CDS mechanism. Further considerations about thermal noise analysis in this architecture are described in appendix A. Voltage V_{o2} is maintained across the following phase 1. Voltage V_{o1} in phase 2 can also be easily found:

$$V_{o1}^{(2)} = V_{i1}^{(2)} + V_{o1}^{(1)} + \frac{C_S}{C_H}(V_{i1}^{(2)} - V_{i1}^{(1)}) + \frac{C_S}{C_H}(V_2^{(1)} - V_1^{(2)}) + \frac{C_T}{C_H}(V_{i1}^{(2)} - V_{i1}^{(1)}) + \frac{C_T}{C_H}(V_{o1}^{(1)} - V_{i2}^{(2)}) \tag{3.9}$$

3.3.3 Ideal behaviour

In the ideal case, the amplifiers have (i) infinite gain, (ii) zero offset voltage and (iii) zero input noise voltage. In these conditions, V_{i1} and V_{i2} are zero in all phases and 3.8 becomes:

$$V_{o2}(nT) = V_{o2}(nT - T) + \frac{C_S}{C_F}\left[V_2\left(nT - \frac{T}{2}\right) - V_1(nT - T)\right] \tag{3.10}$$

where we have considered that the output voltage is sampled at the end of phase 2. In the z-domain, 3.10 becomes:

$$V_{o2}(z) = H_i(z)[V_2(z)z^{+1/2} - V_1(z)] \tag{3.11}$$

where

$$H_I(z) = \frac{C_S}{C_F}\frac{z^{-1}}{1 - z^{-1}} \tag{3.12}$$

is the ideal integrator function. Differently from the circuits in [104, 105], the transfer function referred to the inverting input includes a one-cycle delay. This means that the proposed circuit performs forward Euler integration instead of backward one. Conversely, a half-cycle delay is present in the non-inverting transfer function, in conformity with traditional DTIs [104, 105].

3.3.4 Finite dc gain and offset voltage

Exact calculation of the transfer function taking into account the finite gain of the amplifiers is very complicated, and is beyond the scope of this work. We will limit our analysis to the case where V_1 and V_2 are dc voltages and the output voltage V_{o2} has reached the final asymptotic value. In these conditions, voltages do not vary from a clock cycle to the next one. As a result, 3.8 becomes:

$$V_{i1}^{(1)} - V_{i1}^{(2)} = V_2 - V_1 \tag{3.13}$$

Indicating the input offset voltages of A_1 and A_2, with V_{io1} and V_{io2}, respectively, the following expressions follow:

$$V_{o1} = -A_1(V_{i1} + V_{o1});\ V_{o2} = -A_2(V_{i2} + V_{io2}) \tag{3.14}$$

By means of elementary but tedious calculations it is possible to solve the equation set formed by eqs. (3.5), (3.9), (3.13) and (3.14), finding the dc output voltage:

$$V_{o2}^{(2)} = A_2(A_1^2 + A_1 + 1)(V_2 - V_1) + V_{io1}A_1A_2 - V_{io2}A_2 \tag{3.15}$$

Equation 3.15 proves that the dc gain exceeds $(A_1)^2 A_2$. For $A_1 = A_2 = A_0$, we get a dc gain of the order of $(A_0)^3$. The effective input referred offset voltage of the integrator (V_{io-rti}) can be easily derived from 3.15:

$$V_{io-rti} = -\frac{V_{io1}A_1 - V_{io2}}{A_1^2 + A_1 + 1} \cong -\frac{V_{io1}}{A_1} + \frac{V_{io2}}{A_1^2} \tag{3.16}$$

Therefore, the integrator input offset is dominated by the input offset of the first amplifier, attenuated by A_1 gain.

3.3.5 Discrete-Time simulations

Equations (3.5), (3.8) and (3.9) have been used to setup an ad hoc iterative discrete-time simulator, written using the Scipy scientific modules of the Python language. The simulator has been used to calculate the impulse response, from which the discrete-time frequency response of the integrator has been estimated by means of the Fast Fourier Transform (FFT). The only non-ideality taken into account is the finite gain of the amplifiers, set to 28 (29 dB) for both A_1 and A_2, in conformity with the actual gain of the amplifiers used in the prototype described in next section. Other simulator parameters are C_S/C_F, C_T/C_S and C_H/C_S ratios. The first ratio (C_S/C_F) acts as a multiplier factor in the ideal integrator response given by 3.12, hence the ideal unity gain frequency f_0 is:

$$f_0 = \frac{1}{\pi T} arcsin\left(\frac{C_S}{2C_F}\right) \cong \frac{1}{2\pi T}\frac{C_S}{C_F} \tag{3.17}$$

The other two-capacitance ratios affect the transfer function only in the case of finite gain. Fig.3.6 shows the simulated magnitude and phase response of the integrator for different C_S/C_F ratios. In order to achieve a sufficient frequency resolution the impulse response was simulated over an interval of 4×106 cycles. Notice that the dc gain practically coincides with the ideal value (87.14 dB), given by 3.15. The phase response is close to 90° over two or three decades, depending on the C_S/C_F ratio. The phase decrease at high frequencies is due to the delay term (z^{-1}) which is present in the ideal response 3.12, whereas the phase increase at low frequencies is the effect of finite gain. Magnitude and phase errors with respect to 3.12 are highlighted in Fig.3.7. The magnitude error exhibited at high frequencies is mainly due to the finite gain of A_2, which prevents the charge in C_T from being completely transferred to C_F in the $1 \rightarrow 2$ phase transition. Due to this error, the unity gain frequencies of the DTI are slightly smaller than predicted by 3.17, as shown in Table 3.2, where the phase error at f0, calculated with respect to 3.12 is also reported. The effect of the C_T/C_S ratio is shown in Fig.3.8 where the phase and magnitude error at f_0 are shown for the case $C_S/C_F = 1/4$. Notice that increasing the C_T/C_S ratios reduces the phase error. Finally, simulations performed by varying the C_H/C_S ratio showed that C_H has negligible effects for $f \leq f_0$.

3.3.6 Simulation of an inverter-like prototype

The inverter-like prototype is shown in Fig.3.9. INV-1,2,3 are identical CMOS inverters. All the switches are implemented with complementary p-n transmission gates

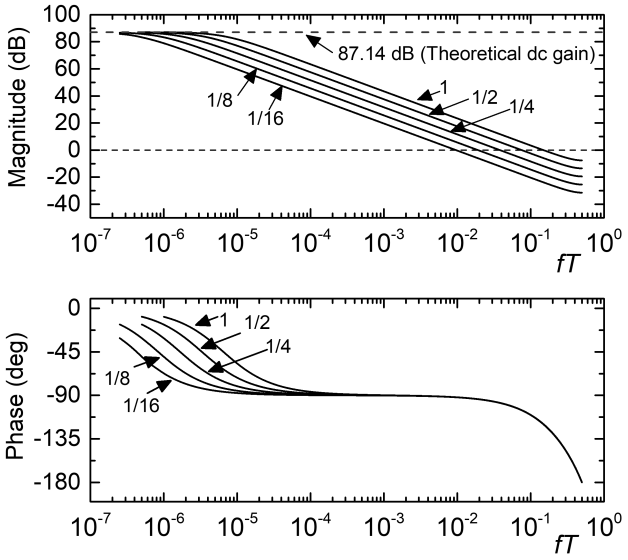


Figure 3.6: *Discrete-time simulation of the magnitude (top) and phase (bottom) response of the proposed DTI for different C_S/C_F ratios, indicated in the figure. Other settings are: $A_1 = A_2 = 28$, $C_T/C_S = C_H/C_S = 1$.*

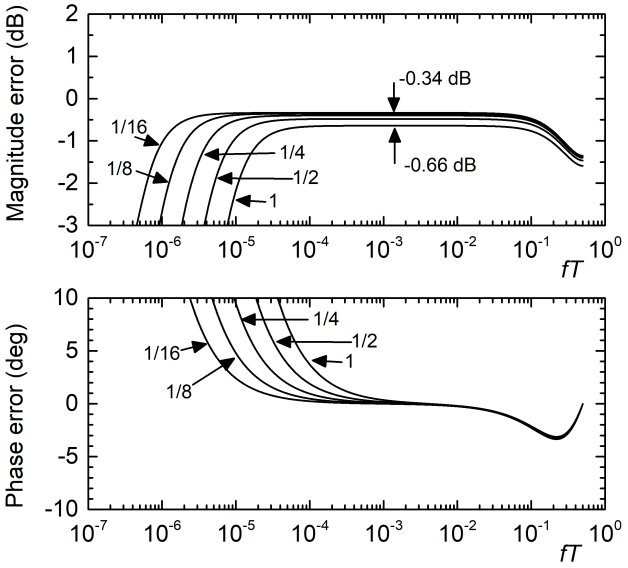


Figure 3.7: *Magnitude and phase error with respect of the ideal forward Euler discrete-time integrator described by equation 3.12 for the same parameters of Fig.3.6. Labels indicate different C_S/C_F ratios.*

(TG1-6). Device aspect ratios are reported in Fig.3.9 caption. Dummy switches are placed on critical nodes to compensate for charge injection. INV-1,2 play the role of A_1 and A_2, while INV-3 is used to create a floating rail at potential V_{ref}, which coincides with the inverter inversion voltage (V_{inv}). The analysis of previous sections is applicable to the circuit in Fig.3.9 if all voltages are referred to V_{ref} and V_{o1}, V_{o2} remain within the linearity range of the inverter output characteristic.

Table 3.2: *Unity gain and phase errors for different C_S/C_F ratios*

C_S/C_F	1/16	1/8	1/4	1/2	1
f_0 error (%)	-3.8	-4.1	-4.6	-6.4	-11
Phase error at f_0	-0.24°	-0.48°	-0.94°	-1.74°	-2.78°

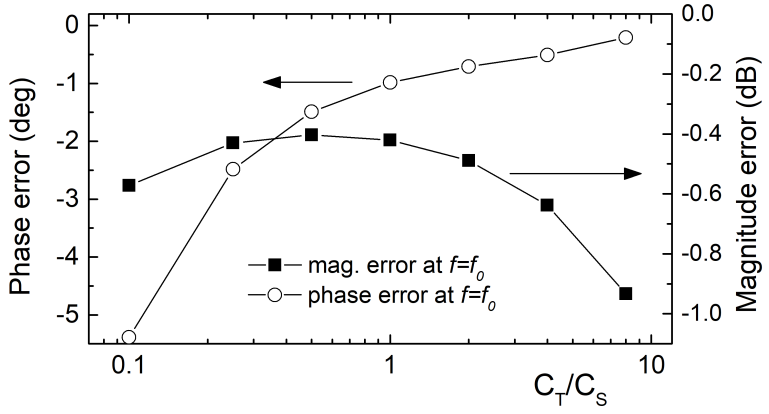


Figure 3.8: *Magnitude and gain errors with respect to the C_T/C_S ratio for $C_S/C_F = 1/4$ and $C_H/C_S = 1$.*

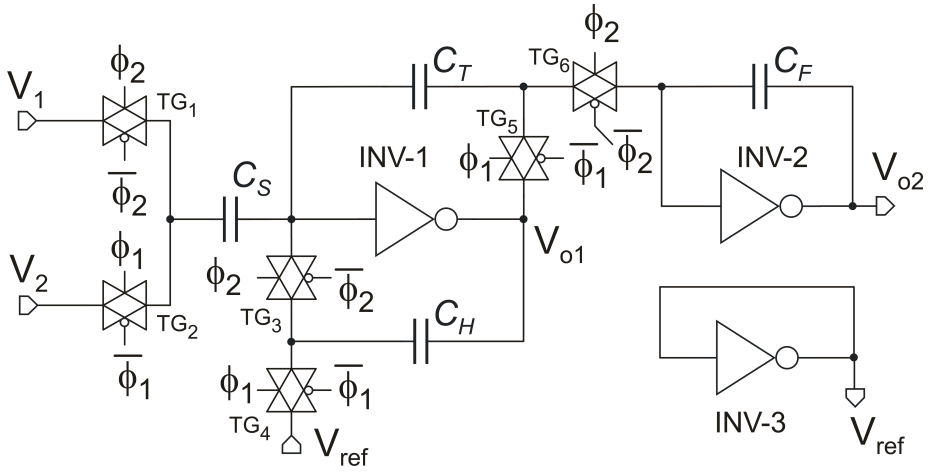


Figure 3.9: *Schematic view of the proposed integrator, implemented with inverter-like amplifiers. MOSFET aspect ratios (width/length, in microns) are as follows: 1.8/0.18 (nmos), 7.2/0.18 (pmos) for the inverter and 0.72/0.18 (nmos) and 2.88/0.18 (pmos) for the transmission gate.*

The circuit has been designed with the 0.18 µm CMOS process of UMC. Capacitors C_S, C_T and C_H have been set to 1 pF whereas C_F is varied from 1 pF to 16 pF to produce the same C_S/C_F ratios as in previous section. The inverter has been designed to allow operation up to clock frequencies of 1 MHz with the mentioned capacitance values and a supply voltage of 0.9 V. Aspect ratios are tuned to obtain $V_{ref} \approx V_{dd}/2$. The dc gain of the inverters, estimated for $V_{in} = V_{ref} = V_{inv}$, is 28 (~29 dB). The circuit in Fig. 3.9 has been simulated using the Spectre™ (Cadence) electrical simulator. Periodic state AC simulations (PAC) have been performed since it is not feasible to simulate the impulse response over a time interval long enough to collect the same

number of samples as in the discrete-time simulations of previous section. Notice that the high dc gain of the DTI, combined with residual charge injection contribution, hinders the achievement of a periodical stationary state. To overcome this difficulty, the closed loop test-bench of Fig.3.10 has been used. An ideal feedback network with gain β is implemented with the voltage-controlled voltage source E_1. The output voltage is sampled at the end of phase 2 and held by the ideal switch SH and capacitor C_M. E_2 prevents C_M from loading the integrator. The relevant waveforms are represented in the bottom right corner of Fig.3.10. Neglecting the duration of phase 3 pulses (=0.01 T), the time-continuous frequency response $H_{CL}(\omega) = V_{out}/V_{in}$ of the test-bench is tied to the discrete-time frequency response of the DTI, $H_I(e^{j\omega T})$, by:

$$H_{CL}(\omega) = \frac{e^{j\frac{\omega T}{2}} H_I(e^{j\omega T})}{1 + \beta H_I(e^{j\omega T})} \left[e^{-j\frac{\omega T}{2}} sinc\left(\frac{\omega T}{2}\right) \right] \tag{3.18}$$

where sinc(x)=sin(x)/x and ω=2πf with $f < f_{ck}/2$.

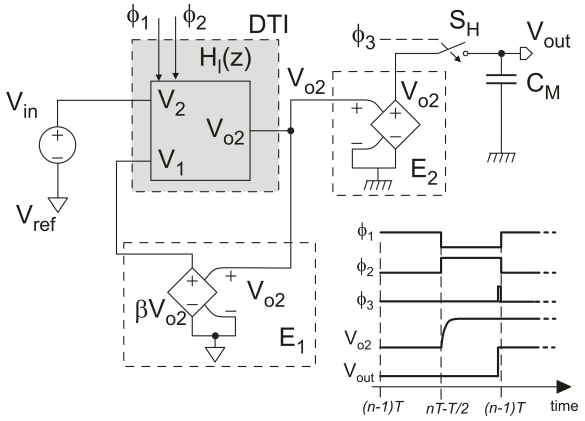


Figure 3.10: *Test bench used to simulate the integrator frequency response with sketch of the main waveforms (bottom-right).*

Inverting 3.18, $H_I(e^{j\omega T})$ was estimated from $H_{CL}(\omega)$, obtained with the PAC simulations. The feedback factor β was set to 10^{-3} to reduce the sensitivity to the simulator accuracy. Fig.3.11 shows the discrete-time frequency response (magnitude and phase) of the integrator in Fig.3.9, obtained with a clock frequency of 1 MHz, V_{dd} = 0.9 V and three different C_S/C_F ratios. The dc gain is around 85 dB, which is slightly lower than the theoretical limit. Preliminary investigation showed that this discrepancy is due to parasitic charge transfer caused by the drain-body and source-body capacitances of the transmission gates.

The curves in Fig.3.12 represent the magnitude and phase difference between the electrical simulations performed on the prototype of Fig.3.9 and the discrete-time simulations of previous section (Fig.3.6), for the particular case $C_S/C_F = 1/4$, and different combinations of supply voltage, clock frequency and C_S value. Starting from the case f_{ck}=1 MHz and V_{dd}=0.9 V, the gain discrepancy varies between -1 dB and -2 dB across the whole input frequency range. A noticeable discrepancy between the phase responses progressively develops at high frequencies. Both phenomena can be ascribed to incomplete charge transfers between capacitors due to the transmission gate on-resistance and/or limited bandwidth of the inverter-like amplifiers. This is confirmed

by the curve obtained by keeping the same supply voltage and slowing down the clock to 100 kHz. In this case, both the gain and phase differences are strongly reduced. Errors at high frequencies can be reduced also by keeping the same clock frequency (1 MHz) and scaling down all capacitors by a fixed factor. The result for a scaling factor of 0.5 is shown in Fig.3.12 (dotted curve). However, this operation degrades the dc gain, due to the higher sensitivity to the mentioned stray charge paths caused by parasitic capacitances. The possibility of operation at reduced supply voltage is proven by the curve at V_{dd} = 0.6 V. In this case, the clock frequency was reduced to 50 kHz to maintain acceptable performance.

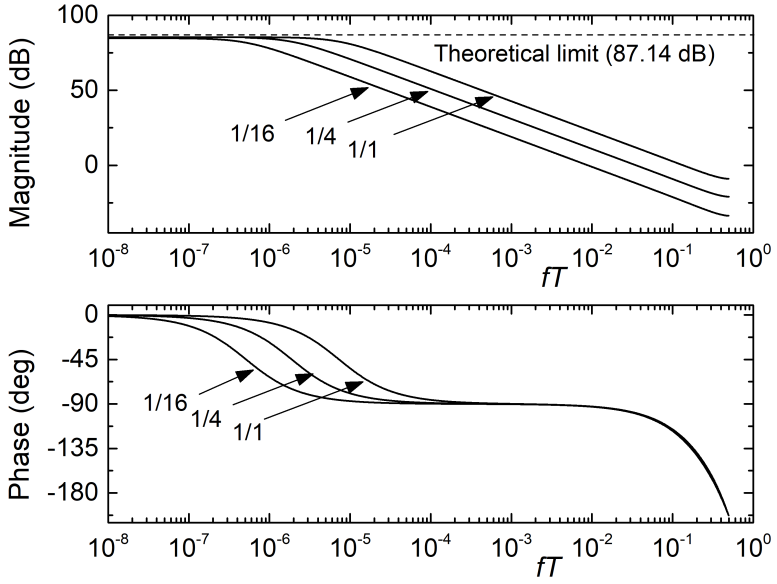


Figure 3.11: *Magnitude and phase response extracted from electrical simulations performed on the circuit of Fig.3.9, for V_{dd}=0.9 V, f_{ck}=1 MHz, and three different C_S/C_F ratios indicated with labels.*

In particular, the dc gain loss at V_{dd} = 0.6 V is only 2 dB. The supply current is 5.6 µA at V_{dd} = 0.9 V and drops to 140 nA at V_{dd} = 0.6 V. Fig.3.13 shows the result of 100 Monte Carlo transient simulations, including both global and local variations, performed on the integrator mounted in unity-gain, closed-loop configuration, implementing a first-order, lowpass filter (cut-off frequency = 40 kHz). In the first 5 µs, C_F is shorted by means of an auxiliary switch (not shown in Fig.3.9), so that V_{OUT} coincides with V_{INV} of INV-2. The high initial dispersion is recovered by the mentioned CDS mechanism, and the final dispersion is shown by the histogram. Finally, the impact of the inverter non-linearity was characterized by stimulating the same first-order filter as in Fig.3.13 with a 1 kHz sinusoidal waveform of 0.7 V peak-to-peak magnitude (78% of V_{dd}), obtaining a THD of -56 dB (15 harmonics) that drops to -65 dB if f_{ck} is reduced from 1 MHz to 500 kHz.

3.3.7 Employment as time-continuous operational amplifier

The proposed SC integrator presents important features that allows its employment as a time-continuous operational amplifier. First of all, the integrator output is always valid, despite the implementation of a CDS technique to reject offset and flicker noise.

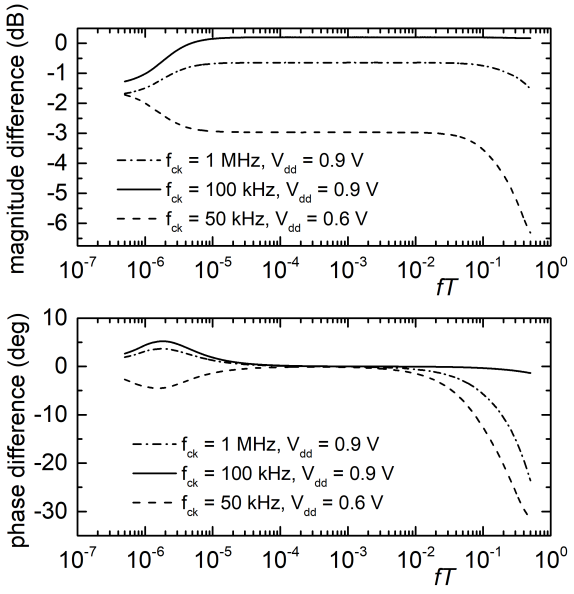


Figure 3.12: *Magnitude and phase difference between the discrete-time and electrical simulations for C_S/C_F =1/4 and different clock, supply voltage and capacitance C_S combinations, indicated in the figure.*

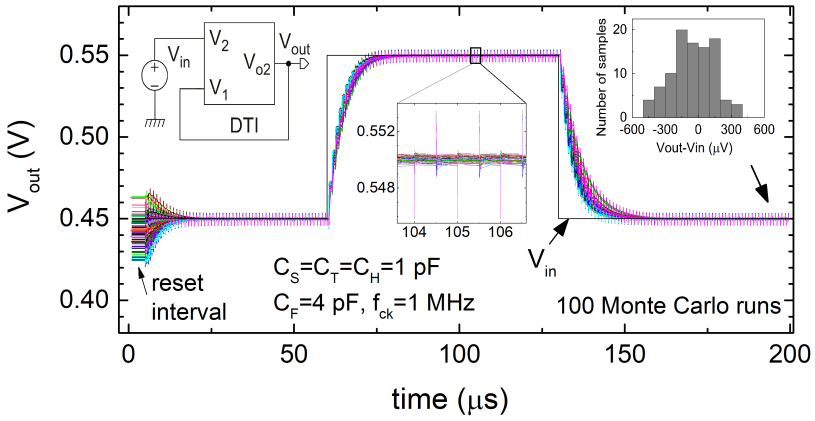


Figure 3.13: *Results of 100 Monte Carlo runs performed on the test bench shown in the left inset (unity gain, low pass filter), stimulated with a 70* μs *pulse of 100 mV magnitude. The histogram on the right shows the dc error distribution estimated over 100 Monte Carlo runs.*

It presents two input terminals, a non-inverting terminal (V_2) and an inverting terminal (V_1). Furthermore, it shows a very high dc gain due to the presence of C_H and a very high input impedance due to the use of the same capacitor C_S for both the input terminals. Of course, a limitation on the signal input bandwidth must be provided by means of an anti-alias filter, because of the sampling operation that is introduced.

The integrator transfer function in the z-domain is 3.12. We can express it in the frequency domain, considering also the hold function of the integrator:

$$H(f) = k\frac{e^{-j2\pi fT_{ck}}}{e^{-j2\pi fT_{ck}}2jsin(pifT_{ck})e^{j2\pi fT_{ck}}}sinc(fT_{ck}) = k\frac{e^{-j2\pi fT_{ck}}}{2j\pi fT_pck} \tag{3.19}$$

where k is the capacitive ratio C_S/C_F. H(f) is equivalent to the frequency response of an ideal time-continuous integrator, with an additional delay of one clock cycle. This frequency response is applied to the (differential) input signal after sampling. If the Nyquist-Shannon condition is ensured, then the discrete-time integrator behaves as a time-continuous integrator.

If we employ the TD integrator in a feedback network as the one in Fig.3.14, we obtain:

$$V_{out}(z) = (V_{in}(z)z^{1/2} - \beta V_{out}(z))\frac{kz^{-1}}{1-z^{-1}} \tag{3.20}$$

$$H_f(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{kz^{-1/2}}{1-z^{-1}(1-\beta k)} \tag{3.21}$$

The z-transfer function of the integrator in negative feedback configuration $H_f(z)$ is the one of an amplifier with low-pass response, with dc gain $1/\beta$ and cut-off frequency in $f_p = f_{fck}/(2\pi(1-\beta k))$. For $k = \beta = 1$, for example, the circuit acts as a half cycle delay. It can be considered a time-continuous buffer which introduces a linear phase delay and it performs the zero-hold function. With $\beta < 1$, the circuits shows a certain amplification β^{-1} and a low-pass filtering response. Actually, sizing properly the product βk is possible to move the cut-off frequency of the circuit to infinity even keeping the amplification constant. Stability of the amplifier is guaranteed if $\beta k \leq 1$.

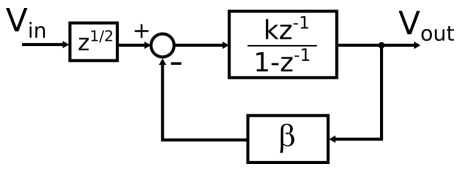


Figure 3.14: *Block diagram of the proposed DT integrator in negative feedback configuration, with a feedback network β.*

3.4 ULV Data Converter

As already mentioned, technology scaling of the last years has seen the scaling also of the maximum supply voltage. With the shrinking of channel lengths of MOSFET devices, also the width of the gate oxide has been reduced, forcing a decrease of the maximum electric field allowed, and then to the maximum supply voltage. Last technology nodes allows maximum supply voltages for the core devices already below 1 V from 32 nm node, and I/O supply from 1.1 V to 1.8 V. The smaller channel lengths together with the lower supply ranges have leaded to huge benefits for the digital circuits, as correctly foreseen by the Moore's Law. The scaling of dynamic and leakage power, together with the improvement of switching performance and, of course, of the area density are the main benefits from the advancement towards new technology

nodes. However, the design of analog/RF blocks, necessary even in mainly digital chips, like bandgap voltage references, temperature sensors, sense amplifiers for memory cells, PLL, analog-to-digital converters, has become more and more challenging. Several non-idealities of MOSFET devices with channel length lower than 100 nm are detrimental for analog blocks, like short-channel effects, well proximity effects, shallow trench isolation stress effects and so on. Even device modelling is not optimized for analog design. Furthermore, small channel lengths unavoidably reduce MOSFET intrinsic gains, while the supply voltage scaling, not followed by threshold voltage scaling (at least not with the same steepness), limit the voltage headroom for the transistors and the number of circuit topologies available in analog design. Smaller dimensions, of course, lead also to greater variability of neighbour MOSFETs on the same die. Furthermore, even typical digital issues like clock, power and data distributions in digital cores are becoming more and more analog problems.

A part from the problem related to the Moore's law, low-voltage design is also very interesting in More-than-Moore applications. In the last years, in fact, several emergent applications have started requiring electronic circuits able to work with supply voltages lower than 1 V down to few hundreds of mV. Energy scavenger able to take energy from the human body through could provide supply voltages as low as 0.38 V. Design of analog front-end for sensor interfacing at such low frequency, providing sufficient resolution and accuracy, is a great challenge. Working with supply voltage on the order of the threshold voltage means necessarily to work with MOSFET devices biased in weak inversion or even in deep subthreshold region. Very low headroom, low driving capability and small bandwidths are the main concerns in ULV design, and ADCs are not an exception.

Several works have been presented in the literature to exploit low-voltage or ultra-low voltage operations. SAR converters, due to their intrinsically similarity with digital operations (most of the operations, in fact, are realized after the comparator decision, in the digital domain), can match quite well the supply voltage scaling [106], [107]. The main limitations are given by the design of an ULV comparator with decent performances in terms of speed and noise. Similarly, full-flash converters may reach supply voltage as low as 0.2 V [108]. Converter architectures implying linear amplifiers, such as pipeline or two-step converter, may be penalized by the supply scaling. DT Δ-Σ modulators, for example, requires amplifiers to realize the switched-capacitor integrators. Several inverter-based solutions have been presented in the literature [96,97,109–112], capable to reach high performances due to high-order topologies or dynamic biasing techniques. Other interesting topologies as VCO-based Δ-Σ modulators take advantage from the intrinsic digital nature and the time-based architecture of a VCO-based quantizer and can reach higher sampling frequency [32, 113].

3.5 Proposed ULV Δ-Σ Modulator

The proposed two-stage SC integrator described in paragraph 3.3 presents several features that match perfectly the requirements of a discrete-time Δ-Σ modulator. In particular, the high dc gain and the CDS technique reduce significantly the complexity of ULV design. As well known, high dc gain reduces the amplitudes of the dead-zones and the gain error of the converter. CDS technique, on the other hand, allows the re-

jection of offset and low-frequency noise, particularly detrimental in sensor interfacing applications, where the bandwidths of interest go from dc to few hundreds of hertz or kilohertz. Here, the description of a DT Δ-Σ modulator suitable for supply voltage as low as few hundreds of millivolts is presented [114].

For the sake of simplicity, we chose the typical discrete-time (DT), second order, Cascade of Integrator FeedBack (CIFB) modulator. This architecture is depicted in the block diagram of Fig.2.6, where INT1 and INT2 are the first and the second integrator, respectively; ADC is simply a comparator and DAC is a 1-bit Digital to Analog Converter. A schematic view of the proposed single-ended, inverter-based implementation is shown in Fig.3.15. Supply rails for the inverters are V_{dd} and ground, with the exception of the inverters in the DAC, for which the power supply is the reference voltage of the converter (V_{ref}), which sets the full-scale range. V_{inv} represents an additional floating rail, which is simply generated by a unity-gain connected inverter (I9 in Fig.3.15). In addition, as far as quantization noise floor and dead zones are concerned, this Δ-Σ structure behaves as a fourth order modulator, while maintaining the stability properties of a second order one.

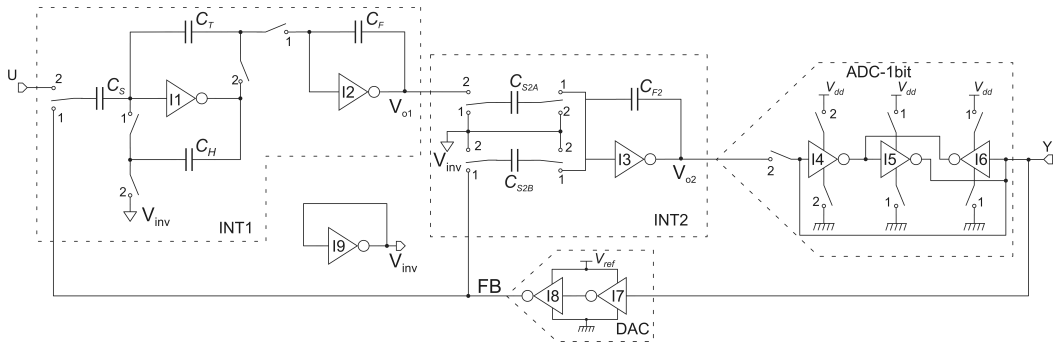


Figure 3.15: *Schematic view of the 2nd order, inverter-based, Δ-Σ Modulator.*

3.5.1 First integrator INT1

The behaviour of the proposed DTI is here recapped, highlighting only the interesting features concerning Δ-Σ modulators. INT1 is composed by two stages: the first stage samples the difference between the global input (U) and the feedback voltage (FB) into C_S and transfers the corresponding charge into C_T. Then, the second stage receives this charge, which is transferred into C_F, realizing the required DT integration. The z-domain transfer function of the proposed integrator is the following [102]:

$$H(z) = \frac{V_{o1}(z)}{U(z)z^{1/2} - FB(z)} = \frac{C_S}{C_F}\frac{z^{-1}}{1 - z^{-1}} \tag{3.22}$$

It can be observed that the input U is sampled with a half clock cycle lead (factor $z^{1/2}$) with respect to FB. The purpose of C_H is to hold the output voltage of I1 during phase 1, reducing the charge-transfer sensitivity to the dc gain of I1 from a $1/A_0$ to a $1/A_0^2$ dependence [103]. Considering also the second stage, formed by I2, it can be easily shown that the overall dc gain of the proposed integrator is proportional to A_0^3. This means that, even employing inverter-like amplifiers with minimum-length devices (showing very low dc gain, e.g. A_0 = 26 dB), the overall dc gain of INT1 may approach

80 dB. In addition, all mentioned charge transfer acts involve a CDS mechanism, so that offset and low frequency noise of the inverters are rejected. The dominant contribution to INT1 offset is due to the mismatch between the switching threshold of I1 and V_{inv}. Fortunately, the Referred-To-Input (RTI) contribution of this mismatch is divided by I1 dc gain and thus its effect is significantly reduced. Coefficients a_1 and b_1 in Fig.2.6 are equal and are given by the capacitive ratio C_S/C_F.

3.5.2 Second integrator INT2

INT2 is a typical parasitic-insensitive, inverter-based integrator. Its low dc gain A_0 is not critical, thanks to the contribution of the first integrator, which allowed us to reach an adequate overall dc gain for modulator loop filter. Its offset, even if not rejected with a specific dynamic cancellation technique, gives a negligible contribution since it affects the ADC input through division by the high dc gain of INT1. The two coefficients c_1 and a_2 coincide with the capacitive ratios C_{S2A}/C_{F2} and C_{S2B}/C_{F2}, respectively.

3.5.3 ADC and DAC

The 1-bit ADC in the Δ-Σ loop is the clocked comparator of Fig. 3.15 (ADC-1bit). In phase 2, the output of the second integrator is amplified by the inverter-like amplifier I4; then, in phase 1, the output of the second integrator and its amplified version provide the initial unbalance to the two cross-coupled inverters I5 and I6. The positive feedback ensures a decision fast enough; the reset of the latch I5-I6 and amplifier I4 in the alternative phases guarantees no hysteresis of the comparator. The correct data is present at the end of phase 1, that is also the moment when INT1 and INT2 samples the feedback signal. In phase 2, the output of the ADC corresponds to the output of INT2. The output of the comparator is fed back through the DAC, which is simply the cascade of two inverters. The feedback signal FB is, thus, a two-level quantized signal, assuming V_{ref} or zero as value. In this work, we adopted the supply voltage V_{dd} as V_{ref}.

3.5.4 Clock boosting

The very low supply voltage forced us to size the inverters employed in the integrators, in the comparator, and in the DAC with a great W/L ratio. This was done in order to increase the bias currents, which are usually very low when operating in subthreshold region. Another critical aspect was represented by the on-resistance of the MOSFETs that were used to implement the switches, which worked in subthreshold region with an even smaller overdrive voltage than the inverter devices. This issue was made worse by the need of avoiding minimum channel lengths to reduce leakage in the off state of the switch. Therefore, the very high W/L ratios necessary to obtain reasonable on-resistances led to pass gates with very large gate areas. This resulted in an excessive capacitive load for the clock drivers and in critical charge injection problems that could not be satisfactorily compensated by the insertion of dummy-switches. To overcome these issues, we designed an original clockboosting circuit (Fig.3.16-a), which improved the clock signal levels and accelerated the capacitor charges and discharges. This circuit behaves like a positive and negative charge pump, being able to boost both high and low level of the clock signal. When the input clock signal clk is high, C_{UP} is charged to V_{dd}; analogously, when clk is low, C_{DOWN} is charged to $-V_{dd}$.

Then, in one phase, a voltage equal to the supply is added to the input clock signal, while in the other phase it is subtracted from the clock. The net result is that the high clock level becomes ideally $2V_{dd}$, while the low one is $\breve{}V_{dd}$. The implementation of the two switches driven by clk and its negated version is not straightforward, due to the level-shifting of the clock levels. For these reasons, transistors M2-M3 and M5-M6 implements a sort of bootstrapping technique, providing the correct value to turn-on the switches (0 for the PMOS M1, V_{dd} for M4), while to turn them off, the gate-source voltage is forced to zero.

Due to the exponential characteristic in subthreshold region, this introduces a dramatic improvement of the on-resistance of both n and p MOSFETs of the switches and at the same time reduces leakage in the off-state. Since the proposed Δ-Σ modulator requires a two non-overlapping phase clock, and each phase consists of two complementary signals, four individual clockboosting circuits are used.

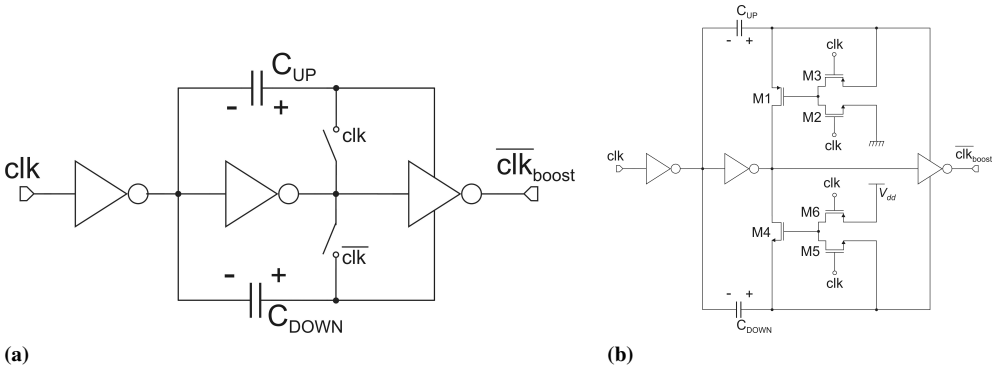


Figure 3.16: *a) Simplified schematic view of the proposed clock boosting circuit. b) Complete schematic view of the proposed clock boosting circuit.*

3.5.5 Device sizing

The structure previously described was designed with the UMC 0.18 μm process using the software Cadence Virtuoso™. We reported the size of every MOSFETs in Table 3.3. All the inverter-like amplifiers present in the circuit were nominally identical, with the exception of the DAC inverters that could be designed with smaller aspect ratios without affecting the maximum clock frequency of the ADC. Table 3.4 lists the sizing of the capacitors employed in the modulator. The values of C_T and C_H were chosen equal to C_F to avoid the saturation of the output voltage of I1 (Fig. 3.15), which may increase the harmonic distortion of the converter.

Similarly to what has been described in 2.3.1, the value of C_S has been chosen to meet the requirements of resolution, area and power consumption. Targeting medium resolution and wanting to develop an ultra-low power modulator, a value of 106 fF has been chosen.

3.5.6 Simulation results

The modulator was simulated by means of the Cadence Spectre™ electrical simulator to prove its functionality and to verify robustness against temperature and pro-

Table 3.3: *Sizing of MOSFET devices*

	L_{nMOS}	W_{nMOS}	L_{pMOS}	W_{pMOS}
Inverters	180 nm	12.6 µm	180 nm	50.4 µm
Pass gates	180 nm	960 nm	180 nm	1.92 µm
Inverters (DAC)	180 nm	5 µm	180 nm	10 µm

Table 3.4: *Capacitor values*

C_S	$C_T = C_H = C_F$	C_{S2A}	C_{S2B}	C_{F2}
106 fF	1 pF	187 fF	70 fF	1 pF

cess variations. In all the tests, we chose $V_{ref} = V_{dd}$ while the oversampling ratio $OSR = f_{ck}/(2B_W)$ was set to 128, where B_W is the bandwidth of the input signal and f_{ck} is the clock frequency (oversampling frequency). With $f_{ck} = 20kHz$, B_W resulted to be 80 Hz, which is suitable for interfacing a wide variety of sensors. Fig. 3.17 shows the Power Spectral Density (PSD) of the output bitstream for V_{dd} = 0.3 V and an input tone of -12 dBFS at a frequency of 10 Hz. The result of a transient simulation performed taking into account electrical noise (transient noise simulation) is compared with a standard (noiseless) transient simulation. The significant contribution of the electrical noise (mainly amplifier and kT/C noise) is well visible in the baseband. The Signal to Noise and Distortion Ratio (SNDR), estimated from the transient noise simulation, was found to be 69.9 dB over the bandwidth of 80 Hz, and the corresponding Effective Number Of Bits (ENOB) was 11.32. The average power dissipated by the whole modulator (including the nonoverlapping clock generator and the clock boosting circuits) P_D was only 15.47 nW, thus resulting in the following Figure Of Merit (FOM):

$$FOM = \frac{P_D}{2^{ENOB} 2B_W} \tag{3.23}$$

Transient simulations performed by varying the operating temperature showed that the SNDR is practically constant over the 0 °C – 110 °C interval. For lower and higher temperatures, the SNDR starts to drop due to bias current decrease (low temperatures) and junction leakage increase (high temperatures). Corner analysis did not show critical issues with the exception of the slow-p, slow-n corner, where the estimated SNDR loss was around 20 dB. In this case, the problem was due to excessive reduction of the inverter bandwidth. Slowing down the clock frequency to 10 kHz lead to a partial recover (10 dB) of the SNDR.

Comparison with an ADC based on standard integrators

In this paragraph we will highlight the benefits of using our original two-stage integrator, instead of a classic topology. Therefore, in the schematic of Fig.3.15, we replaced the first integrator with a simple parasitic insensitive one, which had a much lower dc gain. We will call this modulator MOD-Standard. Performances of MOD-Standard were poorer as the SNDR decreased to 64.8 dB in the same simulation conditions of Fig.3.17, considering also electrical noise. Fig.3.18 compares the dc behaviours of the proposed modulator and of MOD-Standard. It is evident from the inset of the absolute

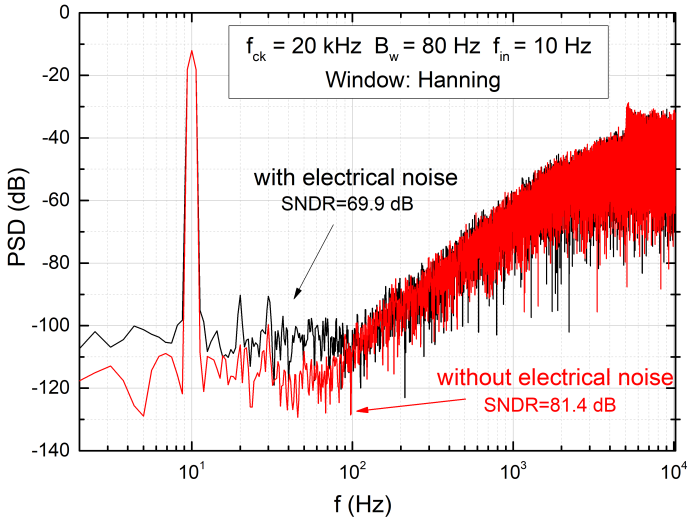


Figure 3.17: *Comparison of the Power Spectral Densities of the proposed modulator with and without electrical noise. The input signal is a sinusoidal waveform with amplitude -12 dBFS at 10 Hz.*

error and from the different slopes of the dc characteristics that the gain error of the proposed modulator is much lower, thanks to the high dc gain of the first integrator. In order to demonstrate the effectiveness of the CDS technique of the proposed integrator, we run 20 Monte Carlo simulations that showed an RTI-offset standard deviation of our modulator of about 925 µV, while the standard deviation of MOD-Standard offset was around 3 times higher. However, the offset spread of our modulator was higher than the value that could be estimated considering only the mismatch of the inverter switching voltages. The excess offset is probably due to charge injection mismatch between switches and dummy switches.

Performances at 0.5 V supply voltage

The modulator was designed and optimized for working with a supply voltage of 0.3 V. Increasing it did not affect the SNDR (and then the resolution) but the maximum operating frequency increased as well, as expected. This is proven in Fig.3.19, where the behaviour of the SNDR as a function of f_{ck} at $V_{dd} = 0.5V$ (red curve) is compared with the case of $V_{dd} = 0.3V$ (black curve). Note that the SNDR starts to drop for frequencies greater than 30 kHz for V_{dd} = 0.3 V, whereas the SNDR drop is shifted up by more than one order of magnitude for V_{dd} = 0.5 V. Obviously, the power dissipated also increased with the supply voltages, due to the exponential dependence of the inverter bias current with V_{dd}. Nevertheless, the power dissipation for V_{dd} = 0.5 V was still around 350 nW, preserving suitability for low power applications.

Comparison with the state of the art

Table 3.5 compares the performances of the proposed Δ-Σ modulator with other works on this subject. Our work showed an excellent FOM mainly due to the exceptionally low power consumption. This is true for both the supply voltages that we considered.

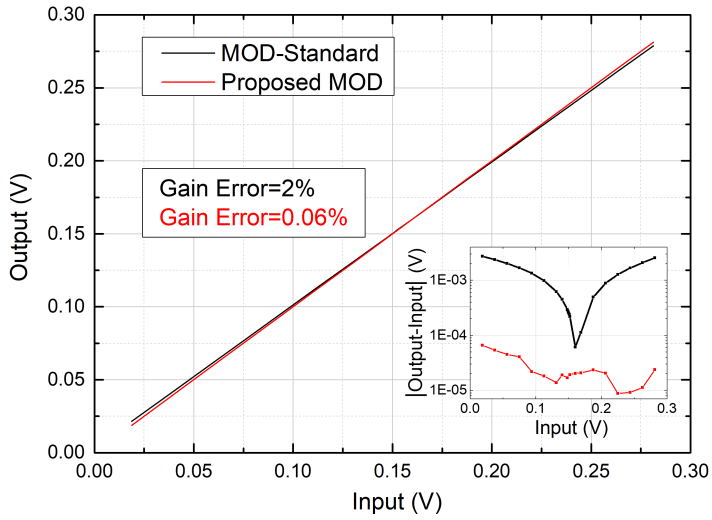


Figure 3.18: *Comparison of the dc performances of the modulator using: the standard integrator (black curve) the proposed integrator (red curve).*

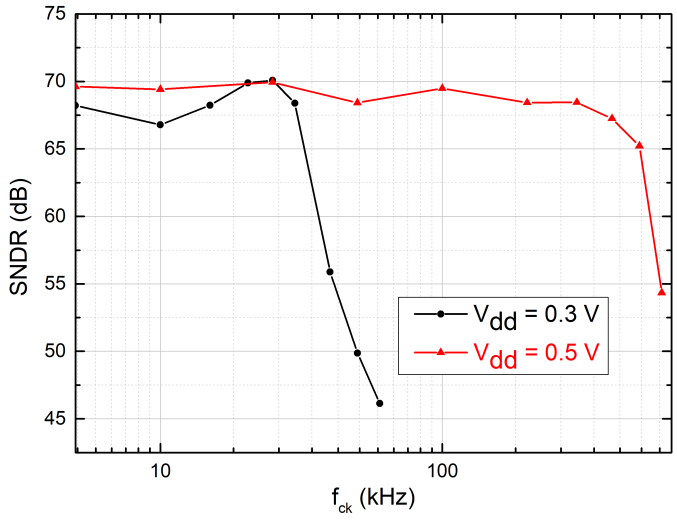


Figure 3.19: *SNDR vs. clock frequency, with V_{dd} = 0.5 V and with V_{dd} = 0.3 V.*

On the other hand, the signal bandwidth was one of the lowest, although it was appropriate for interfacing a wide range of sensors (e.g. temperature, atmospheric or tire pressure, chemical sensors). It should be observed that some designs included also the digital power dissipation, while we considered only the power dissipated by the modulator.

Table 3.5: *Comparison with other ULV Δ-Σ Modulators*

	This work	This work	[110]	[111]	[112]
Technology	0.18 µm	0.18 µm	65 nm	0.13 µm	0.18 µm
V_{dd} [V]	0.3	0.5	0.7	0.25	0.3
B_W [Hz]	80	800	20k	10k	62
P_D [nW]	15.5	353	15210^3	7.510^3	37
$SNDR$ [dB]	69.9	68.4	89	61	53.3
FOM [fJ/step]	38	103	165	410	790

3.6 Measurement results

In this section, measurements effectuated on a silicon prototype of an ULV Δ-Σ converter are shown. To prove the effectiveness of the proposed SC inverter-like integrator, for the sake of simplicity a first Δ-Σ modulator on UMC 0.18 µm process has been designed. Even if 1st order modulators present several limitations, mainly due to the high sensitivity to the integrator finite dc gain, thanks to the appealing features of the proposed ULV block. Moreover, the first order modulator is the most compact Δ-Σ ADC and can find application in high-volume testing for complex SoC as [115]. Compared to the modulator of Fig.3.15, the parasitic-insensitive integrator implementing INT2 has been suppressed, keeping the same structure and sizing for the first integrator, the comparator and the DAC. The same CIC filter already described in the previous chapter has been exploited also to filter the bitstream of this modulator, before proper translations of the digital levels to 1.8 V, the supply compliant with the digital core. Here, preliminary measurements to characterize the static and dynamic performances for different supply voltages are shown. The design has been optimized for working at $V_{dd} = 0.3V$. However, supply voltages as low as 0.2 V and up to 0.7 V have been tested. The picture of the final layout is shown in Fig.3.20, where it is possible to notice the compact dimensions of the whole modulator.

The modulator is inside the same test-chip described in Chapter 2. The supply voltage of the modulator is separated from the rest of the chip and it is provided from a specific pad. The same generation of the clock has been used, except for the level-shifting of the clock levels from the digital voltage (1.8 V) to the modulator supply voltage. A measurement set-up similar to the one already described in Chapter 2 has been used, with the difference of the single-ended input.

3.6.1 DC characteristics

Fig.3.21 shows the output code of the converter for different oversampling frequencies, with dc input voltage equal to half of the full-scale (i.e. the V_{dd}). The measurements have been repeated for different supply voltages. It is evident how, for high sampling frequency, the modulator is not able to work properly, as it can be recognized from the sudden drop of the output of the filter. For the different supply voltages, a maximum sampling frequency can be identified, and they are shown in Table 3.7.

Fig.3.22 shows the dc characteristics for different supply voltages. It is worth remarking the characteristic reported for $V_{dd} = 0.208V$. Even if the measure has been effectuated on a single sample, and the modulator is able to work only with oversam-

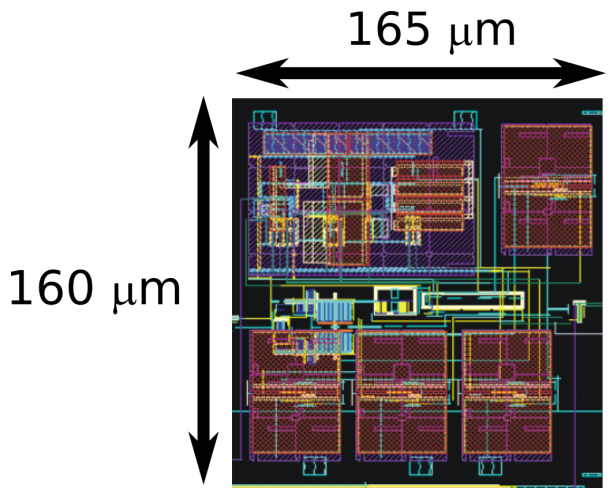


Figure 3.20: *Layout of the converter prototype designed in UMC 0.18* μm *CMOS process.*

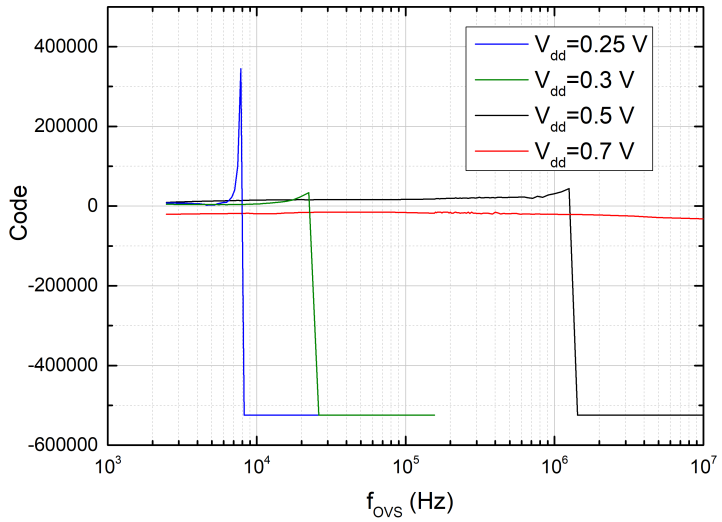


Figure 3.21: *Output code (on 20 bit word) with a dc input equal to $V_{dd}/2$, sweeping the oversampling frequency f_{ovs} for different V_{dd}.*

pling frequency lower than 3 kHz, still we are able to distinguish the functionality of the ADC, even if optimized for a higher supply voltage. Fig.3.23 shows the INL for the different supply voltages, while a recap of the static performances of the converter has been reported in Table 3.6. Offset values higher than expected from simulations have been measured, despite of the CDS technique implemented. From preliminary investigations, the cause of the offset arising is to be found in mismatch of charge injections in the SC integrator. FD implementations should mitigate this issue.

3.6.2 Spectrum analysis

From FFT analysis of the output bitstream, it is possible to evaluate the SINAD and then effective resolutions of the proposed converter. The measurements have been repeated for the different supply voltages and the obtained spectrums are shown in Fig.3.24, in the range from 0.25 V to 0.7 V. Table 3.7 reports a recap of the dynamic performances

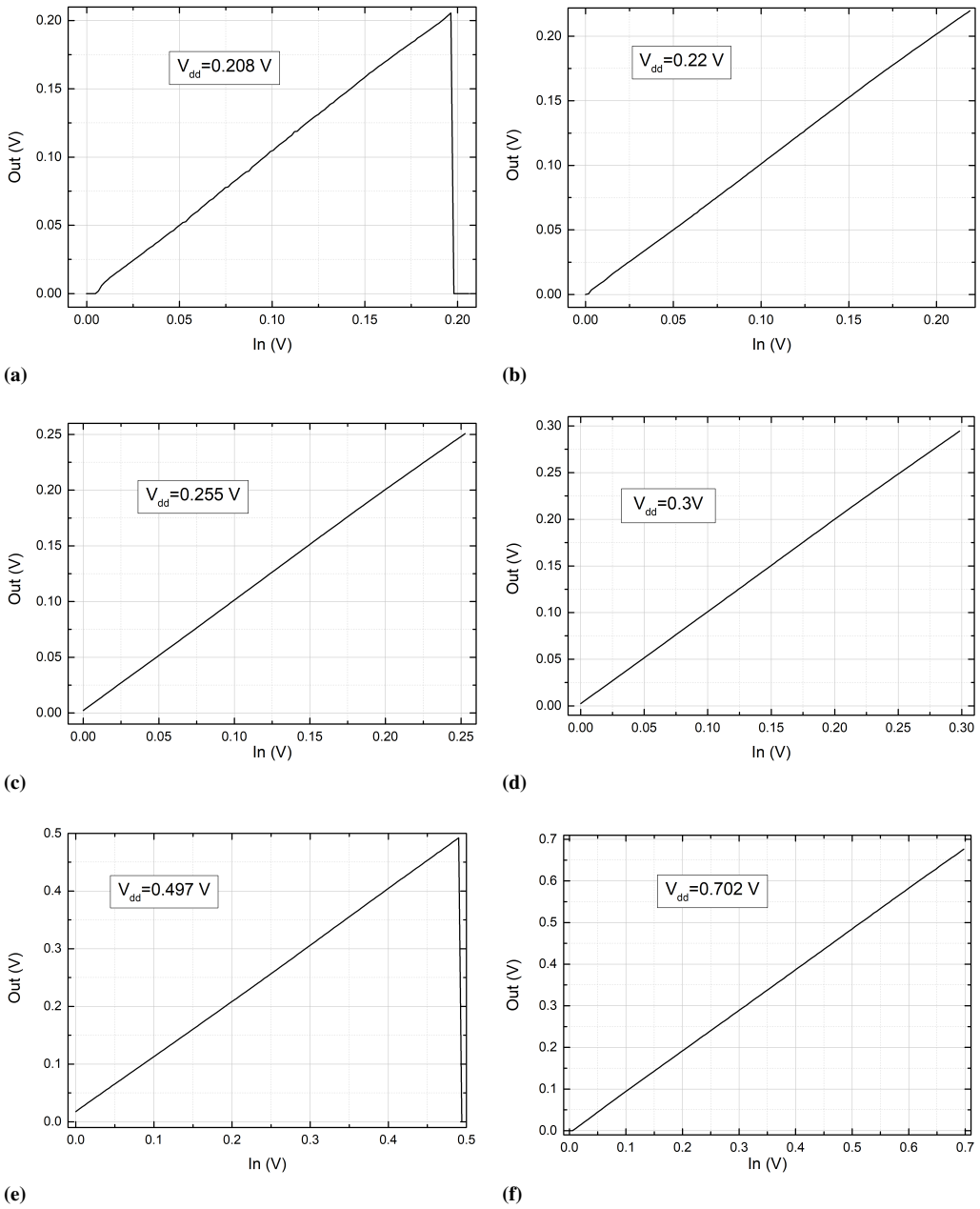


Figure 3.22: *DC characteristics for different supply voltages.*

Table 3.6: *Summary of static performances for different supply voltages.*

Supply Voltage (V)	Offset (V)	Gain error (%)	INL (LSB on 7 bit)
0.208	-5.6 m	3.75	1.68
0.22	-6.5 m	0.3	1.35
0.255	-7.2 m	1.66	0.67
0.3	-8.6 m	2.16	0.54
0.497	3.9 m	3.16	0.87
0.702	-19.6 m	2.17	0.88

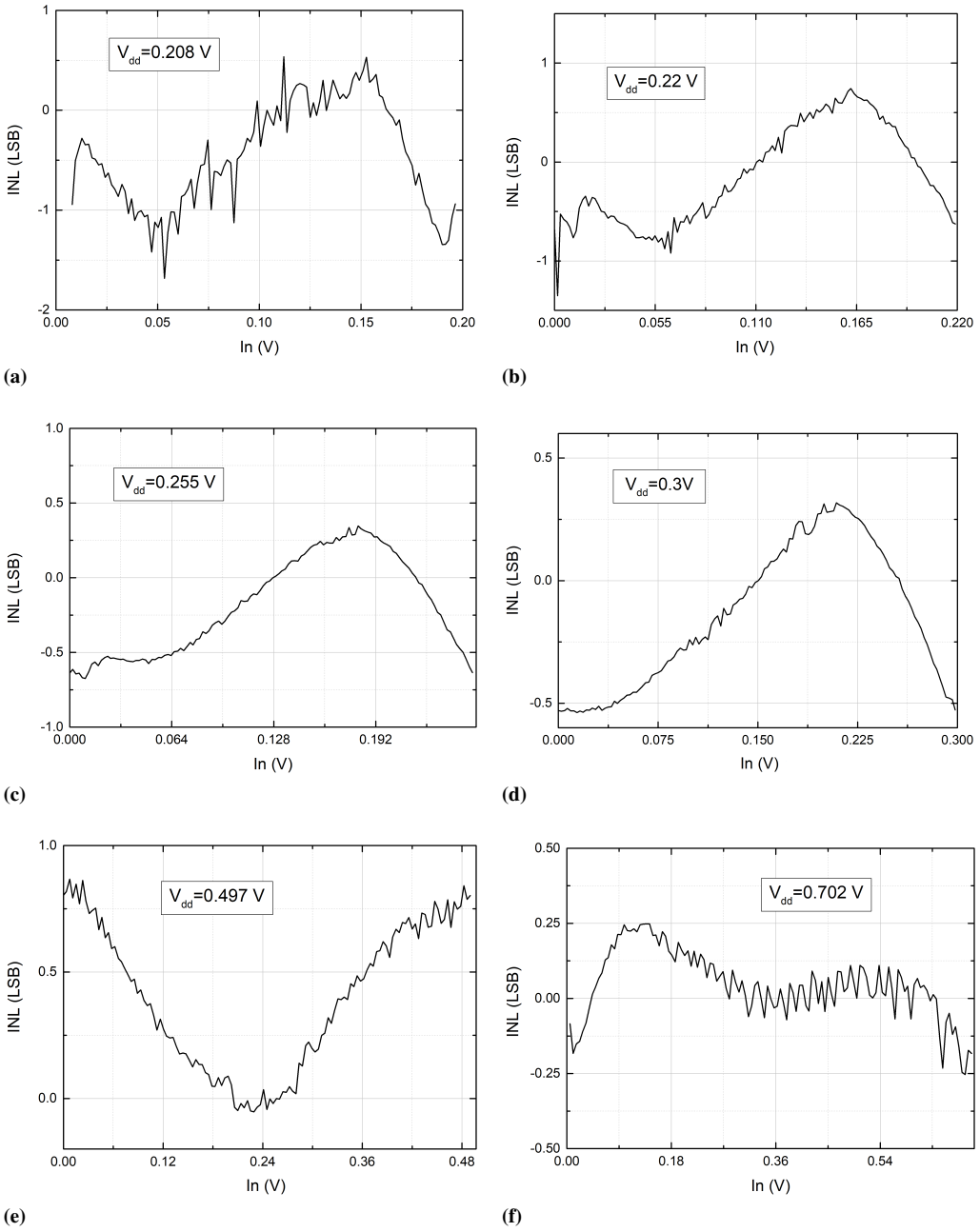


Figure 3.23: *INL for different supply voltages.*

and the power consumption of the proposed ULV converter at the different supply voltages. FoM_W of 147 fJ/conv at 0.25 V is very promising, in the optics to implement the 2nd order modulator already proposed in [114]. For higher supply voltages, higher power consumptions limit the FoM_W, as expected due to the employment of class-AB inverters as amplifiers, sized with high W/L aspect ratios to reach sufficiently high GBW at the lowest supply voltages.

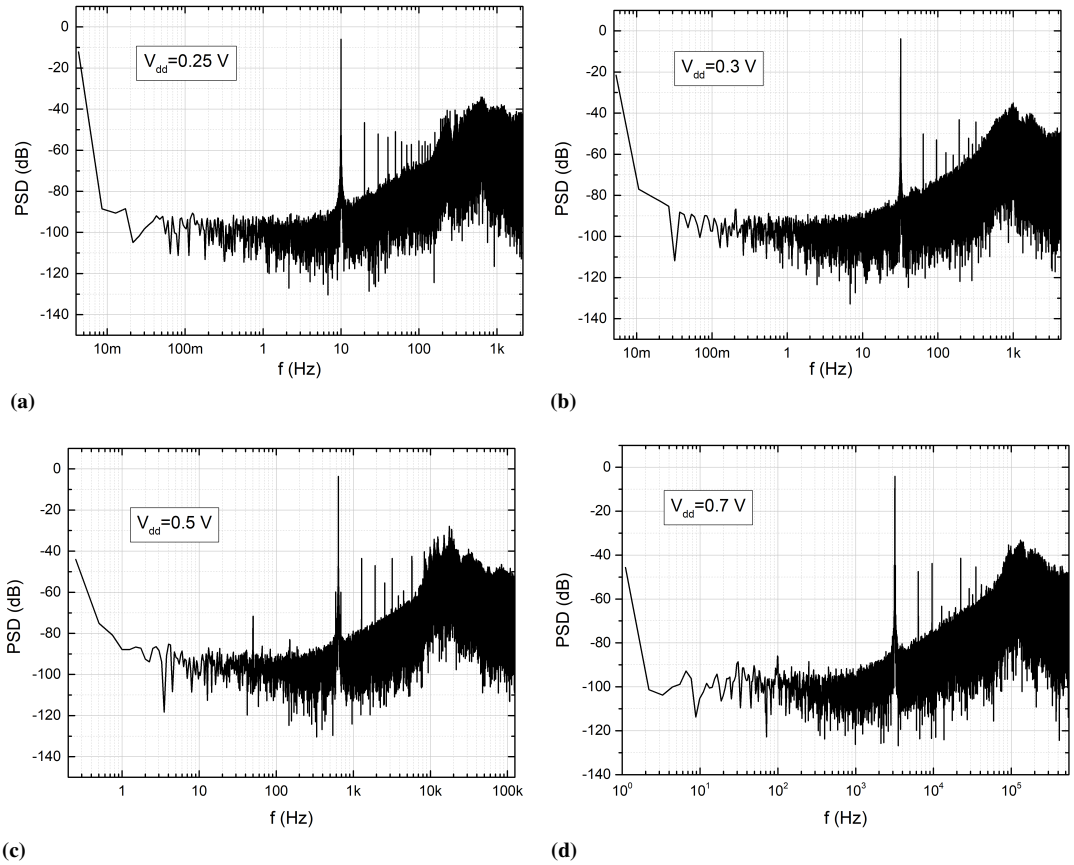


Figure 3.24: *Spectrum results at different supply voltages, sampling frequencies and input tone frequencies. a)* $V_{dd} = 0.25V$*;* $f_s = 4.3kHz$*;* $f_{in} = 12Hz$*. b)* $V_{dd} = 0.3V$*;* $f_s = 8.6kHz$*;* $f_{in} = 32Hz$*. c)* $V_{dd} = 0.5V$*;* $f_s = 250.7kHz$*;* $f_{in} = 640Hz$*. d)* $V_{dd} = 0.7V$*;* $f_s = 1.1MHz$*;* $f_{in} = 3.2kHz$

3.7 Discussion and conclusion

In this chapter, the full description of an Analog-to-Digital Converter capable of working with ultra-low supply voltages, thought for energy harvesting scenarios, is provided. First, general considerations about microelectronic design in the presence of small supply voltage ranges are given. A novel switched-capacitor integrator capable of reaching very high dc-gain even employing low-gain amplifier allowed the realization of a full inverter-like Δ-Σ modulator optimized for working with V_{dd} = 0.3 V. Furthermore, the proposed integrator implements a correlated double sampling technique to reject offset and flicker noise. Measurements on a silicon prototype fabricated with UMC 0.18 μm CMOS process confirm the effectiveness of the proposed solution for a first order

Table 3.7: *Summary of dynamic performances for different supply voltages.*

Supply Voltage (V)	Max. Sampling Frequency (Hz)	P_d (W)	SINAD (@OSR=128) (dB)	FoM_W (pJ/conv)
0.25	5 k	1.5 n	51.4	0.147
0.3	17 k	10 n	48.46	0.688
0.5	1 M	1.27 µ	55.1	1.395
0.7	10 M	23 µ	53.3	7.084

modulator. Future works concern the design of the second order Δ-Σ modulator already proposed in [114] and proven by means of electrical simulations. Another improvement will consist in a fully-differential implementation, that can guarantee more robustness to common-mode disturbs and better linearity. The starting point will be the design of the fully-differential switched-capacitor integrator, that requires a FD inverter-like amplifier.

CHAPTER 4

Design of high-speed cryo-CMOS ADC for quantum computing

4.1 Introduction

Since the first time quantum computing was proposed [116], a lot of effort has been spent on searching and developing new devices for the implementation of the quantum bit (or qubit). A qubit is the basic building block of a quantum computer, i.e. the equivalent of a bit in traditional computers. Explaining the working principle of a quantum computer is far from the goal of this chapter. In the next section, only a brief introduction to quantum computing is provided, mentioning the possible applications where it would overcome the actual technology due to its exponential speed-up of computational power. A concise overview about the main differences between quantum and classical computing is presented, concentrating on one of the possible physical implementation of qubits.

The aim of this chapter, actually, is to make the reader aware of the challenging engineer problem related to quantum computing, in particular concerning the design of the electronic readout interface. First, the issues of designing integrated circuits for an extreme environment (i.e. for temperature down to 4 K), as requested for quantum computing applications, is presented. Then, the specifications for the qubit readout chain, and in particular about the ADC, will be drawn. Finally, the design of an ADC for radio-frequency (RF) reflectometry interface in qubit readout is explained, starting from the high-level specifications, dwelling upon the architectural choices and concentrating on the details of transistor-level design. This ADC aims to enrich the library of Intellectual Properties (IPs) for qubit readout designed in the Applied QUantum Architecture Department (AQUA) of TU Delft, where this project has taken place. Furthermore, if proven by experimental measurements, this circuit would be the first example

of high-speed ADC for cryogenic applications.

To the best of our knowledge, the fastest cryogenic ADC present in the literature is [117], proven to work at 15 K with an effective Nyquist rate of 30 MHz and an effective resolution of 6 bit. Being implemented in an FPGA, [117] has a power consumption of 750 mW, that is not comparable with the one of ASIC solutions. A flash converter [118] has been proven to work at 4.3 K with 8 bit of resolution at a sampling frequency of 12.5 kHz; a delta-sigma converter capable of working from room temperature (RT) to cryogenic temperatures [119] shows a resolution of 11 bit with a power consumption of only 70 µW, for an input bandwidth of 5 kHz.

Among the different ASIC data converters designed for cryogenic temperatures, the successive approximation ADC is the most popular, and in 4.3.1 the motivation will be given. SAR converters presented so far for cryogenic applications [120–126] show low-medium sampling frequency (maximum of 20 MHz), with medium resolution (up to 10).

The proposed SAR ADC targets a sampling frequency of 1 GHz, with a resolution of 6 bit and a maximum power consumption of 1 mW. Additional reconfigurability features have been implemented in order to explore different design spaces, facing the effects of cryogenic temperatures on a standard CMOS process and extend its feasibility also to different fields of applications.

4.2 Quantum computing

Quantum computing is a model of computation that is not based on the principles of classical mechanics, as a traditional computer. A quantum computer is implemented with qubits, the corresponding building block of classical bits for traditional computers. The main differences between classical bits and qubits are entanglement and superposition. Due to the latter, the value of the qubit, instead of being either 1 or 0, can be a superposition of the two, so that the actual value is represented as an array in the Bloch sphere (figure 4.1). Quantum operations on the qubit can be seen as rotations of the array. Moreover, qubits can be correlated one another, due to the entanglement effect, increasing exponentially the information that they can carry on.

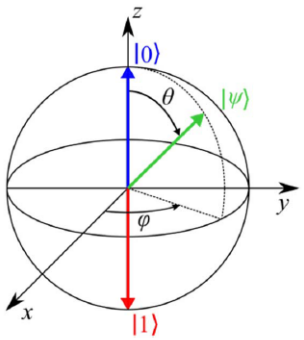


Figure 4.1: *Representation of the Bloch sphere, reproduced from [127].*

This exponential speed-up in computational power promises to solve complex problems that can not be faced with traditional computers. Fields like quantum cryptography, quantum simulations for synthesis of new drugs and materials and complex op-

timizations could be finally explored by means of quantum computers. If Neven's Law [128] will take over the Moore's Law [129], i.e. that the computing power (thanks to quantum computing) will increase with a doubly exponential rate instead of the well known doubling every two years of classical electronics, "quantum supremacy" will really come true.

However, there are several issues that make the realization of quantum computers still far from the reality. One of the most critical is related to decoherence. Due to the interaction with the environment, the quantum state of the qubit can be corrupted and the information lost. Every qubit technology, in fact, is characterized by the decoherence time, that is the average time qubit keeps the information. Decoherence time must be long enough to guarantee useful operations on the qubit before the lost of the information. In order to solve this issue, algorithms of Quantum Error Correction (QEC) has been implemented. As a fundamental principle of quantum mechanics, the measurement of the quantum state of a qubit is destructive due to the collapse of the quantum state. Furthermore, it is impossible to copy the state of a qubit on another qubit, as stated in the no-cloning theorem. The only way to have access to the qubit information is through the addition of extra qubits, called ancillary qubits. Thanks to the entanglement of the ancillary qubits with the data qubits, it is possible to detect and correct errors on the state of data qubits. Lot of effort has been spent in the recent years on QEC because of its importance towards the realization of useful quantum computers.

There are several implementations of qubits, based on different physical principles, that are promising candidates for a mature implementation of a quantum computer, according to the famous DiVincenzo's criteria [130]: superconducting qubits [131, 132], spin qubits [133], ion-based qubits [134, 135] and diamond-based qubits [136]. At the moment, the most mature technologies are based on transmons, a type of superconducting charge qubit, and spin qubits. In this work, we will concentrate our attention on the latter topology, due to its advantageous small dimensions, compatibility with technology scaling, and relative long decoherence times.

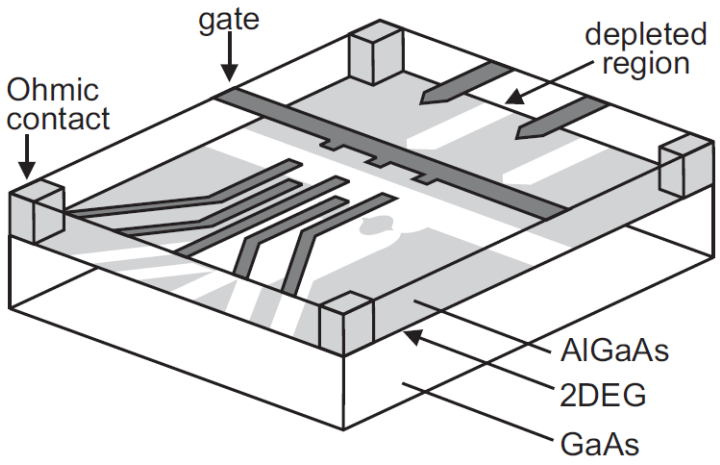


Figure 4.2: *Schematic view of a quantum device, reproduced from [133].*

As the name suggests, in spin qubits the information is stored in the spin of the electrons. The difficulty consists in the manipulation of a single electron for each single

qubit, by means of quantum dots. Fig.4.2 shows a possible physical implementation of a qubit, where the substrate is GaAs and on top there is a deposition of AlGaAs, in order to obtain a 2D electron gas at the interface of the two materials. GaAs is not the only substrate available: several works of spin qubits realized in silicon have been presented ([137–139]), opening the way to a full integration of qubits and classical electronic. Manipulating the voltages on the electrodes shown in Fig.4.2, a deplete region small enough to trap a single electron can be formed. Controlling the other electrodes, the spin of the electron can be manipulated or read out. Due to the limited dimensions of the quantum dot, the energy levels allowed for the electron are quantized. In the lowest energy level only two electrons can be present, with opposite spin. Applying a strong magnetic field, due to the Zeeman effect, it is possible to obtain two sub-levels with a single electron each, with opposite spin. As can be easily foreseen, the energies in play are really low, so that the thermal energy must be lower than the Zeeman splitting ΔE, in order to avoid unwanted jumps of the electron to other energy levels. This is the reason of the very low temperatures needed for the quantum computer (usually on the order of hundreds of mK).

In order to read the spin of the qubit, a conversion from spin to charge is developed. Controlling the voltages of the electrodes around the quantum dot, it is possible to vary the tunnelling barrier from the dot to the reservoir, depending on the spin of the electron. The presence of the electron in the dot determines the conductivity of the channel next to the dot due to electrostatically coupling. The resistance of this kind of sensor, called Quantum Point Contact (QPC), is on the order of 25 kΩ, with a variation due to the spin of the electron in the quantum dot on the order of 1%. A more sensitive charge sensor is the Single-Electron Transistor (SET), whose resistivity variations is on the order of 10%. Two different approaches for reading the state of the qubit by means of QPC or SET will be discussed in paragraph 4.4.

4.3 Electronic controller and readout

The actual state-of-the-art quantum processors are the "Bristlecone", a 72-qubit quantum chip by Google, and "Tangle Lake", a 49-qubit superconducting test chip by Intel. Other multinational corporations leaders in the technology field, as IBM or Microsoft, are investing considerable amounts of money on the research on quantum computing. Even if the goal of a quantum processor with million of physical qubits is far from the reality, huge steps have already been made.

All these qubits must be served by a classical electronic controller, in order to feed them with high frequency electrical signals to realize useful operations on them, and acquire the electrical signals for reading their logical states. In the actual measurement setups (Fig.4.3), the electronic interface is placed at RT, and wired directly to the qubits in the coldest stage of the dilution fridge. In an intermediate stage, around 4 K, only few electronic blocks are placed, such as the Low Noise Amplifier (LNA) for a first preamplification of the acquired signal, and an attenuator of the control signals, as the one shown in Fig.4.7. This solution is still feasible for interfacing a few number of qubits. With the scaling up of the computational power a change in the electronic controller will become necessary. The large number of connections from the mK stage to RT, in fact, will become a problem for the scalability of an useful quantum computer,

considering the presence of thousands or millions of cables carrying GHz signals for several meters, increasing not only the space occupation but also the thermal load.

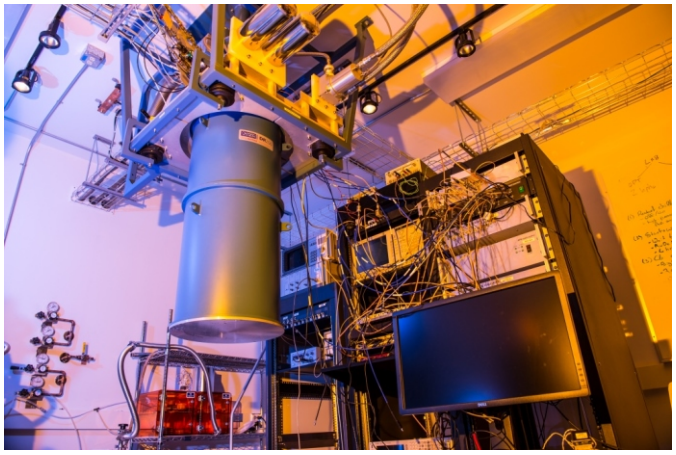


Figure 4.3: *Dilution fridge at Raytheon BBN Technologies in Cambridge, Massachussets. Picture taken from: https://www.raytheon.com/news/feature/quantum_computer*

An alternative solution presented in [127, 140] suggests the implementation of a cryogenic controller, placed in the dilution refrigerator as close as possible to the real quantum processor, as depicted in the block diagram of Fig.4.4. The best compromise between the lowest temperature for electronics and the highest cooling power available is given by the liquid helium temperature stage (4.2 K). This stage in the dilution fridge is close enough to the real quantum computer and allows around 1 W of cooling power. Several technologies have been tested at such low temperatures. Among them, CMOS technology is one of the most promising, considering the development and the maturity of the process, already diffused for industrial and military temperature range (down to -55 °C) and tested experimentally to work at 30 mK [141]. Difference in the behaviour of MOSFET devices, compared to RT, has been measured, as reported in [142–144]. Furthermore, relevant differences between the different processes, especially between long channel and short channel processes, have increased the interest on the characterization of cryogenic CMOS processes. The efforts to realize a complete modeling procedure for those CMOS processes candidates for cryogenic temperature is becoming mandatory, even if still few examples are present in the literature, such as [143–145]. A better insight of cryogenic behaviour of standard CMOS processes will be given in the next paragraph; for an extensive analysis of the topic, the reader is invited to consult the cited works.

The proposed solution of integrating the electronic controller at the 4 K stage would provide great benefits in terms of signal fidelity, scalability and thermal load reduction. Furthermore, [139] explores the possibility to increase the operating temperature of silicon qubit from tens of mK to 1.5 K, very close to the stage of electronic controller, with a view on the implementation of the qubits and the electronic at the same stage (possibly on the same substrate), in order to reduce the connections from the different stages in the dilution fridge and room temperature as much as possible.

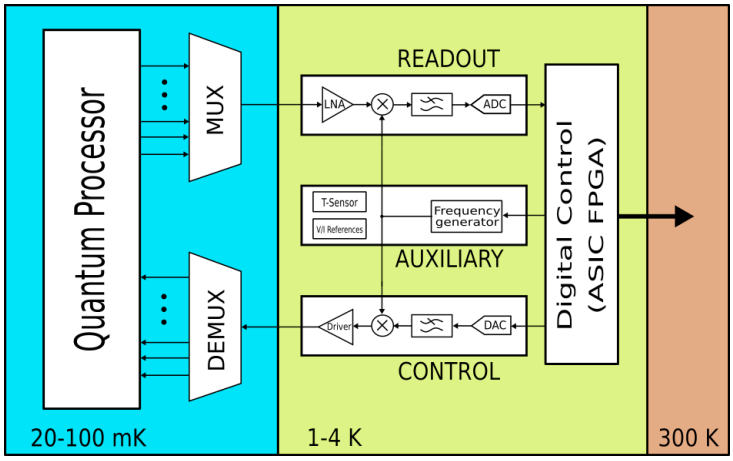


Figure 4.4: *Block diagram of the Cryo-CMOS controller presented in [140]*

4.3.1 Cryogenic CMOS

As explained in the previous section, the necessity of designing the classical controller and readout compatible with temperatures very close to the quantum computer, has pushed the research to find a process suitable for such extreme conditions. The standard CMOS process has been revealed as one of the most interesting candidate, due to its low cost and high maturity. However, CMOS processes are usually characterized until -55 °C for military application. As a result, the models provided by the foundry are not available for cryogenic temperatures, and the changing of the physical behaviour of the devices is not fully understood so far. Cryogenic CMOS is also source of interests for many other applications, such as electronics for space applications, physics experiments and medical imaging systems, just to cite the most important ones. A brief overview of the most noticeable effects of cryogenic temperatures to standard CMOS process is provided, taking [146] as a reference for the measurements.

It is well known the increase of mobility due to less phonon scattering at very low temperatures. Other scattering mechanisms like surface scattering and ionized impurity scattering, instead, increase at lower temperatures due to the lower kinetic energy of the electrons. Low temperatures leads also to an increase of the electrical field values which generate velocity saturation. The final result is an increase of mobility of nearly two times compared to room temperature.

In older CMOS processes, a kink of MOSFET drain current for high drain-source voltages has been measured [147]. However, this effect, particularly detrimental for analog design, caused by impact ionization and freeze-out effects, is not present in thin-oxide processes and small channel devices (e.g. in 40 nm devices, as it looks evident from measurements shown in Fig.4.5).

Another well known effect is the threshold voltage increase of MOSFET devices at low temperatures. This means that a higher gate voltage is needed in order to form the inversion layer and start the conduction in the channel, as depicted in Fig. 4.6. The increase is on the order of $100 \div 150$ mV, affecting heavily the design of analog blocks due to the reduced voltage headroom, considering the typical supply of 1.1 V or lower of modern CMOS processes (e.g.: 1.1 V for 40 nm technology, 0.7 V for 10 nm technology).

Another important effect is the increasing of the subthreshold slope. The subthreshold slope is defined as the slope of the drain current expressed as a function of the gate-source voltage in a logarithmic scale. It coincides with the expression of the equivalent thermal voltage for a MOSFET in subthreshold (see paragraph 3.2). Being directly proportional to the absolute temperature, a decreasing of almost a factor 100 from RT to 4 K would represent an increase of the same order of the subthreshold slope. Actually, the subthreshold slope increases sublinearly with temperature decreasing, due to the increase of the non-ideal factor n present in the equation of the drain current of a MOSFET in subthreshold region (equation 3.1).

Other effects that must be taken into account are the increase of the n-well resistance due to the freeze-out of the substrate and the linear dependence of the drain current to the gate-source voltage caused by the velocity saturation.

Concerning the noise, thermal noise reduces at lower temperature, but it does not go to zero as expected. It is limited by the shot noise of the transistor [148], especially in small channel lenghth devices, while a definitive theory is not present about flicker noise. [149] shows a decreasing of flicker noise measured down to 87 K, but further investigations needed to be made for a better understanding. Concerning device mismatch, it has been measured an increase of the mismatch at cryogenic temperatures, even if the reasons are not completely understood so far [150].

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4.4 Qubit readout

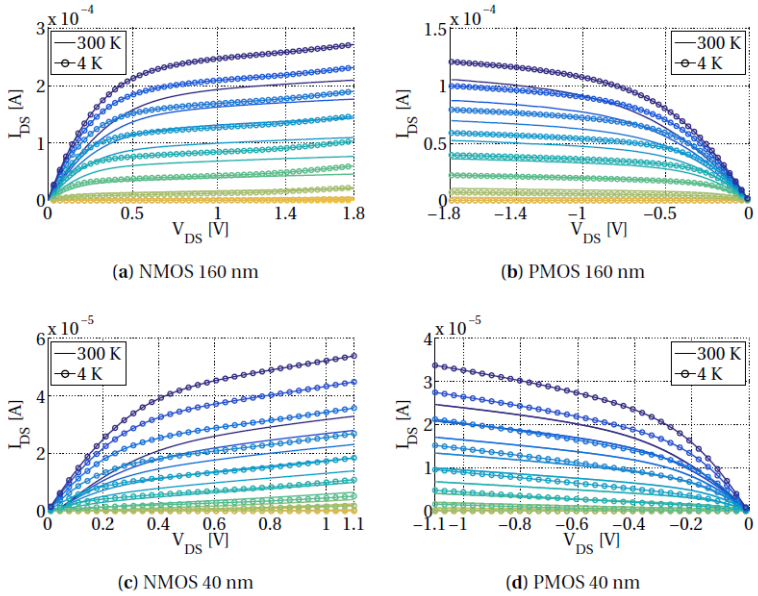
The readout of spin qubits is basically related to the measurement of the electrical resistance of the SET or QPC. Then, two different approach can be exploited: dc measurement or RF reflectometry. Both techniques are here described, highlighting the advantages, the drawbacks and the practical considerations that leaded us towards the reflectometry readout.

4.4.1 Baseband readout

The dc or baseband readout consists in the direct reading of the value of the resistors of the SET. Using a TransImpedance Amplifier (TIA), it is possible to detect the value of the resistor and then the logical state of the qubit. Unfortunately, the parasitic capacitance of the transmission line limits the frequency response of the transimpedance amplifier. Furthermore, a high-pass filter is usually added at the input to filter out noise coupling from the amplifier to the SET. This solution is limited by the flicker noise of the amplifier and by the parasitic capacitance of the line going from 20 mK to 4 K. This issue forbids the possibility to use frequency division multiplexing access (FDMA). An alternative solution could be time division multiplexing access (TDMA), if the switches were implemented close to the qubits at the lowest temperature stage; the efficiency of the compression, in that case, grows exponentially with the number of control bits for the multiplexer.

4.4.2 RF Reflectometry

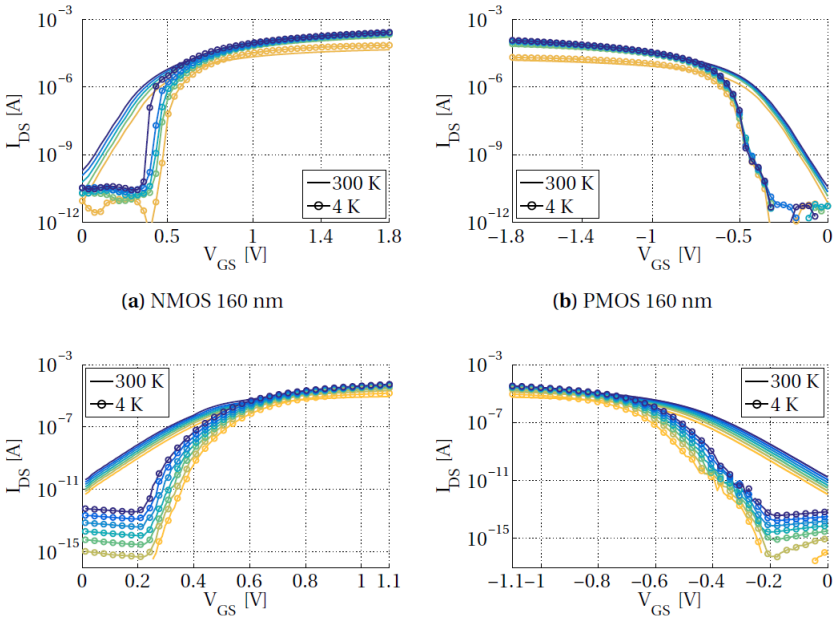
The other possible readout, that is the one taken under analysis in this chapter, it is the RF reflectometry. The SET is matched to 50 Ω through a LC matching network



(a) NMOS 160 nm (b) PMOS 160 nm

(c) NMOS 40 nm (d) PMOS 40 nm

Figure 4.5: *I_{DS} vs V_{DS} for NMOS and PMOS devices in 160 nm and 40 nm technologies. Graphs taken from [146]*



(a) NMOS 160 nm (b) PMOS 160 nm

(c) NMOS 40 nm (d) PMOS 40 nm

Figure 4.6: *I_{DS} vs V_{GS} for NMOS and PMOS devices in 160 nm and 40 nm technologies. Graphs taken from [146]*

at the mK stage, as shown in Fig. 4.7. A directional coupler at the 4 K stage is used to provide the stimulus to the SET and to bring the reflected wave to the LNA. The matching network, made up of the parasitic capacitance C_P of the SET (mainly due to the pad, on the order of hundreds of fF) and the inductor L, matches the nominal resistance of 25 kΩ. The value of the inductor is on the order of 0.9-1 µH, that is one of the limit of this approach, especially considering the FDMA, where multiple inductors

of the same order of magnitude are required. Depending on the spin of the electron, the

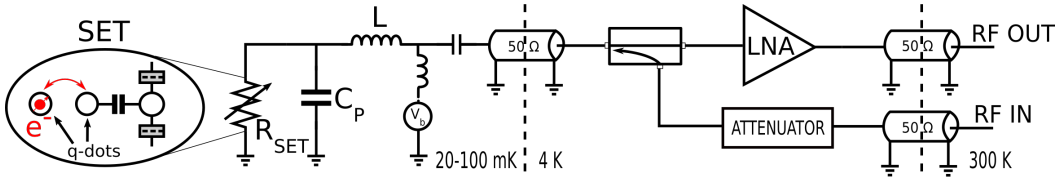


Figure 4.7: *Block diagram of RF reflectometry readout for SET.*

electron may tunnel through the dot, generating a temporary variation of the channel resistance of the SET, that can be detected as a variation of the reflection coefficient of the matching network. In order to read the information, an incident waveform at the resonance frequency of the matching network is applied. Depending on the value of the electron spin, no reflected wave or a reflected wave with an amplitude proportional to the variation of the reflection coefficient will be present. The maximum power that can be applied to the SET P_{max} is on the order of -99 dBm, limited by the possible harmful interactions with the neighbouring qubits. The quality factor of the matching network is:

$$Q = \sqrt{\frac{R_{SET}}{R_S} - 1} = 22.3 \tag{4.1}$$

considering the nominal value for R_{SET} of 25 kΩ and the line resistance R_S of 50 Ω. With a parasitic capacitance of 730 fF, the value of the inductor needed to match the SET resistance is 910 nH, obtaining a resonance frequency of around 195 MHz, while the bandwidth of the resonator is 8.5 MHz. The reflection coefficient at the resonance frequency is:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{\frac{L}{R_{QPC}C} - R_S}{\frac{L}{R_{QPC}C} + Z_0} = \frac{L - R_{QPC}R_SC}{L + R_{QPC}R_SC} \tag{4.2}$$

Considering a 10% variation of the SET resistance due to the electron tunnelling from the quantum dot, the variation of the reflection coefficient is around 5%. Than, the amplitude of the reflected waveform at the input of the LNA at the 4 K stage is:

$$V_{reflected} = \frac{\sqrt{P_{max}2R_{SET}}\Gamma}{Q} \approx 180\,nV \tag{4.3}$$

The shot noise of the SET at the input of the LNA has an equivalent noise temperature of 0.5 K. This leads to a SNR, considering only the noise contribution of the SET source, of 6.5 dB on a bandwidth of 10 MHz.

4.5 Design of Cryo-CMOS ADC

The reflectometry RF interface can be analysed from a system-level point of view, as a receiver of On-Off Key (OOK) modulated signals. Due to the value of the electron spin, and consequently the value of the resistance of the SET, the reflected signal will have a zero amplitude, or the one evaluated in 4.3. This signal will be the input of a LNA, and

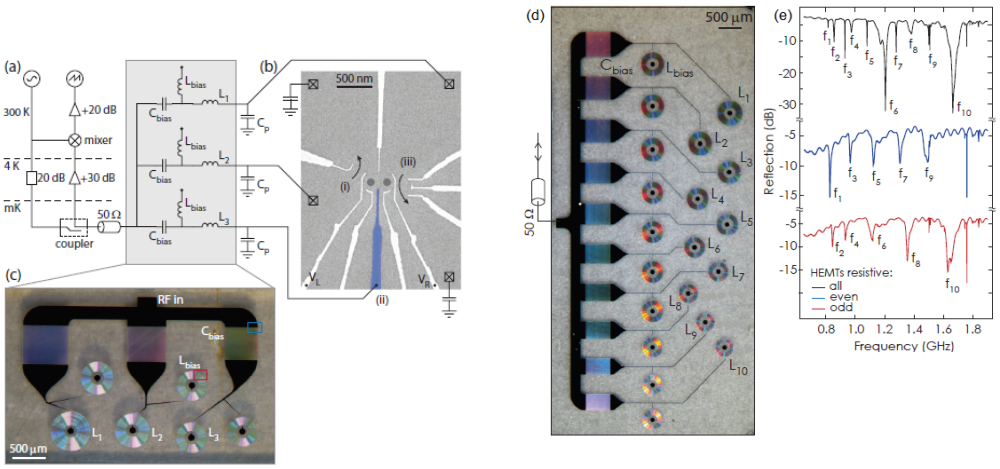


Figure 4.8: *FDMA in RF reflectometry readout shown in [151]. (a) Block diagram of the FDMA readout. (b) GaAs double dot device. (c) Optical micrograph of the multiplexing chip. (d) Optical micrograph of a 10:1 MUX chip. (e) Frequency response of MUX chip in (d).*

after a proper amplification, it will be converted by an ADC. Through Matlab-Simulink simulations, it is possible to evaluate the performances of this "receiver" in terms of BER after an ideal decision-maker, as a function of the several parameters (source noise, LNA gain and noise, ADC resolution and linearity, etc.). The performances of the system are already limited by the signal-to-noise ratio of the source, i.e. of the SET sensor. Great steps have been made by the physicists in the last two decades, and many other steps are yet to come, in order to improve the performances of the sensor close to the qubit. The LNA will be then the most critical block of the electronic interface, as stated by the Friis formulas. The ADC is not the bottle-neck of this acquisition system, but some specifications can be drawn from the high-level descriptions. Targeting the FDMA readout of 20 qubits, a SINAD of 60 dB and a sampling frequency of 1 GHz would be enough to reach a BER of 1e-3, that is the fault tolerance error threshold for one cycle of QEC. Considerations about the power consumption are heavily affected by the process involved. If CMOS is used for the LNA, the power consumption divided by the number of qubits read in parallel with FDMA is around 1 mW/qubit. This means that the cooling power of the actual dilution refrigerator (1 W of cooling power for the stage at 4 K) would guarantee a maximum number of 1000 qubits. This would be already an optimum result considering the actual state-of-art, but still far from the goal of millions of qubits needed for an useful quantum computer. Silicon-Germanium LNAs, on the contrary, show a power efficiency of 10 µW per qubit, and they are really promising candidates.

In order to have a power budget for the ADC negligible in the case of CMOS LNA, or comparable with the power budget of a SiGe LNA, a target power consumption of 40 µW/qubit is desirable. This leads to a total power consumption of the ADC of 800 µW. It is quite easy to evaluate the Walden figure-of-merit that we are targeting:

$$FoM_W = \frac{P_D}{2^{ENOB}\, f_{Nyq}} = \frac{800\ \mu W}{2^6 \cdot 1\ GHz} = 12.5\ fJ/conv \tag{4.4}$$

This is already a challenging specification, considering the high sampling frequency

and looking at the state-of-the-art for ADCs working at RT (Fig.1.19). Furthermore, the ADC should work properly at 4 K. This complicates the design of the ADC, considering also the lack of proper device models for the simulations at such low temperatures.

Looking one more time to Fig.1.19, it looks evident how the main candidate to achieve the target resolution and sampling frequency with low power consumption is the Successive Approximation Register (SAR) ADC [152]. Another possible solution is a Time-Interleaving SAR, which requires anyway the optimization of a single SAR slice. In the last years, SAR and TI SAR are leading the trends of high-speed converters, due to the introduction of new techniques as asynchronous timing [153, 154], 2 bit-per-stage SAR [155, 156], alternate comparators [157] and loop-unrolled topologies [156, 158].

In order to have more flexibility, we focused on the design of a SAR ADC capable of reach an higher resolution than the one strictly required by the RF reflectometry readout, exploiting the time-interleaving principle to increase the sampling frequency. Thanks to the addition of programmability inside the ADC, it is possible to configure the resolution from 6 to 9 bits, with a maximum sampling frequency that goes respectively from 1 GHz to 600 MHz.

4.5.1 SAR

The SAR seems a promising candidate for working at cryogenic temperatures for different reasons. First af all, the main bulding blocks of this kind of converter are: comparators, logic gates, switches and capacitors. All these devices benefit from the technology scaling; the same does not happen for most of the analog circuits. No linear circuit such as residual amplifier are employed, differently, for example, from pipeline converters. Most of the operations in the SAR are effectuated after the comparator decision, i.e. in the digital domain. This looks very appealing, also considering the problems of designing for cryogenic temperatures without proper device models available. We know that the increasing of the threshold voltage and the mobility of the transistors are the most dominant effects. This means that the time to turn on a transistor will increase, but it will have more driving capability and it will be faster in charging and discharging capacitors.

Using a dynamic comparator, standard CMOS logic and a Capacitive DAC (CDAC), no static current consumption is dissipated. SAR represents a very high efficient solution for medium resolution data converter. In order to increase the sampling frequency, time-interleaving solution can be adopted, where the single slice is a SAR. In the next subsections, each building block of the SAR will be analysed, discussing each choice and focusing mainly on the specific strategies adopted for the cryogenic application. The design and implementation of the necessary auxiliary blocks for the proper working of the ADC, such as the clock receiver, the digital interface and the SRAM for the storing of the converted data, will not be discussed in this work.

4.5.2 Comparator

The conventional SAR architecture requires one dynamic comparator. In the literature there are several possible different topologies of comparators [159, 160]. All of them have in common, at least partially, the typical latch structure, in order to provide a

positive feedback which guarantees the regeneration of the output levels to the full CMOS levels. One of the most popoular dynamic amplifier is the so called Strong-ARM comparator [161], presented the first time in 1993 as a latch sense amplifier. The behaviour of this circuit has been studied deeply in [162–164], due to its important in several applications, from memories (as a sense amplifier) to ADCs. In Fig.4.9, the version proposed in [165] is depicted.

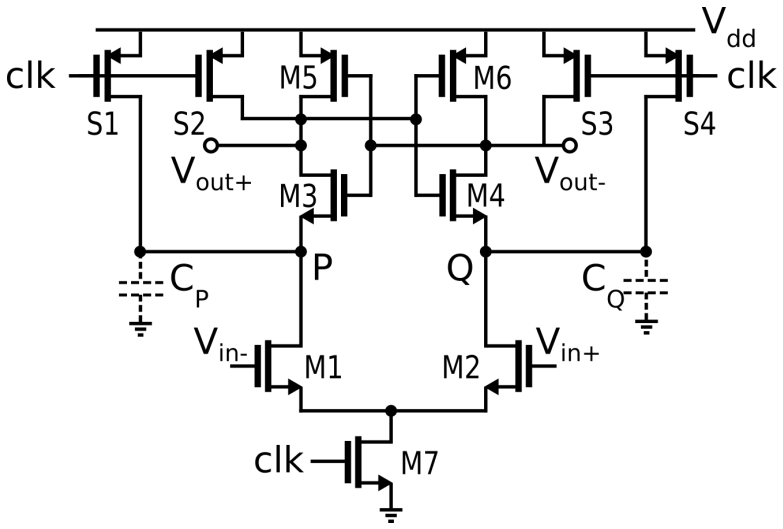


Figure 4.9: *Schematic view of the Strong-ARM comparator with nMOS input differential pair.*

The input differential pair M1-M2 provides a differential current proportional to the input differential signal into the latch composed by M3-6 (cross-coupled inverter configuration). Current is supplied through transistor M7, which is driven by the clock signal that controls the comparison and the reset phases. When the clock signal is low, no current is drawn from M7, and both the couples of nodes P,Q and V_{out}^{+}, V_{out}^{-} are shorted to the supply rail through the reset switches S1-4. When the clock signal goes high, current starts flowing in the circuit through the input differential pair. Depending on the input differential signal, the parasitic capacitances $C_{P,Q}$ start to be discharged with a different rate, leading to a differential voltage on the respective nodes P,Q. When the voltages at nodes P,Q go lower than V_{dd} of a threshold voltage, M3-M4 turn on and the regenerative behaviour starts. In a similar way, V_{out}^{+} and V_{out}^{-} are discharged by M3-M4 until they fall below V_{dd} of a threshold voltage. Then the whole latch made up of M3-M6 is on and depending on the sign of the input differential voltage, the decision is taken, leading one of the output to a rail and the other output to the opposite rail. At the end of the decision phase, no static current is flowing in the circuit, because either the PMOS or the NMOS of the two branches of the latch is off.

The absence of static current consumption, together with the current recycle for the dynamic preamplifier (made up of M1-2, $C_{P,Q}$) and the dynamic latch, made the strongARM comparator a very promising candidate for low-power SAR. Furthermore, the gain provided by the intrinsic dynamic preamplifier allows us to get rid of an additional preamplifier. A preamplifier would be beneficial to reduce the referred-to-input thermal noise, offset and differential kickback present in the dynamic comparator, but at the cost of very high power consumption, considering the targeted high speed. The

dynamic amplifier implemented by M1 and M2 provides a voltage gain A_V from the input to the nodes P,Q, integrating a differential current proportional to the differential input voltage on $C_{P,Q}$ for a time t_{amp}. t_{amp} is the duration of the amplification phase, and it lasts from the rising edge of the clock signal until the common mode current of M1-2 discharges P,Q, turning on M3-M4.

$$A_V = \frac{\Delta V_{P,Q}}{\Delta V_{in}} = -\frac{g_{m1,2}}{C_{P,Q}} t_{amp} \tag{4.5}$$

$$t_{amp} = V_{th3,4} \frac{C_{P,Q}}{I_{CM}} = V_{th3,4} \frac{C_{P,Q}}{g_{m1,2} V_{TE1,2}} \tag{4.6}$$

where I_{CM} is the common mode current flowing in M1 and M2. Replacing (4.6) in (4.5) and considering the input pair working in strong inversion, the expression of the voltage amplification provided by the input pair is:

$$A_V = \frac{V_{th3,4}}{V_{CM} - V_{th1,2}} \tag{4.7}$$

After the amplification phase, M3-4 turn on and start discharging the load capacitances C_L present on the output nodes $V_{out}^{+,-}$. The output nodes are discharged with an exponential behaviour. Depending on the value of C_L and $C_{P,Q}$, this phase may already provide some regeneration [162, 164]. When the output voltages $V_{out}^{+,-}$ reach $V_{dd} - |V_{th5,6}|$, the regeneration phase takes place, leading one of the output to V_{dd} and the other one to ground, with a positive exponential behaviour (with time constant proportional to the latch transconductance).

From (4.7) it is already possible to foresee some of the critical aspects concerning the comparator design. Indeed, the voltage gain A_V affects the circuit performances: the higher is A_V, the smaller is the effect of the dynamic latch in terms of offset and noise. The value of A_V is on the order of few units to ten, depending on the input common mode voltage. Actually, this is a pivotal issue of this kind of comparator. The input common mode affects heavily the speed and noise/offset performances. An higher input common mode implies an higher common mode current and then a faster discharge of the nodes P,Q, leading to a smaller t_{amp} and then a faster decision. But a smaller t_{amp} also implies a smaller A_V, and then an increase of offset and noise.

The offset of the comparator is usually dominated by the threshold and the β mismatch of the input differential pair, because of the contribute of M3-4 is divided by the voltage gain A_V provided during the amplification phase [164]:

$$v_{io} = \Delta V_{th1,2} + \frac{\Delta \beta_{1,2}}{\beta_{1,2}} \frac{V_{CM} - V_{th1,2}}{2} \tag{4.8}$$

Also a difference in $C_{P,Q}$ affects the offset of the comparator. This effect can be exploited to calibrate the offset of the input pair, adding properly an additional capacitance on node P or Q [162].

Considerations about the thermal noise are similar to the one made for the offset: most of the contribution comes from the input differential pair, considering a sufficient gain A_V.

$$\langle v_{n-th} \rangle^2 = \frac{2S_I t_{amp}}{C_{P,Q}^2} \frac{1}{A_V^2} = \frac{V_{CM} - V_{th1,2}}{V_{th3,4}} \frac{kT}{C_{P,Q}} \left[4\gamma + 2\frac{V_{CM} - V_{th1,2}}{V_{th3,4}} \right] \tag{4.9}$$

where S_I is the power spectral density of the drain current noise of M1,M2. γ is the excess of noise of a MOSFET in saturation region compared to the noise of a resistance with value $1/G_m$.

A trade-off between the speed and the RTI noise of the comparator is clear from eqs. (4.6) and (4.9), and an optimum value of the input common mode can be found. In Fig.4.10, the behaviour of the rms noise and the comparator delay (with a differential input voltage of 1 mV and a supply voltage of 1.1 V) for different input common modes of a StrongARM comparator with NMOS input pair is shown. RTI offset of the comparator has a behaviour similar to RTI noise with the variations of the input common-mode, as depicted in Fig.4.11. This offset variation may lead to converter non-linearities, if the input common-mode is not kept constant during the different bit-cycles of the SAR. CDAC switching scheme as [166] are thought to keep the comparator input common mode constant during the whole conversion in order to avoid these harmonic distortions.

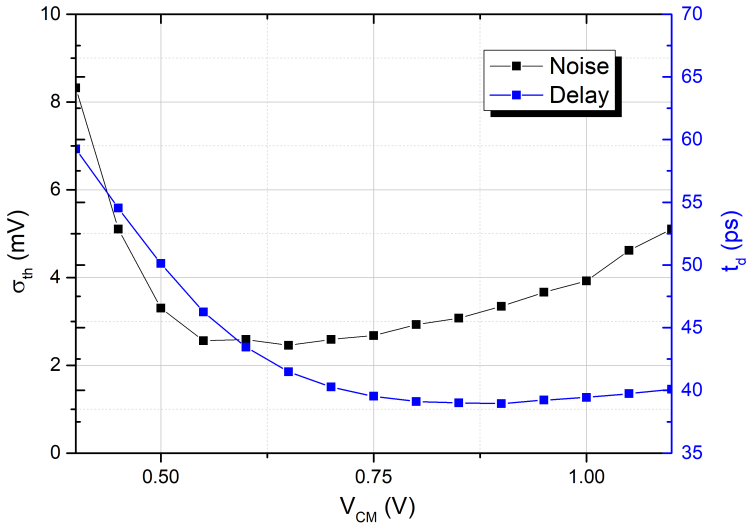


Figure 4.10: *Delay time and thermal noise standard deviation of StrongARM Comparator varying the input common mode, at 27 °C.*

Until now, no considerations about the modifications of comparator behaviour from RT to cryogenic temperatures are mentioned. Because of the absence of proper models of the adopted process at 4 K, simulations at -55 °C were performed. Fig.4.12 shows the differences in terms of comparator delay for a NMOS and a PMOS input pair comparator (sized with the same power consumption) at RT and -55 °C, performing a sweep of the input common mode. A part from the intrinsic slowness of the PMOS comparator compared to the NMOS comparator even at RT, an increasing of the comparator delay at 4 K for input common mode close to mid-rail is present. The variation of comparator performances has been one of the main concern of this design, due to its pivotal role in the SAR converter.

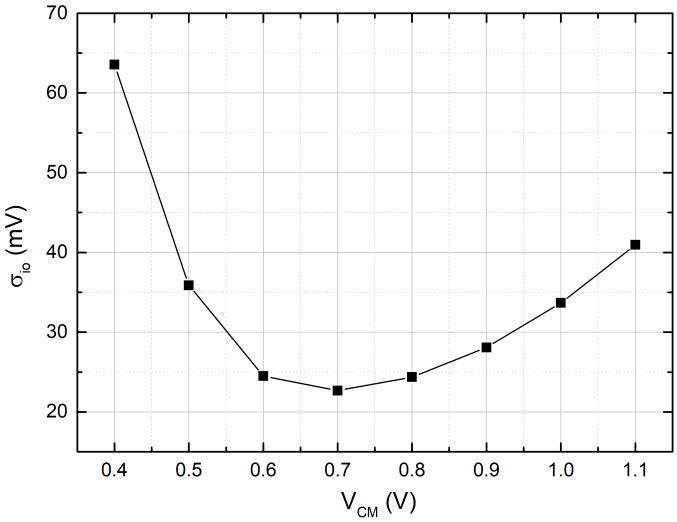


Figure 4.11: *Comparator offset varying the input common mode.*

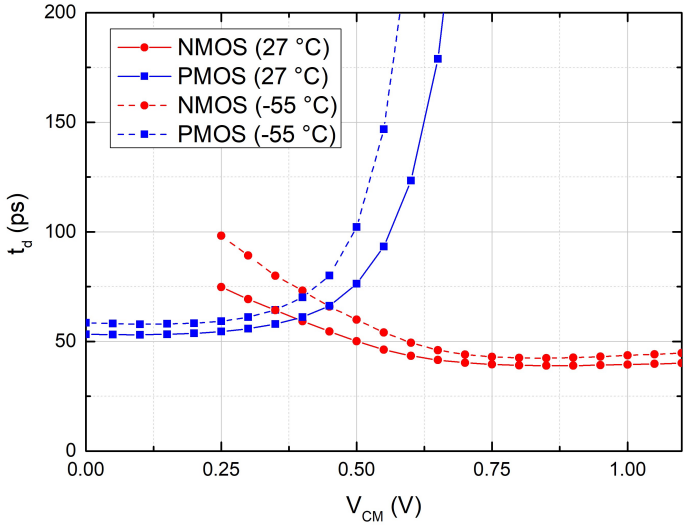


Figure 4.12: *Delay time of NMOS and PMOS input pair StrongARM Comparator varying the input common mode, at 27 °C and -55 °C.*

4.5.3 CDAC

The DAC is another key block of the SAR. As already explained, it is used to approximate the input signal that has to be converted. Any source of error injected in the DAC affects one-to-one the performances of the whole ADC. Then, a SAR converter with a resolution N must employs a DAC with the same resolution (and with similar requirements about noise and linearity). Among the different possible DACs, the typical implementation for a SAR is a capacitive DAC, which shows several advantages. First of all, it does not suffer of static current consumption, and this is particularly important for all the low-power applications where SAR converter leads the trends. Second, the capacitances implemented in the CDAC can be used also to implement the Sample&Hold circuit. From now on, only a fully-differential implementation will be

discussed, because of its several benefits in terms of disturb rejection and linearity.

About the sampling, two main techniques are usually implemented: the bottom plate sampling and the top plate sampling. In the bottom plate sampling, the input signal is sampled on the bottom plate of each capacitor of the DAC. This reduces the parasitic capacitance on the top plate of the CDAC, and reduces the effect of charge injection. The drawbacks are that it requires one switch for each capacitance (increasing the circuit complexity and the load for the driving buffers), and it requires an extra switch for the MSB decision. The top plate sampling uses the top plate of all the capacitors for sampling the input signal. It requires only one switch for the sampling, and it allows to save the first switching cycle, because the input signal is already present at the input of the comparator just after the opening of the sampling switch. However, the presence of the input switch on the top plate increases the parasitics, reducing the linearity and increasing the effect of charge injection. Considering the target requirements of resolution, speed and power consumption, top plate sampling has been implemented.

Concerning the noise of the CDAC, two main contributions can be recognized. The sampling noise is given by:

$$P_{n-samp} = \frac{2kT}{C_S} \tag{4.10}$$

where C_S is the sampling capacitance, that can be split up in two parts: C_{DAC}, that is the overall capacitance of the DAC, and C_h, that is the attenuation capacitance due to the parasitics present on the top plate (made up of the parasitic capacitances of the switch, of the routing and of the input MOSFETs of the comparator). The factor 2 comes from the differential implementation. The other noise source comes from the buffers driving the capacitors and it can be written in the form of KT/C noise too:

$$P_{n-DAC} = \frac{2kT}{C_S}\frac{C_{DAC}}{C_h} \tag{4.11}$$

The sampling noise is inversely proportional to the sampling capacitance, and then inversely proportional to C_{DAC}. The expression of the noise of the DAC is inversely proportional to the sampling capacitance but depends also on the ratio between C_{DAC} and C_S. If the parasitic capacitances are on the same order of the overall DAC capacitance (that is often the case in low power design), the noise from the DAC is the same as the sampling noise. Both noise sources are anyway not limiting in the choice of C_{DAC}. Considering for example a full-scale range of 1 V, an overall capacitance of 105 fF leads to a noise power equal to 10 bit quantization noise power. Furthermore, both sources of noise, deriving from thermal noise, are expected to decrease moving from RT to cryogenic temperatures.

Another consequence of the value of the DAC capacitance is the attenuation of the full-scale range given by the partition of C_{DAC} and sC_h. The attenuation of the full-scale range means an attenuation of the same order of the quantization step Δ. The attenuation worsens the requirements on the thermal noise power, especially the one coming from the comparators.

Concerning the linearity, a variation of the value of the DAC capacitors due to mismatch can introduce DNL errors. The most severe condition is given by the mid-code transition, since all the capacitors are switched in a binary-scaled DAC. The typical

requirement is of a maximum DNL lower than half LSB. A relative matching error between two nominally identical capacitors lower than 1.5 % would guarantee the linearity requirement for an 8 bit CDAC [167]. Lastly, the value of C_{DAC} and C_h also affects the linearity, considering the non-linear behaviour of C_h.

The dynamic power consumption of the CDAC depends on the switching algorithm chosen, but can be expressed with the general expression:

$$P_{n-DAC} = \alpha f_s C_{DAC} V_{dd} \tag{4.12}$$

where α depends on the switching algorithm and f_s is the sampling frequency. In order to reduce the dynamic power, a low value of C_{DAC} would be preferred. The minimum value of C_{DAC} can be obtained from the noise and linearity specifications above mentioned.

The layout chosen for the CDAC has been inspired by the one proposed by P.Harpe in [167] and shown in Fig.4.13. Custom-designed MOM capacitor using only two metal layers are used, in order to obtain very low values of the unit capacitor (around 500 aF). The values of the real unit capacitor and the parasitic capacitances are obtained by means of parasitic-extraction tools after layout. The advantage of this approach is the possibility to implement capacitor with every desired values of capacitance (limited, of course, by the minimum spacing of the metal layers, and by the amount of parasitic capacitances present), that is not typically possible with parametric MOM cells provided by the foundry. Moreover, this approach is totally scalable to other technologies and it takes advantage of technology scaling, due to the improvement in photolithography and shrinking of the minimum pith between different metal traces. Fig.4.14-b shows the final layout of the implemented 9 bit CDAC. For the last bit, a capacitor equal to two times the unit capacitor, that will be driven by a voltage reference equal to a quarter of the nominal V_{ref} is used. The reason of this choice is mainly motivated by low risk design considerations. For the target application, already a resolution of 6 bit would be sufficient. In order to explore further the design space, a maximal resolution of 8 bit looked appealing in term of optimization of power, speed and comparator noise. Actually, a comparator sizing in order to have a thermal noise power equal to the double of the quantization noise power for 8 bit of nominal resolution has been targeted. However, in order to exploit (and also to explore) the decreasing of thermal noise at cryogenic temperatures, we have been motivated to increase further the maximal resolution to 9 bit. However, the value of the unit cap of 500 aF has been preserved for linearity issues, deciding to implement the additional bit without reducing further the unit cap. The possible solution, then, is to keep the same unit cap and half the reference voltage. An additional $V_{ref2} = V_{ref}/2$ would not be a good choice in terms of DAC settling time. In fact, considering a $V_{ref} = V_{dd}$, an intermediate V_{ref} would be detrimental for the r_{on} resistance shown both by PMOS and NMOS used for charging the capacitor. Eventually, we opted for a reference voltage $V_{ref2} = V_{ref}/4$, that would be sufficiently low to guarantee a correct driving by means of only NMOS switches. Requirements on V_{ref} and V_{ref2} matching are not particularly critical, considering that V_{ref2} is used only for the least significant bit. A simple resistive divider would be sufficient to provide V_{ref2} from V_{ref}.

The criteria to choose the switching algorithm among the tens present in the literature are: sampling typology, value of MSB capacitor, dynamic power consump-

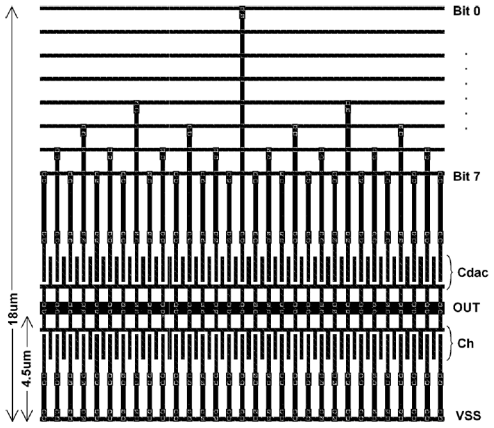


Figure 4.13: *Layout of CDAC proposed in [167].*

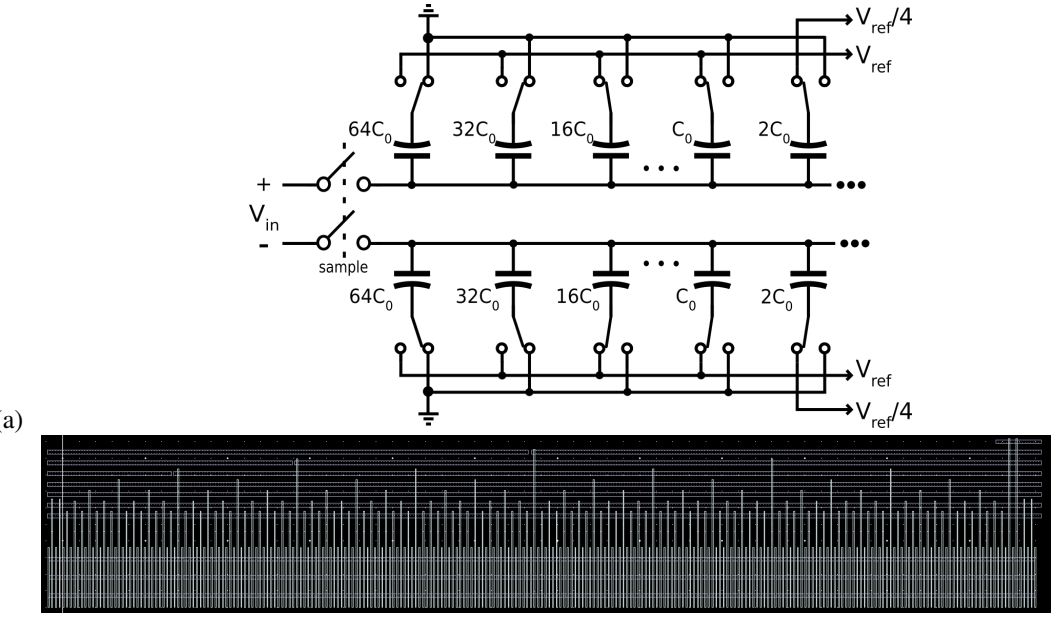


Figure 4.14: *9 bits CDAC: a) schematic view, b) layout.*

tion, complexity and effect on DAC common mode voltage. Some of the most popular switching algorithm are described in [87, 166, 168, 169].

The monotonic algorithm, also called "set and down" [87], is one of the simplest switching algorithm. It is allowed only in fully-differential CDAC implementation and it requires a MSB capacitor equal to $2^{N-2}C_0$, where N is the number of bit and C_0 is the unit capacitor. It does not require additional reference voltages as in many other algorithms [166]. During the sampling phase, all the capacitors are charged to V_{ref}, and then during the SAR operations, depending on the comparator decisions, for each branch only a capacitor on one side is discharged to ground. This means that the settling of the CDAC is characterized only by discharging through NMOS switches, that are faster than the PMOS ones. The charge to V_{ref}, through PMOS switches, takes place

during the reset phase at the end of the conversion, and it does not require fast settling.

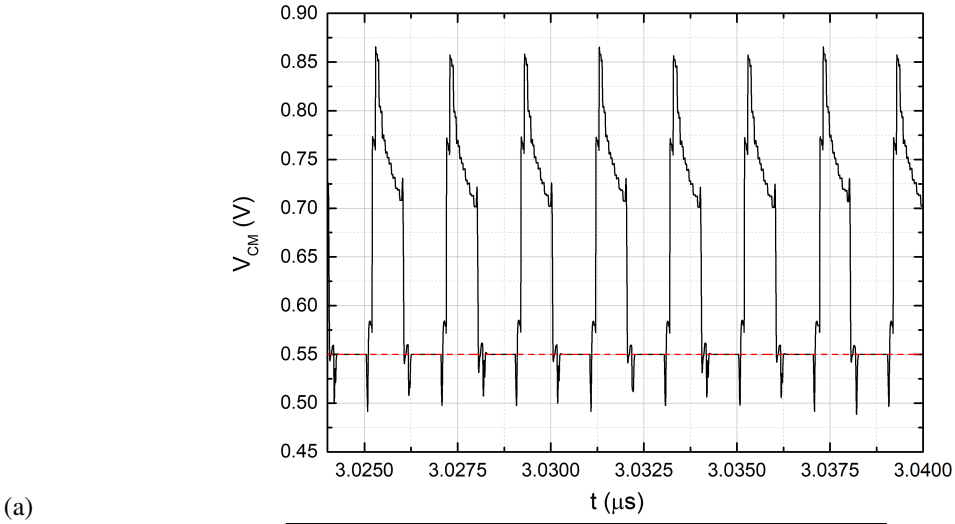
Two main problems are related to this algorithm. The DAC common mode voltage, starting from the input signal common mode, can only decrease of a quantity equal to $V_{ref}(\frac{1}{2} - 2^{-N})$. This also implies that only dynamic comparator with PMOS differential input pair can be used. As discussed in paragraph 4.3.1, at cryogenic temperatures MOSFET devices show an increase of their threshold voltage. At 4 K, for this process, an increasing of around 100 mV for the NMOS devices and 150 mV for the PMOS devices have been measured. This limits heavily the performances of the comparator, especially considering that for the first decisions it should work with an input common mode close to half of the V_{ref} (i.e. 0.55 V in our project), where the input differential pair is very close to the subthreshold region. Considering the smaller delay of the NMOS comparator and the smaller increasing of threshold voltage at 4 K, the NMOS comparator sounds more efficient and more reliable for cryogenic operations. This choice forces a modification of the switching algorithm respect to the "set-and-down" one. Keeping in mind the low complexity of the monotonic algorithm, a slight modification is necessarily required. Instead of pre-charging all the capacitors to V_{ref} and then executing only the discharging to ground during the conversion, the two largest capacitors of each side of the CDAC are connected to ground. For the two most significant bits, then, the algorithm is inverted, implementing a "set-and-up". During the first 2 decisions, the capacitors of one side are charged to V_{ref} through PMOS switches. This leads to an increase of power consumption respect to the classical algorithm, but it allows the use of a NMOS comparator.

Instead of keeping the "set-and-up" algorithm for all the bit cycles, a change of algorithm is performed, switching to the "set-and-down" for the remaining bits. Keep increasing the input common mode is not an efficient solution, as shown in figs. 4.10 and 4.11. Comparator thermal noise and offset, in fact, continue increasing while the delay time does not benefit sufficiently. Furthermore, the charging of the capacitor would still use PMOS switches, with lower efficiency. A change of algorithm after the first two bits from "set-and-up" to the conventional "set-and-down" is chosen, improving the efficiency in the DAC settling and the performances of the comparator in terms of speed-power trade-off. The behaviour of the comparator input common mode and differential mode are shown in Fig.4.15 during the normal operations of the converter.

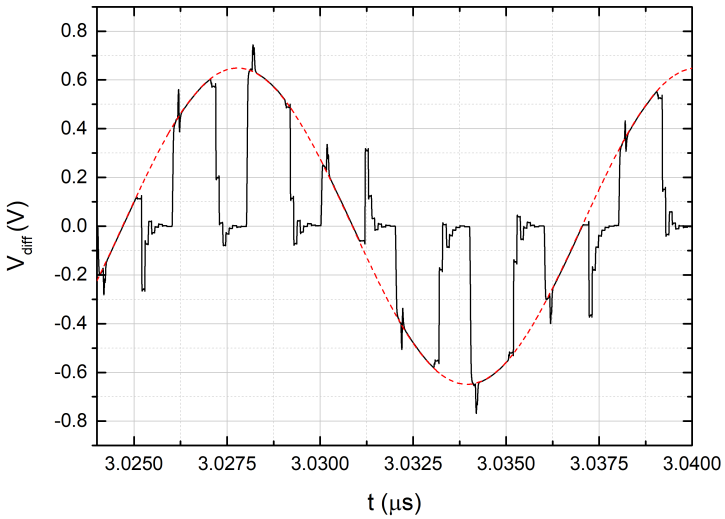
It is well known how a variation of the comparator input common mode leads to a variation of the comparator offset during the different bit cycles, i.e. to a converter distortion. On the contrary, a constant input common mode would guarantee a constant offset, that it reflects as a converter offset and then easily calibrated off-line. We decided to avoid a switching algorithm capable of providing a constant input common mode, because of the chosen SAR topology, that it will be described later. In the chosen topology, N different comparators are implemented for the N different comparisons. Thus, intrinsically they will have different offsets, regardless of the switching algorithm used. A calibration procedure in order to get rid of the comparators' offset will be implemented, allowing also the introduction of the proposed switching algorithm.

4.5.4 Asynchronous logic

One important choice in the design of a SAR converter regards the timing of the comparator operations. The main classification is between synchronous and asynchronous



(a)



(b)

Figure 4.15: *a) DAC common mode variation during different conversion cycles: the first 2 bits follow the "set-and-up" algorithm, the leftovers the "set-and-down". The dashed red curve is the input signal common mode. b) DAC differential mode variation during different conversion cycles. It is possible to recognise the sampling phase, where the DAC differential signal is equal to the input differential signal (red dashed curve); during the conversion, it converges to zero, following the typical binary approximation algorithm of a SAR.*

timing. Synchronous SAR employs a clock signal that is derived from the sampling signal, with a frequency that is a fraction of the main clock signal one. The clock frequency is equal to the sampling frequency divided by the number of bit of the converter resolution. For each bit, the dynamic comparator must be triggered and then reset after it has taken the decision. The clock period must be long enough to guarantee the proper decision of the comparator, the storage of the result in a latch and then the reset of the comparator. If the comparator is proper designed, only one of the decision in the whole conversion is critical and can induce metastability. Metastability occurs when the input signal of the comparator is so small that the output of the comparators has

not reached the full CMOS levels. Consequently, the CDAC could be not driven properly and an error in the output code will be present. The type of switching algorithm also contributes to the metastability and can mitigate this kind of code errors. Another solution to reduce the probability of metastability consists in spending more time for each bit-cycle, so that the comparator can take the correct decision even for smaller inputs during the single critical cycle. In synchronous SAR, this solution may mitigate metastability issue with severe penalties of speed performance. In fact, to reduce the metastability of one possible critical decision in each conversion period, every bit cycle must be enlarged.

A clever solution is represented by the asynchronous SAR. Presented for the first time in [153], the asynchronous SAR does not need an external clock for the comparator operations. After each comparator decision, a digital block detects it and generates the clock signal to reset the comparator and than trigger it for the next bit cycle. In this way, each bit cycle can have a different time period, depending on the input amplitude and the relative criticality. The only condition that must be guaranteed is that during a conversion cycle, all the decisions take place (depending on the requirements on the converter BER).

The main differences between the two timings are depicted in Fig.4.16. In asynchronous SAR, in order to reduce the possibility of metastability, only one bt cycle has to be longer, instead of all bit cycles as in synchronous SAR, increasing significantly the speed performances. The complete analysis on metastability in synchronous and asynchronous SAR can be found in [170, 171].

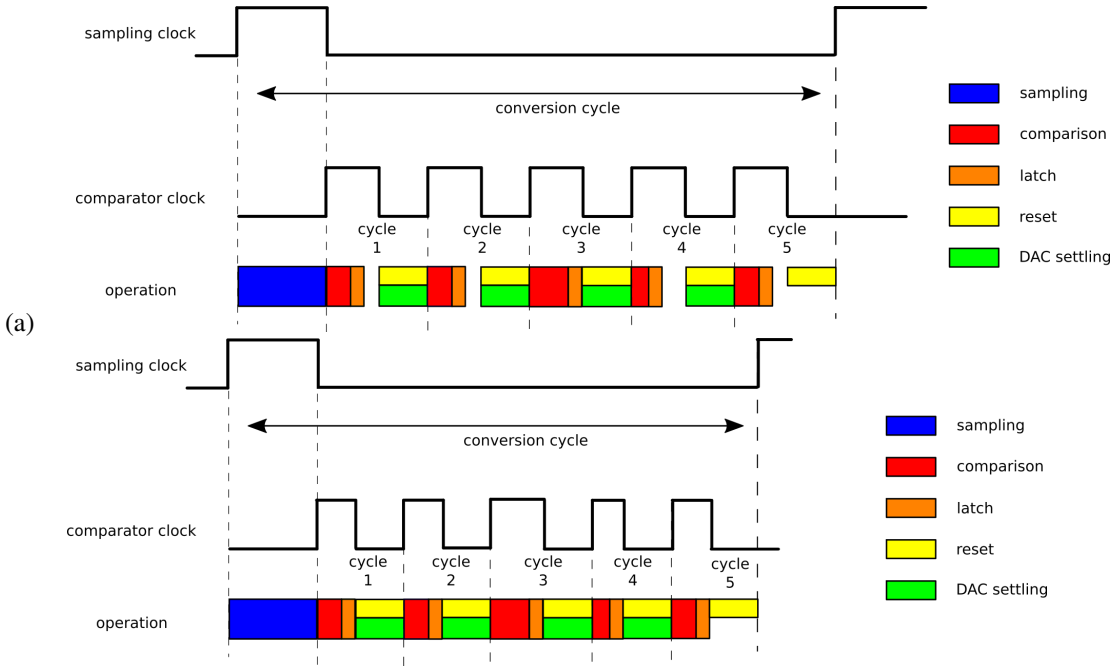


Figure 4.16: *Waveform diagrams of: a) synchronous SAR, b) asynchronous SAR.*

4.5.5 Loop Unrolled SAR

The conventional SAR topology presents a limitation of the maximum achievable speed due to the critical path length, even with asynchronous timing. As shown in Fig.4.16, after each decision of the comparator, the result must be store in a memory element (as a latch) which will drive a branch of the CDAC, according to the chosen switching algorithm. Meanwhile, the comparator can be reset in order to be ready for the next comparison. An alternative SAR topology, called loop unrolled, proposed for the first time in [158], employs a different comparator for each bit cycle, instead of a unique comparator (Fig.4.17). In this way, each comparator, after its decision, does not need to be reset, but thanks to its latch behaviour, can store the result and drive the respective branch of the CDAC. Thus, the critical path is shortened because of the suppression of the latch time in each cycle. It is worth noting that employing a dynamic comparator as the StrongARM comparator, which does not dissipate static power, the power consumption for the comparators is exactly the same. In fact, instead of a single comparator triggered N times in a conversion cycle as in a traditional SAR, there are N comparators triggered only once for conversion cycle. Actually, this mechanism mitigates the electromigration and self-heating, having reduced the switching activity in the comparator. This architecture allows speed up and power saving, due to the removal from the critical path of the latch for storing the result of each comparator decision. The reset of all the comparators takes place at the end of the conversion cycle, and it is relaxed since it is not in the critical path any more. As a result, also the speed requirement of the reset switches S1-4 in the StrongARM comparator (Fig. 4.9) are relaxed, allowing minimal size transistors and then less parasitic loads on the critical nodes of the comparator. It is worth noting from Fig. 4.17 that the intrinsic principle of loop unrolled SAR is asynchronous, because after each decision, a proper circuit detects it and triggers the next comparator, waiting a proper delay longer than the DAC settling time. A possible circuit which generates the ready signal for the following comparator is shown in Fig.4.18. The first nand gate determines the comparator decision, while the following logic gates recognizes the end of the conversion or the beginning of the sampling phase. An additional programmability has been added in the path, because of the possible variations at cryogenic temperatures. It is possible, by means of an additional configuration bit, to add two inverter delays in the path of enable signal generation. In this way, more settling time is allowed for the DAC, in the case of arising of settling time errors due to changings of device behaviours at 4 K.

The typical clock waveforms of asynchronous timing in loop-unrolled SAR is depicted in Fig.4.19. In this architecture it is also straightforward to run the converter faster, at the cost of less resolution. In fact, by means of the addition of few logic gates and configuration bits, it is possible to disable the ready signal that triggers the last comparator (or also the second to last and so on).

The main drawback of the loop unrolled architecture is, a part the increasing of circuital complexity due to the presence of N comparators instead of only one, the effect of the comparators' offset on the converter resolution [172]. In a traditional SAR, an offset of the comparator, as long it does not vary from cycle to cycle, is reflected into a converter offset, that can be ignored in many applications or easily calibrated off-line. In a loop unrolled SAR, on the contrary, the offsets of the different comparators may introduce distortion, in a similar fashion as in flash converter. Then, the need of an

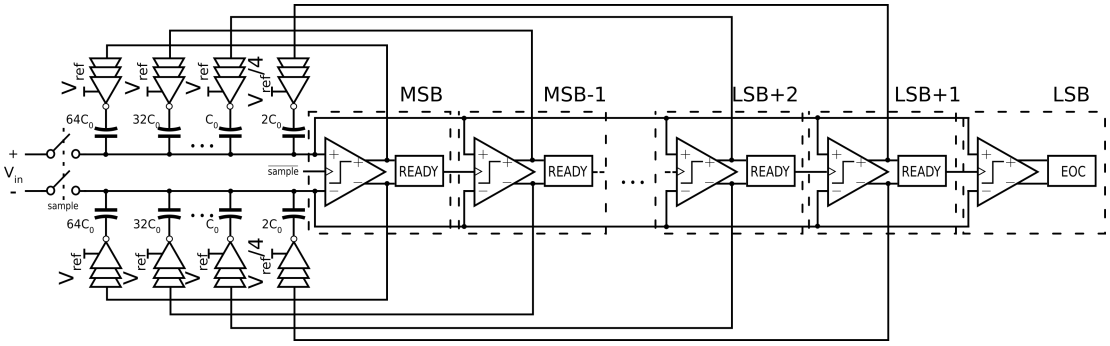


Figure 4.17: *9 bits loop unrolled architecture.*

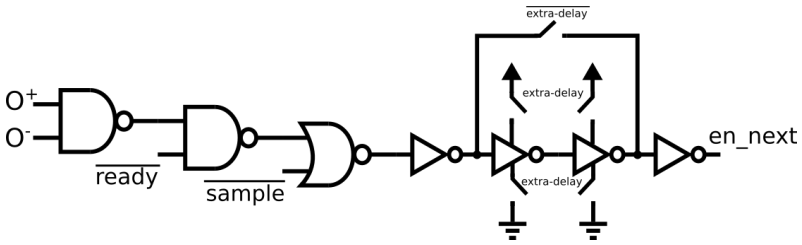


Figure 4.18: *Schematic view of the enable signal generator.*

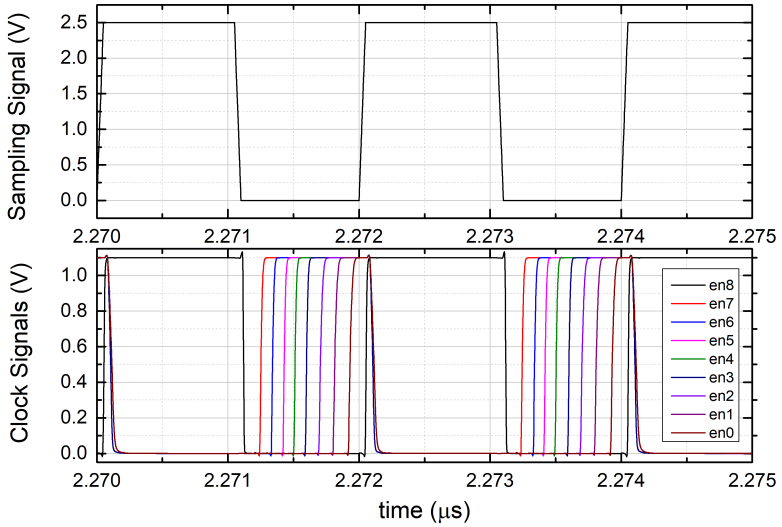


Figure 4.19: *Timing of asynchronous clocks in loop unrolled SAR. On top the sampling signal provided from outside, below the clock signals that enable the different comparators.*

offset calibration for each comparator becomes mandatory.

The use of N different comparators for the N different bit-cycles, beyond the advantage of reducing the critical path, allows also the optimization of each comparator in terms of noise/power. As well known, the last bit-cycles during the SAR conversion are the most critical. In fact, the differential voltage of the CDAC is halved every bit cycle; then, the probability of making a mistake during the comparison due to thermal noise increases exponentially with the number of cycles. A possible optimization on the power allocation for the comparators has been proposed in [173]: sizing differently

each comparator according their respective bit cycles, it is possible to save power for the comparators allocated for the first bit cycles and spending more power for the comparators employed for the last decisions. The net result is a power saving compared to the traditional design of N equal comparators, tarketing the same effective resolution. A simpler approach that allows power saving without introducing the complexity of N different comparator sizings and layouts, consists in using two different sets of comparators: a low power/high noise sizing for the MSB comparators, and a high power/low noise sizing for the LSB comparators.

4.5.6 Calibration network

There are several ways to implement the calibration of the comparator offset. Two main categories of calibration will be discussed: background and foreground. The background calibration runs continuously and it is usually implemented in circuits where it is needed to track continuously the variations of the quantity that must be calibrated. It is also a solution frequently adopted in the literature with loop unrolled topologies [172]. Usually, an additional bit cycle is allocated for the calibration of all the comparators. In this extra cycle, the differential inputs of the converter are shorted; the N comparators decide all together and their decisions are used to correct the offsets. The offset correction occurs by means of a self-calibration circuits, one for each comparator. This procedure is also beneficial for metastability. In the case that metastability occurs, in fact, the extra cycle used for calibration is skipped and the period is used for solving the metastability. Typically, the missing of one cycle of calibration does not impact on converter performances.

In the application for which this data converter is designed, fast PVT variations are not expected. Actually, working at cryogenic temperatures in dilution refrigerators, the environmental conditions are well controlled and stable because of the qubit requirements. For this reason, we opted for a foreground calibration. The foreground calibration runs only at the start-up of the converter, or it can be duty-cycled during the normal operations. After the calibration loop has been run, the configuration bits are stored in a memory and the calibration network works statically.

The introduction of a static DAC for the calibration of the offset of each comparators is required. As already mentioned in paragraph 4.5.2, a possible way is to add programmable bank of capacitors on the comparator internal nodes P,Q (Fig.4.9). However, this approach can limit severely the maximum speed of the comparator and it is preferred in higher resolution, lower speed application. An alternative solution [174] implements a current DAC which injects currents on the nodes P,Q to compensate the unbalance due to the offset; it has the drawback of introducing an additional static current consumption, function of the offset that needs to be corrected.

The calibration network chosen for this design consists in a 6 bit resistive DAC, which provides the differential signals for two differential pairs added as shown in Fig.4.20. The two additional pairs are used to split the calibration in a coarse and a fine part, in order to reduce the DAC complexity. The pair for coarse calibration made up of M1c-M2c is a scaled version of the input pair M1-M2, with a width ratio equal to $1/4$. The common mode voltage from the resistive DAC is set to $3/4V_{dd}$, thus the differential voltage ($V_{c+} - V_{c-}$) generated by the DAC can be set to a maximum value of 0.55 V, that implies a maximum calibratable offset voltage of $0.55V/4 = 0.1375V$

from the coarse DAC. The coarse calibration has only 4 bits, while the fine one exploits all the 6 bit of the DAC resistor string. The additional pair M1f-M2f is sized with an additional width ratio of $1/4$, in order to calibrate offsets lower than 1 mV (i.e. less than 1 LSB). Part of the calibration network is used by all the comparators employed in the loop-unrolled SAR, sharing the same resistor string. In order to avoid cross-talk from the different comparators, decoupling MOSFET capacitors have been added for every devices of the additional calibration pairs.

This kind of calibration, employing additional differential pairs connected to the internal nodes P,Q, also provides a speed up of the comparator delay time, at the cost of increasing the comparator thermal noise. The same principle has been exploited in [175] in the so called "gm-boosted Strong-ARM comparator. The additional pair connected to the clock signal in [175] provides a common mode current that reduces the amplification time. From 4.9, it is straightforward to evaluate the expression of the comparator thermal noise with the presence of the additional pairs. A more efficient result could be obtained by increasing the dimensions of the input pair, at the cost of more attenuation of the full-scale range and more kickback due to the increased parasitic capacitances.

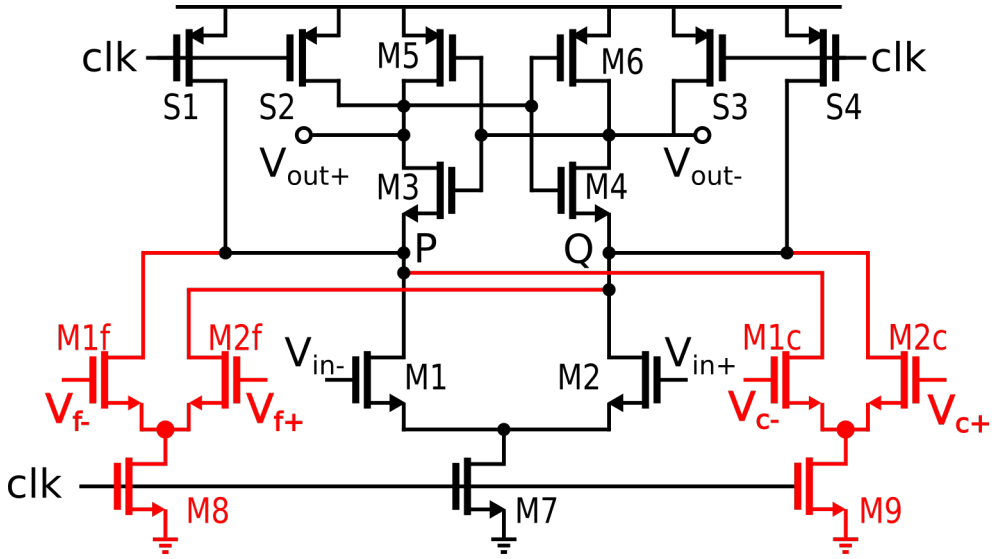


Figure 4.20: *Schematic view of the Strong-ARM comparator with additional input pairs for calibration.*

As already stated, the foreground calibration procedure is performed before starting the conversions. Depending on the switching algorithm, the different comparators in the loop unrolled topology may work with different input common modes. It is very important to provide, during the calibration loop, the same input common mode present during the normal conversion operations. In background calibration for loop unrolled SAR [172], all the comparators are calibrated at once, providing the same input common mode for all of them. If that is the case, only switching algorithm able to guarantee a constant input common mode are allowed. The chosen algorithm, optimized for facing the comparator behaviour changing at cryogenic temperatures, is based just on the common mode variations of the DAC voltage and would not be suitable for background calibration.

The easier way to guarantee the right calibration of the comparators' offset, taking

into account the input common mode variations, is to emulate the normal SAR operations during the calibration phase. Calibration is performed after shorting the top plates of the CDAC as shown in Fig.4.24. During the sampling phase, only an input common mode voltage equals to the one of the input signal that needs to be converted is present. Then, the first comparator will receive a zero differential signal, with the same input common mode as during normal operations. The decision of the comparator will depend on the sign of the offset, and the result of the comparison will update the differential signals from the resistive DAC for the calibration pairs. After the decision, the first branch on one side of the CDAC will be driven accordingly to the switching algorithm, modifying only the common mode on the top plates. The same procedure is repeated for all the comparators, emulating perfectly a normal SAR conversion. The result of the decisions of each comparator will be used to update the digital input of the resistive DAC. After M identical cycles of the calibration loop, where M is the number of bits of the resistive DAC (the sum of the resolution of the coarse and the fine DAC), the calibration loop is completed and the offset of each comparator is calibrated. Actually, this procedure can run slower than the normal SAR operations and it will be repeated several times in order to average the results of each calibration loop and achieve an accuracy on the residual offset below the thermal noise level of the comparators.

4.5.7 Ping-pong SAR

Another critical block is represented by the input sampling switch. Considering the maximum target frequency of 1 GHz, the linearity of the sampling switch can be a major concern. A fundamental aspect about the requirements of the sampling switch regards the sampling period, that is the fraction of the conversion cycle allocated for the sampling of the input signal. Typically, in a single channel ADC the sampling period is in the order of 10-20 $\%$ of the conversion period. This would mean that only 100-200 ps are allocated for the sampling. As an example, in order to reach an accuracy of 8 bit, a on-resistance of the sampling switch lower than 500 Ω would be needed. This specification would be considering an input driver with a 0 Ω impedance; considering also the output impedance of the input driver, than the sampling switch resistance must be even lower and also the power consumption to guarantee a sufficient driving capability would be very high. The design of the input driver will not be part of this work; from now on, the focus will be only on the sampling switches.

Simulations on pass-gates performed at different input frequencies show that they are not even sufficient to guarantee 6 bit of linearity at -55 °C. Fig.4.21 depicts the comparison of pass-gate THD at RT and -55 °C: a deterioration of the THD at lower temperatures due to the increase of the threshold voltage looks evident. Also techniques of body biasing are not enough to reach a sufficient linearity at high frequency and low temperature. This problem is well known in the literature also for RT design; typical solutions employ bootstrapping techniques for the sampling switch as in [87]. However, these techniques require additional power consumption, as well as complexity increasing; the risk of malfunctions of this critical block at cryogenic temperatures dissuade us from the implementation of bootstrapped switches. We decided to adopt a safer approach, choosing the available thick oxide devices present in the design kit, that allows a maximum gate voltage of 2.5 V. With such a gate voltage, even at -55 °C, a simple NMOS shows a sufficient linearity even at high frequency (Fig.4.22). This

solution does not come for free: an increasing of the complexity and the power consumption of the clock chain, in order to guarantee a sufficient low jitter on the higher voltage clock needed for the sampling switch, is the cost that we have to pay.

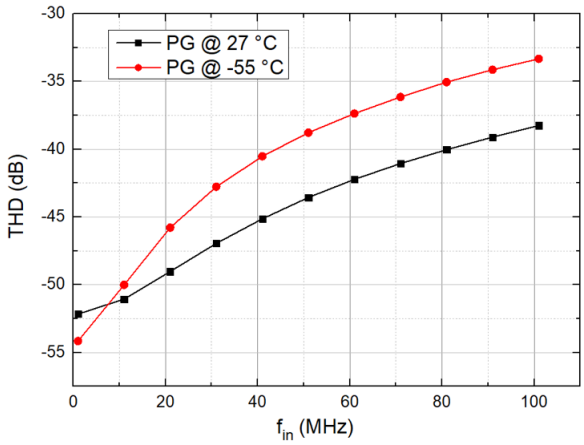


Figure 4.21: *THD of a pass-gate varying the frequency of the sinusoidal input signal, compared at RT and -55°C.*

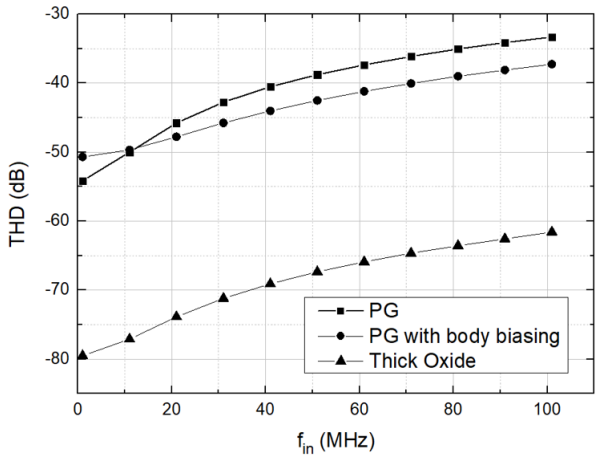


Figure 4.22: *THD comparison of a PG, a PG with body-biasing and a thick-oxide NMOS at RT and -55°C.*

Another improvement concerning the sampling switches, and in general the speed requirement for every block of the ADC, comes from the implementation of time-interleaving techniques. Adopting a ping-pong approach, i.e. a time-interleaving ADC with two slices, half of the conversion period is allocated for the sampling of one slice while the other is converting; the opposite occurs during the second half (Fig.4.23). Moreover, it is possible to reach the target sampling frequency of 1 GHz with a single slice SAR capable of working at 500 MHz, relaxing the speed requirements for the comparators and the logical circuits. Speed improvement due to time-interleaving are not gained without any drawback. A part from the obviously doubling of the area and power consumption, time-interleaving ADCs require matching conditions between the different slices [12]. Gain, offset and bandwidth mismatch, as well as time-skew be-

tween the two sampling clock edges, may introduce additional spurs on the converted signal spectrum. Additional calibration circuitry must be implemented to limit these sources of errors, together with off-line calibration of the whole ADC.

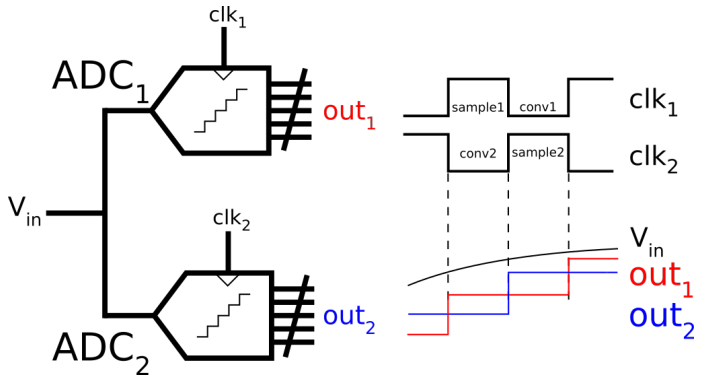


Figure 4.23: *Block diagram of ping-pong architecture and waveform of clock, input and output signals.*

4.5.8 Final architecture

The proposed SAR converter implements a ping-pong architecture in order to double the final sampling frequency. Problems of gain error and linearity mismatches between the two slices will be calibrated off-line, while offset mismatch will be almost completely compensated with the foreground calibration implemented for each single slice. Time skew between the two sampling signal will be calibrated by means of a fine alignment of the two clock signals, provided by an additional circuitry. The results of the conversion will be stored in a SRAM with sufficient size to effectuate the spectrum analysis of slow input signal down to 10 MHz. Each single slice is a SAR converter with a programmable resolution N (from 6 to 9 bit). The converter architecture is a loop unrolled that employs 9 different comparators. An optimization of the comparator sizing is present, with two different sets of StrongARM comparators, one for the least significant bits and the other one for the most significant bits. A modification of the "set-and-down" algorithm has been implemented, in order to modify the input common mode and to face the threshold voltage increase at cryogenic temperatures. Additional programmability has been used to set two possible delays in the generation of the asynchronous clocks, to mitigate potential settling time errors not observed from simulations due to the lack of proper device models for cryogenic temperatures. The foreground calibration loop allows the offset compensation of each comparator even in presence of input common mode variations, differently from typical solutions present in the literature. Fig.4.24 shows the final schematic view of the proposed SAR slice designed for cryogenic environment.

4.5.9 Simulations and results

Due to the lack of proper device models at 4 K, simulations have been performed at -55°C, that is the minimum temperature at which the models provided by the foundry are fully characterized. Electrical simulations performed with Spectre simulator were used to verify the behaviour of the single slice SAR ADC. The following simulations

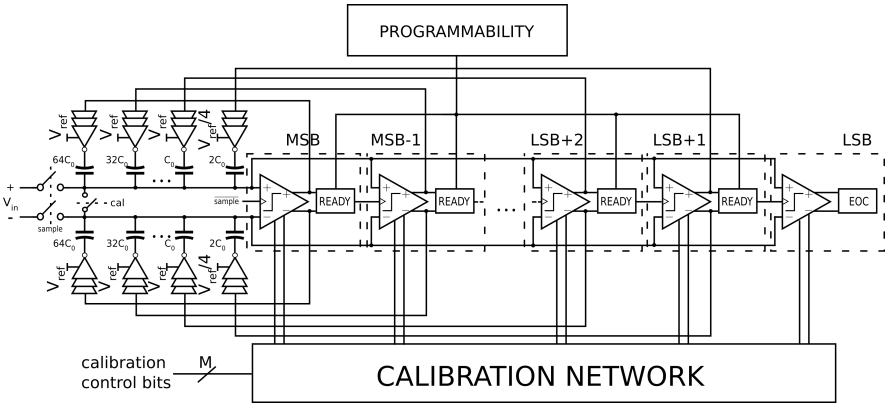


Figure 4.24: *Overall schematic view of the SAR slice.*

take into account only the post-layout parasitic extraction of the CDAC; for the other blocks, the pre-layout schematic views were used.

Fig.4.25 shows the INL curves for all the possible resolution configurations, in nominal conditions. Maximum INL of 0.54 LSB in the 6 bit configuration and a maximum INL of 0.8 LSB in the case of 9 bit resolution have been observe. A worsening of the linearity performance may be ascribed partially to the sampling switches and mainly to the CDAC, that was designed for 6 bit linearity.

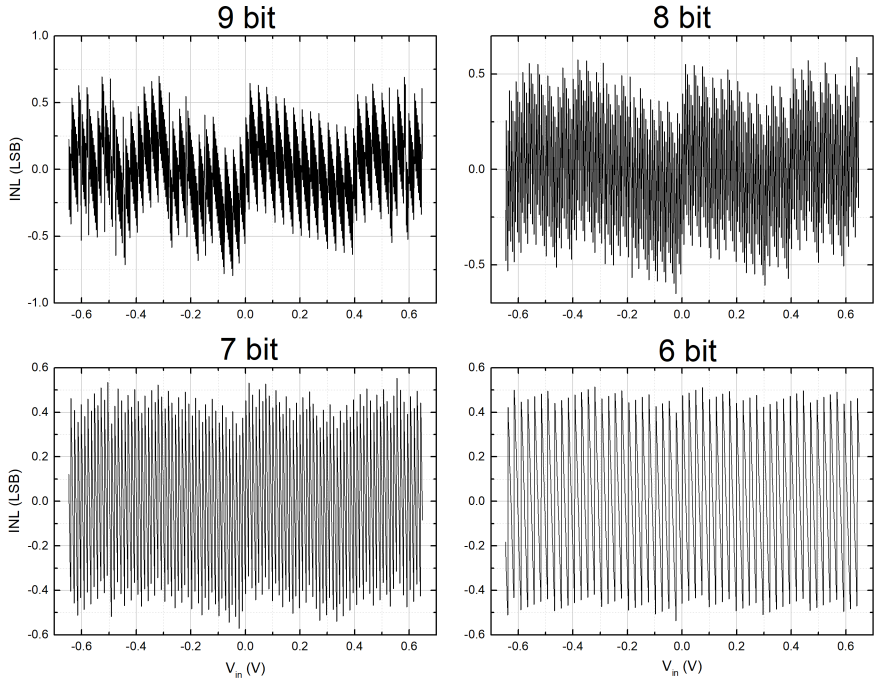


Figure 4.25: *Converter INL for the four possible nominal resolution.*

To characterize the dynamic performances of the converter, spectrum analysis of transient simulations (with and without electrical noise) have been performed, by means of the FFT on the output converted data. Here, 9 bit and 8 bit configurations spectrum are shown (figs. 4.26 and 4.27), which represent the most critical case in terms

of resolution. From transient noise simulations, a SINAD of 47.08 dB and 44.56 dB, respectively in the configurations of 9 and 8 bit, have been obtained. The total harmonic distortion simulated is sufficiently low for the target application. A total power consumption of 274 µA in the 9 bit configuration confirms the great power efficiency of the SAR converter and in particular of the adopted loop unrolled topology. Considering a doubling of the power dissipation due to ping-pong approach, 13.7 µW/qubit would be the result obtained from simulations. It is worth remarking that only parasitic extraction for the CDAC has been taken into account: an increase of the power consumption for the comparator and the logic blocks is expected, and particular attention has to be spent on the layout of each block.

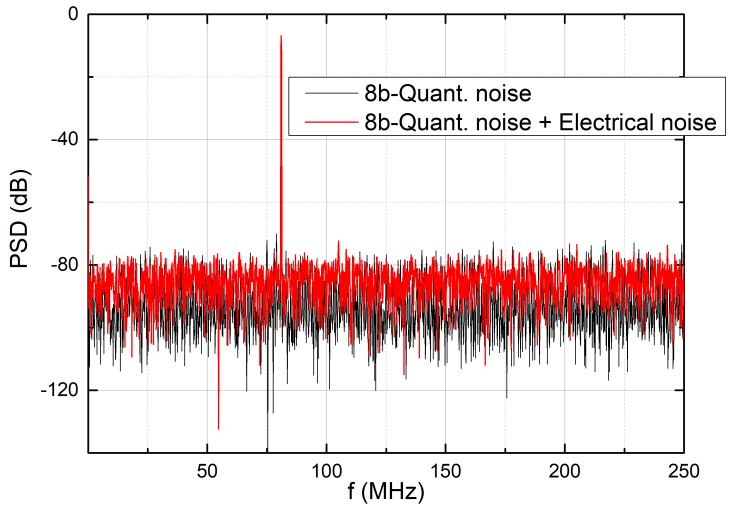


Figure 4.26: *SAR output spectra with 8 bit nominal resolution, compared with and without electrical noise.*

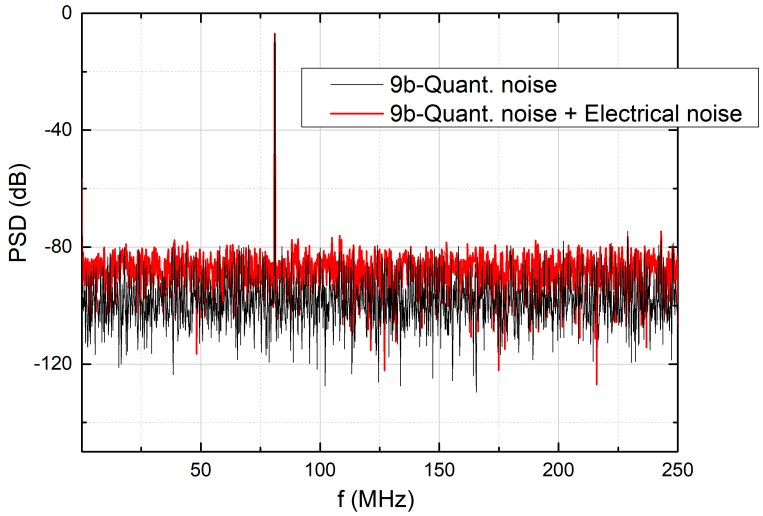


Figure 4.27: *SAR output spectra with 9 bit nominal resolution, compared with and without electrical noise.*

Table 4.1 recaps the dynamic performances and the power consumption of the con-

Table 4.1: *SAR ADC performances in 9 bit and 8 bit configurations*

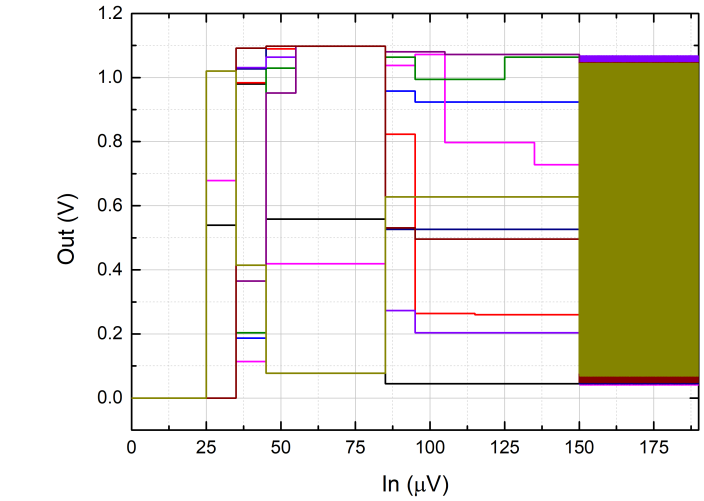
Resolution (bit)	f_S (MHz)	SQNR (dB)	SINAD (dB)	THD (dB)	P_{DAC} (µW)	P_{logic} (µW)	P_{cmp} (µW)	FoM_W (fJ/conv)
8	500	48.07	44.56	-65.97	109.24	101.73	30.51	3.75
9	500	53.58	47.08	-64.79	110.44	109.80	54.44	2.98

verter in the two configurations with highest resolution. The power dissipation has been split in the different contributions: from the CDAC, the logic blocks and the comparators. A FoM_W of $3 \div 4$ fJ/conv is obtained from simulations at -55°C. A slight worsening is expected after the extractions of the post-layout parasitics of the whole converter, while it is not easy to predict the performances at cryogenic temperatures. Higher threshold voltages could limit the comparators' speed (even if proper countermeasures have been adopted during the design), but thermal noise drop could further increase the SINAD in the 9 bit configuration. However, if the reported FoM_W would be confirmed (or at least its order of magnitude), even at RT the proposed converter would be competitive with the actual state-of-the-art. Concerning cryogenic temperatures, it would represent a big step forward respect to the works present in the literature. Its characteristics make it appealing for present setups of qubit RF reflectometry readouts, and still suitable for the coming years.

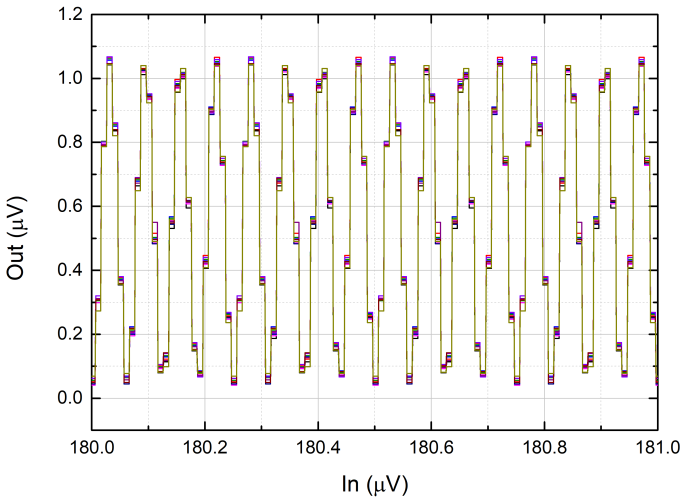
Fig.4.28 shows 10 MC runs of the SAR converter, highlighting the effectiveness of the proposed calibration. Calibration has been run for the first 150 µs at lower frequency respect to the normal operation frequency. At the end of the calibration phase, a sinusoid has been applied. In the graph on the right, a zoom on the converted sinusoudal waveforms of the 10 MC runs show the effectiveness of the calibration. In all the 10 MC runs, dynamic performances are confirmed. A part for a small residual offset, different gain errors in the 10 realizations are noticeable. This kind of error, that could introduce additional spurs in a ping-pong architecture, will be calibrated off-line.

4.6 Discussion and conclusion

This chapter presents the description of a full-custom design of a SAR converter for cryogenic applications in 40 nm CMOS technology of TSMC. The converter is thought for quantum computing applications, more precisely for radio-frequency reflectometry readout interface of spin qubits. A brief description of quantum computing and cryo-CMOS design is present, in order to contextualize this work. The focus is on the most challenging requirements for conventional electronics aimed to work in an extreme environment as the liquid helium stage in a dilution fridge. A ping-pong approach, with two loop unrolled SAR slices, has been adopted to reach a maximum sampling frequency of 1 GHz and a programmable resolution from 6 to 9 bit. This work has concentrated on the optimization of the single slice, implementing ad-hoc techniques for cryogenic applications. Electrical simulations performed at -55 °C, taking into account also electrical noise, show a FoM_W around 3 fJ/conv, which is comparable with the actual state-of-the-art. If proven to work at cryogenic temperatures, this ADC would be the fastest converter operating at 4 K.



(a)



(b)

Figure 4.28: *10 MC runs of transient simulations of the SAR output, converterd in voltage. a) Complete transient with initial calibration procedure and conversion of the sinusoidal input signal. b) Zoom of the previous graph of the 10 MC runs of the converted sinusoid.*

APPENDIX $\mathcal{A}$

Time-discrete analysis of switched-capacitor circuits

A.1 Switched-Capacitor circuits

Switched-Capacitor (SC) circuits find their natural implementation in the CMOS processes, due to the possibility of realizing good switches and operational amplifiers with high input impedance. Thanks to the capacitive ratios employed for realizing precise gains, no resistors are needed, avoiding a resistive load for the amplifier. In this way, the amplifier may be designed with a single stage topology, achieving a large gain thanks to the high output impedance, thus reducing a lot the design complexity. Furthermore, SC integrators allow large and precise time constants without large values of the passive elements. The basic principles of SC circuits are: i) the sampling of the input voltage on a capacitor; ii) the transmission of the charge proportional to the input voltage on other capacitors. Both operations must be performed correctly; amplifier finite dc gain, noise and offset may affect heavily the overall performances. Due to its intrinsic discrete-time nature, this kind of circuits is extremely popular for sampled-data systems, as in Analog-to-Digital Converters.

The limit of SC circuits, of course, is related to their application for time-continuous signals. Because of the intrinsic sampling operation, a proper relationship between the circuit clock frequency and the input signal bandwidth must be ensured. Furthermore, the operational amplifier speed must be high enough to guarantee a proper settling of the capacitor voltages in half of the clock period.

The two pivotal SC building blocks are SC integrators and amplifiers. In this appendix, we will focus on the first category, due to its importance in DT Δ-Σ modulators, as analysed in chapter 2 and 3. Besides a general analysis of the parasitic-insensitive integrator, considering also the effect of finite dc gain and noise of the operational am-

plifier, we will deeply analyse the behaviour of the novel two-stage, high dc gain, SC integrator proposed in [102].

A.2 Parasitic-Insensitive Switched-Capacitor Integrator

The parasitic-insensitive integrator is one of the most important switched-capacitor circuits, very diffused in Δ-Σ and time-discrete analog filters. The circuit, shown in Fig.A.1, is made up by an operational amplifier with a dc gain A, two capacitors C_s and C_f, and four switches driven in two alternative phases. The name of this circuit is due to the low sensitivity of the charge transfer from the parasitic capacitors of the switches. In this configuration, the two input signals (V_1 and V_2) are sampled at the end of phase 1 and phase 2, respectively; a charge proportional to the difference of the input signals is periodically transferred to the integrating capacitor C_F, implementing the accumulation (i.e. the time-discrete integration function).

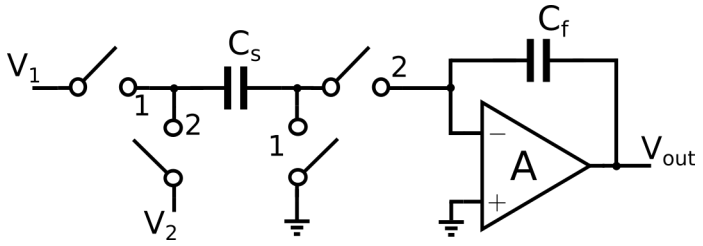


Figure A.1: *Schematic view of the parasitic-insensitive switched-capacitor integrator.*

In this first analysis, the ideal behaviour of the circuit will be studied, neglecting the effects of amplifier offset, noise and finite dc gain; switch non-idealities will be neglected as well. In order to study the circuit, the charge accumulated on each capacitor at the end of each phase can be derived from the differential voltage on the capacitor itself. Then the charge transfer from one phase to the following one allows us to derive the final expression of the output voltage at the end of each phase. It is possible to write the differential voltages on the capacitor C_S and C_F in the two phases, considering the signs as expressed in Fig.A.2. The timing diagram of the clock cycle which controls the two sampling phase is reported in Fig.A.3. It is worth mentioning that two non-overlapping phases are required in SC circuits, to not spoil the correct charge transfers during the clock transitions. With $V_x^{(i)}$, it is indicated the value of the voltage V_x at the end of the phase i.

$$\begin{cases} V_{C_S}^{(1)} = V_1^{(1)} \\ V_{C_F}^{(1)} = -V_{out}^{(1)} \end{cases} \tag{A.1}$$

$$\begin{cases} V_{C_S}^{(2)} = V_2^{(2)} \\ V_{C_F}^{(2)} = -V_{out}^{(2)} \end{cases} \tag{A.2}$$

The voltage on the capacitor C_F at the end of the phase 2 can be written as the voltage on the same capacitor at the end of the previous phase, plus an increment of voltage due to the variation of charge transferred from the capacitor C_S from phase 1

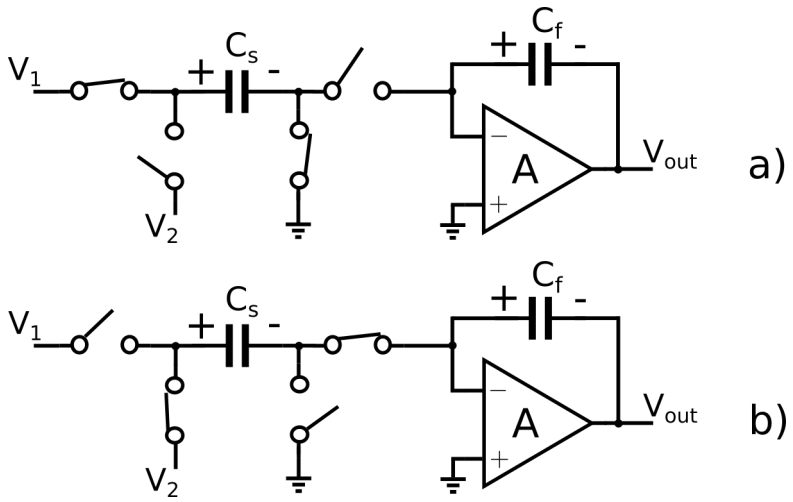


Figure A.2: *Configuration of the PI integrator in the two phases: a) phase 1, b) phase 2.*

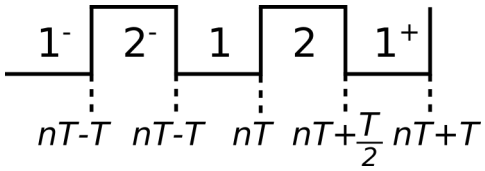


Figure A.3: *Timing diagram of the clock signal that drives the switched capacitor circuit. The two phases are indicated. The sampling instants at the end of each phases are represented as the sequence: nT-T, nT-T/2, nT,+++*

to phase 2:

$$V_{C_F}^{(2)} = V_{C_F}^{(1)} + \frac{\Delta Q_{C_F}^{(1\to2)}}{C_F} = V_{C_F}^{(1)} + \frac{\Delta Q_{C_S}^{(1\to2)}}{C_F} \tag{A.3}$$

$$\Delta Q_{C_S}^{(1\to2)} = C_S(V_{C_S}^{(2)} - V_{C_S}^{(1)}) = C_S(V_2^{(2)} - V_1^{(1)}) \tag{A.4}$$

It is possible to write the output voltage at the end of the phase 2 combining equations eqs. (A.1) to (A.4) and obtaining:

$$V_{out}^{(2)} = V_{out}^{(1)} + \frac{C_S}{C_F}(V_1^{(1)} - V_2^{(2)}) \tag{A.5}$$

Considering that the output voltage during phase 1 is the same as in phase 2 (phase 1 is called the hold phase), we can write the output voltage at the end of phase 2 and the next phase 1 as:

$$\begin{cases} V_{out}^{(2)} = V_{out}^{(2^-)} + \frac{C_S}{C_F}(V_1^{(1)} - V_2^{(2)}) \\ V_{out}^{(1^+)} = V_{out}^{(1)} + \frac{C_S}{C_F}(V_1^{(1)} - V_2^{(2)}) \end{cases} \tag{A.6}$$

C_S/C_F is also called the integrator gain, from now on expressed with k, and it sets the integrator unity gain-frequency.

It is possible to write the expression of the output, for example in phase 1+, in the z-domain, typically used to describe the behaviour of discrete-time circuits as the switched-capacitor ones:

$$V_{out}(z) = V_{out}(z)z^{-1} + k(V_1(z)z^{-1} - V_2(z)z^{-1/2}) \tag{A.7}$$

Defining the input signal $V_{in}(z) = V_1(z) - V_2(z)z^{1/2}$, we can write the integrator transfer function in the z domain as:

$$H(z) = \frac{V_{out}(z)}{V_{in(z)}} = \frac{kz^{-1}}{1 - z^{-1}} \tag{A.8}$$

The last expression is the ideal transfer function of an integrator with delay, also called forward Euler integrator. Using the substitution $z = e^{j2\pi fT}$, where T is the sampling clock frequency, it is easy to obtain the integrator transfer function in the frequency domain:

$$H(f) = \frac{V_{out}(f)}{V_{in(f)}} = \frac{ke^{-j2\pi fT/2}}{2jsin(2\pi fT/2)} \tag{A.9}$$

Fig.A.4 shows the comparison of the magnitude Bode plot of the discrete-time (DT) integrator transfer function, compared to the continuous-time (CT) integrator $(1/j2\pi f)$ and the frequency response obtained by means of the Tustin transformation of the CT integrator. It is worth noting how the DT integrator approximates almost perfectly the CT integrator, for frequency lower than a decade of the sampling frequency. The z-transformation of the CT integrator approximates better the DT integrator response but stills introduces some errors for f close to the sampling frequency.

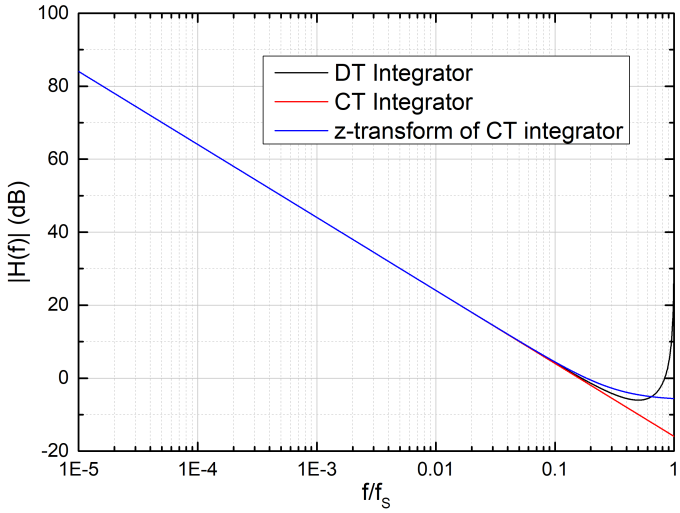


Figure A.4: *Comparison of magnitude Bode plot of discrete-time integrator, continuous-time integrator, and the z-transformation of the continuous-time integrator.*

The integrator unity-gain frequency, as it looks evident from the graph in Fig.A.5, is directly proportional to the gain k of the integrator.

A.2.1 Finite dc gain

In order to study the effect of the amplifier finite dc gain on the integrator transfer function, it is possible to replicate the calculations done in the previous paragraph,

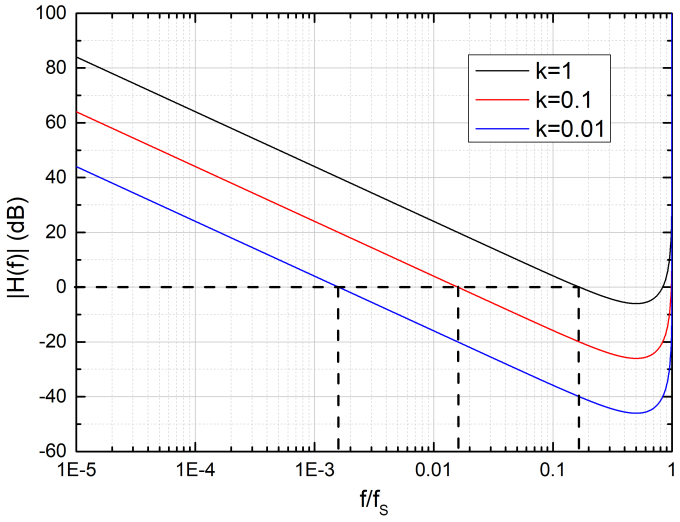


Figure A.5: *Comparison of the magnitude Bode plot of the z-transform function sweeping the integrator gain k.*

considering a constant amplifier gain A. Due to the finite gain, at the inverting input of the amplifier, it will not be present zero (perfect virtual ground), but a voltage equal to: $-V_{out}/A$.

Than, it is easy to rewrite equations eqs. (A.1) and (A.2) as:

$$\begin{cases} V_{C_S}^{(1)} = V_1^{(1)} \\ V_{C_F}^{(1)} = -\frac{V_{out}^{(1)}}{A} - V_{out}^{(1)} \end{cases} \tag{A.10}$$

$$\begin{cases} V_{C_S}^{(2)} = V_2^{(2)} + \frac{V_{out}^{(2)}}{A} \\ V_{C_F}^{(2)} = -\frac{V_{out}^{(2)}}{A} - V_{out}^{(2)} \end{cases} \tag{A.11}$$

From those, repeating the same algebraical calculations seen before, the expressions of integrator output at the end of phase 2 and 1+ are:

$$\begin{cases} V_{out}^{(2)} = V_{out}^{(2^-)} + \frac{A}{1+A} k (V_1^{(1)} - V_2^{(2)} - \frac{V_{out}^{(2)}}{A}) \\ V_{out}^{(1^+)} = V_{out}^{(1)} + \frac{A}{1+A} k (V_1^{(1)} - V_2^{(2)} - \frac{V_{out}^{(1^+)}}{A}) \end{cases} \tag{A.12}$$

The integrator transfer function in the z domain, considering the finite gain A, can be written as:

$$H(z) = \frac{V_{out}(z)}{V_{in(z)}} = \frac{A}{1+k+A} \frac{kz^{-1}}{1 - z^{-1}\frac{1+A}{1+k+A}} \tag{A.13}$$

It is easy to verify how, for the limit of A to infinite, the integrator transfer function becomes the expression in A.8. This transfer function is equal to the one of a continuous-time low-pass filter, with dc gain equal to A and cut-off frequency around: $\frac{f_s}{2\pi} k/(1+A)$, as shown in Fig.A.6.

In this condition, the integrator is also called "leaky integrator", and it is possible to express its transfer function with the following generic expression:

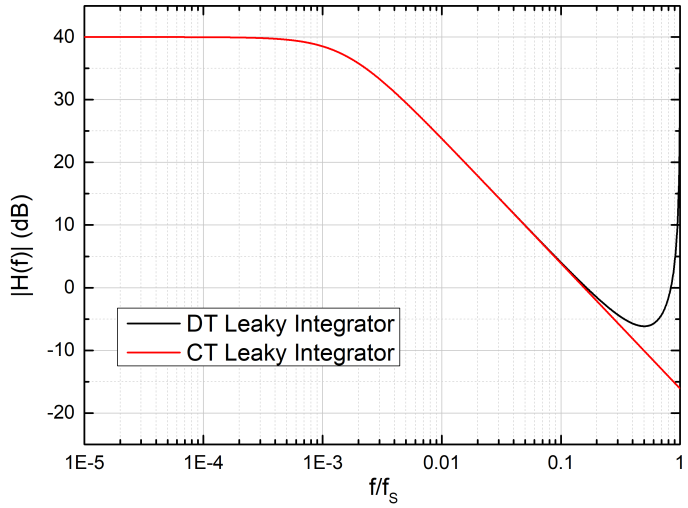


Figure A.6: *Comparison of the magnitude Bode plot of the z-transform function sweeping the integrator gain k.*

$$H(z) = \frac{V_{out}(z)}{V_{in(z)}} = k\frac{\lambda z^{-1}}{1-\alpha z^{-1}} \tag{A.14}$$

where λ is the integrator gain error and p is the integrator phase error. Typically, the phase error is more critical in many applications like state-variable filter or Δ-Σ converter. For the parasitic-insensitive, the two errors are:

$$\begin{cases} \lambda = \frac{A}{1+k+A} = 1 - \frac{1+k}{1+k+A} \\ \alpha = \frac{1+A}{1+k+A} = 1 - \frac{k}{1+k+A} \end{cases} \tag{A.15}$$

Both errors are inversely proportional to the dc gain of the amplifier.

A.2.2 Noise analysis

In this paragraph, we will concentrate our attention on the noise analysis. About the offset, it is straightforward to notice that an amplifier offset is reflected directly in a input-referred integrator offset.

The following noise analysis of the parasitic insensitive integrator follows the one proposed in [45]. The referred-to-input (RTI) noise of the SC integrator can be evaluated considering the expression of the output noise in the z-domain, and then dividing for the integrator transfer-function. In this analysis, we will be considered only thermal noise, neglecting flicker noise component. The RTI power spectral density of the amplifier can be expressed in a general way as: $4kT/G_M\gamma$, where G_M is the transconductance of the input pair, while γ is a multiplicative factor that takes into account the amplifier topology. With that expression, the amplifier noise looks like the one of a resistor equal to $1/G_M$, with an excess of noise γ.

Fig.A.7 shows the equivalent circuit for the noise analysis in the two phases. The switches are represented with their r_{on} resistance and the relative thermal noise source. The amplifier, instead, it is represented with its input impedance (Fig.A.8-a) and the RTI noise source.

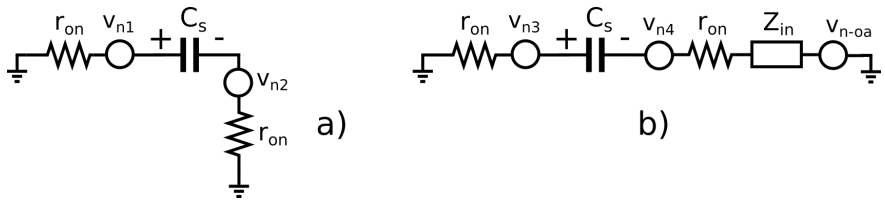


Figure A.7: *Schematization of the PI integrator in the two phases, considering the on-resistance and the noise from the switches, and modelling the amplifier with its input impedance and RTI noise. a) Phase 1; b) phase 2.*

In order to consider the input impedance of the amplifier, we will consider a single-stage amplifier topology (as a folded-cascode amplifier, that is a standard choice in several implementations). Under the hypothesis of output resistance much higher than the inverse of the input transconductance, (that is the typical case), it is possible to consider Z_{in} constant, equal to $1/G_M$, as it can be easily derived from the small signal model depicted in Fig.A.8-b.

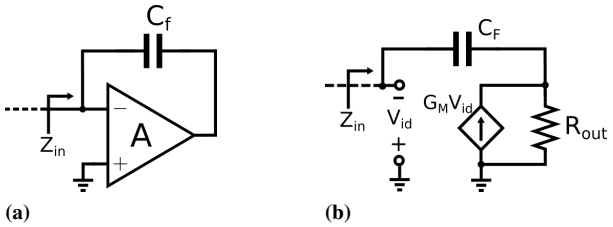


Figure A.8: *a) Input impedance of the operational amplifier with capacitive feedback. b) Small signal model of the operational amplifier.*

During phase 1, the voltage noise on capacitor C_S can be expressed in the frequency domain as:

$$V_{n-C_S}(f) = \frac{v_{n1} + v_{n2}}{1 + jf/f_{p1}} \tag{A.16}$$

where f_{p1} is the cut-off frequency of the RC circuit of phase 1, i.e. $f_{p1} = 1/(2\pi 2 r_{on} C_S)$.

In the transition from phase 1 to phase 2, the noise voltage on capacitor C_S is sampled, leading to noise fold-over.

In phase 2, in addition to the noise contributions from the switches, there is also the noise contribution of the amplifier, filtered by a different RC network:

$$V_{n-C_S}(f) = \frac{v_{n3} + v_{n4} + v_{n-oa}}{1 + jf/f_{p2}} \tag{A.17}$$

where $f_{p2} = 1/(2\pi(2r_{on} + 1/G_M)C_S)$. A charge proportional to the difference of the sampled noise voltages at the end of the two phases is then transferred to the integrating capacitance C_F. It is possible to evaluate the noise power of the difference of the noise voltages in the two phases as:

$$\Delta V_{n-C_S}(f) = V_{n-C_S}(f) - V_{n-C_S}(f) \tag{A.18}$$

$$S_{\Delta V}(f) = \frac{S_{n1} + S_{n2}}{1 + (f/f_{p1})^2} + \frac{S_{n3} + S_{n4} + S_{n-oa}}{1 + (f/f_{p2})^2} \tag{A.19}$$

Under the condition of $r_{on} \ll 1/G_M$ (i.e. the circuit settling time is not influenced by the switch on-resistance), we obtain:

$$P_{\Delta V} = (S_{n1} + S_{n2}) f_{p1} \frac{\pi}{2} + (S_{n3} + S_{n4} + S_{n-oa}) f_{p2} \frac{\pi}{2} = \frac{kT}{C_S}(1 + \gamma) \tag{A.20}$$

The expression of the output noise voltage in phase 1+ is then:

$$V_{n-out}^{(1+)} = V_{n-out}^{(1)} + v_{n-oa}^{(1+)} - v_{n-oa}^{(1)} + \frac{C_S}{C_F} \Delta V_{C_S} \tag{A.21}$$

Rewriting the last equation in the z-domain:

$$V_{n-out}(z) = V_{n-oa}(z) + k \frac{\Delta V_{C_S}}{1 - z^{-1}} \tag{A.22}$$

Dividing this expression for the integrator transfer function, we obtain the expression of the RTI noise voltage:

$$V_{n-RTI}(z) = V_{n-oa}(z) \frac{1 - z^{-1}}{kz^{-1}1} + \frac{\Delta V_{C_S}}{z^{-1}} \tag{A.23}$$

The amplifier noise is multiplied for $(1 - z^{-1})$, that is the operation of the derivative in the z-domain. We will demonstrate in the next paragraph that it is easily negligible. Thus, it is possible to write the expression of the RTI power spectral density in the frequency domain, and from that evaluating the RTI noise power:

$$S_{n-RTI}(f) \simeq S_{\Delta V}(f) \tag{A.24}$$

$$P_{n-RTI} = P_{\Delta V} \simeq \frac{kT}{C_S}(1 + \gamma) \tag{A.25}$$

The RTI noise power is practically the same of the sampling capacitor C_S. It is difficult to go below the limit of kT/C noise, a part from few exceptions [176]; definitively, it is important to minimize the factor γ, optimizing the amplifier topology and sizing. In case of fully-differential implementation, due to the presence of two sampling capacitors, the contribution of sampling noise is exactly doubled.

A.3 High-gain Switched-Capacitor Integrator

In this paragraph, the description of the two-stage, high-gain switched capacitor integrator [102] is provided. The novel integrator is thought to be implemented with inverter-like amplifier in order to work with ultra-low supply voltages. It presents interesting features, as a very high dc gain and the implementation of correlated-double sampling technique, making it appealing for inverter-like designs. Furthermore, having the output always valid (differently from typical switched-capacitor circuit with CDS technique), it can be employed as a continuous-time operational amplifier for feedback

amplifier configurations, if the input signal bandwidth is much lower than the sampling frequency and anti-alias filter is placed before the integrator [103].

As seen for the parasitic-insensitive integrator, the analysis of the ideal behaviour of the circuit is described. Than, the effects of amplifiers' finite dc gain and noise are will be taken into account.

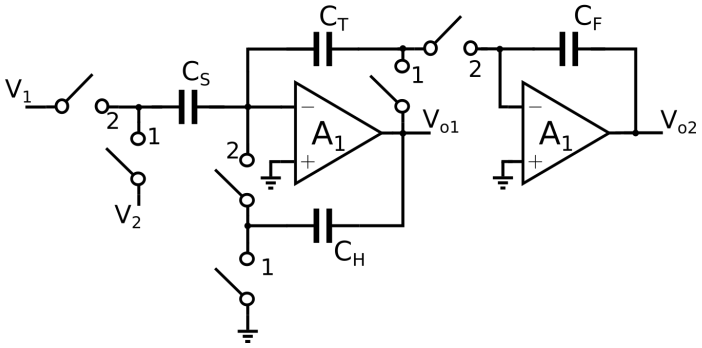


Figure A.9: *Schematic view of the proposed two-stages, high dc gain integrator.*

The study of the circuit behaviour is similar to the one used in the previous section for the parasitic insensitive integrator. It is possible to write the differential voltage on all the capacitors in the two phases depicted in Fig.A.10:

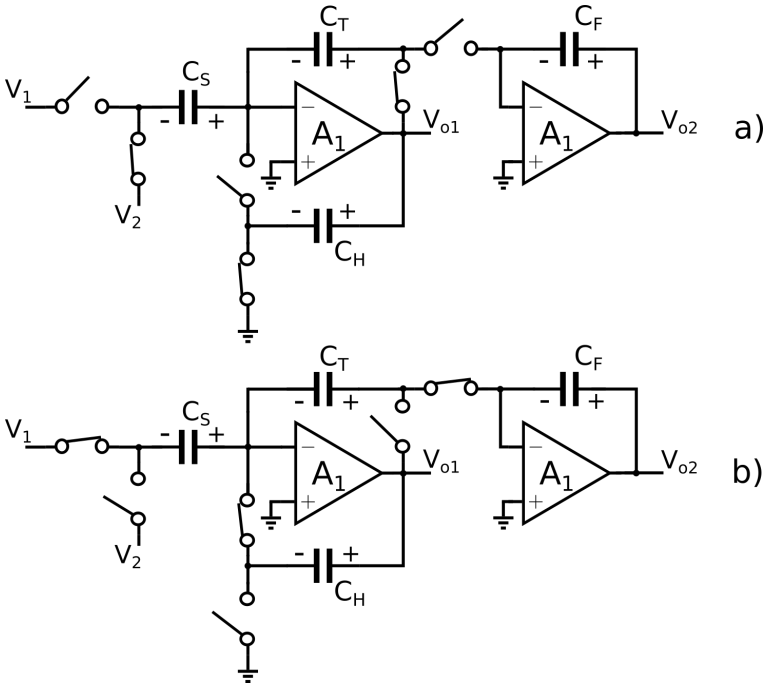


Figure A.10: *Configuration of the proposed integrator in the two phases: a) phase 1, b) phase 2.*

$$\begin{cases} V_{C_S}^{(1)} = V_{i1}^{(1)} - V_2^{(1)} \\ V_{C_T}^{(1)} = V_{o1}^{(1)} - V_{i1}^{(1)} \\ V_{C_H}^{(1)} = V_{o1}^{(1)} \\ V_{C_F}^{(1)} = V_{o2}^{(1)} - V_{i2}^{(1)} \end{cases} \tag{A.26}$$

$$\begin{cases} V_{C_S}^{(2)} = V_{i1}^{(2)} - V_1^{(2)} \\ V_{C_T}^{(2)} = V_{i2}^{(2)} - V_{i1}^{(2)} \\ V_{C_H}^{(2)} = V_{o1}^{(2)} - V_{i1}^{(2)} \\ V_{C_F}^{(2)} = V_{o2}^{(2)} - V_{i2}^{(2)} \end{cases} \tag{A.27}$$

To obtain the expression of the output voltage in phase 2, it is necessary to start analysing the circuit from phase 2- (whose expressions are the easily obtained from A.27). From the charge transfer from C_S to C_T in the transition from phase 2$^-$ to 1, it is possible to evaluate $V_{o1}^{(1)}$:

$$V_{C_T}^{(1)} = V_{C_T}^{(2^-)} + \frac{\Delta Q_{C_T}^{(2^-\to 1)}}{C_T} = V_{C_T}^{(2^-)} + \frac{\Delta Q_{C_S}^{(2^-\to 1)}}{C_T} \tag{A.28}$$

$$\Delta Q_{C_S}^{(2^-\to 1)} = C_S(V_{C_S}^{(1)} - V_{C_S}^{(2^-)}) = C_S(V_1^{(2^-)} - V_2^{(1)} + V_{i1}^{(1)} - V_{i1}^{(2^-)}) \tag{A.29}$$

$$V_{o1}^{(1)} = V_{C_T}^{(1)} + V_{i1}^{(1)} = V_{i2}^{(2^-)} + V_{i1}^{(1)} - V_{i1}^{(2^-)} + \frac{C_S}{C_T}(V_1^{(2^-)} - V_2^{(1)} + V_{i1}^{(1)} - V_{i1}^{(2^-)}) \tag{A.30}$$

To evaluate the expression of the output voltage V_{o2}, the charge transfer from C_T to C_F during the transition from phase 1 to phase 2 is derived:

$$V_{C_F}^{(2)} = V_{C_F}^{(1)} + \frac{\Delta Q_{C_F}^{(1\to 2)}}{C_F} = V_{C_F}^{(1)} + \frac{\Delta Q_{C_T}^{(1\to 2)}}{C_F} \tag{A.31}$$

$$\begin{aligned} \Delta Q_{C_T}^{(1\to 2)} &= C_T(V_{C_T}^{(2)} - V_{C_T}^{(1)}) = C_T[V_{i2}^{(2)} - V_{i2}^{(2^-)} - (V_{i1}^{(2)} - V_{i1}^{(2^-)}) \\ &\quad - \frac{C_S}{C_T}(V_1^{(2^-)} - V_2^{(1)} + V_{i1}^{(1)} - V_{i1}^{2^-})] \end{aligned} \tag{A.32}$$

$$\begin{aligned} V_{o2}^{(2)} &= V_{C_F}^{(2)} + V_{i2}^{(2)} = V_{o2}^{(2^-)} + \frac{C_S}{C_F}(V_2^{(1)} - V_1^{(2^-)}) + \left(1 + \frac{C_T}{C_F}\right)(V_{i2}^{(2)} - V_{i2}^{(2^-)}) \\ &\quad - \frac{C_T}{C_F}(V_{i1}^{(2)} - V_{i1}^{(2^-)}) - \frac{C_S}{C_F}(V_{i1}^{(1)} - V_{i1}^{(2^-)}) \end{aligned} \tag{A.33}$$

It is possible to write the expression of the output in the z domain, neglecting the effect of amplifier finite gain, offset and noise ($V_{i1,2} = 0$):

$$V_{out}(z) = V_{out}(z)z^{-1} + \frac{C_S}{C_F}(V_2 z^{-1/2} - V_1 z^{-1}) \tag{A.34}$$

Indicating with $V_{in}(z) = V_2 z^{1/2} - V_1$, we can write the integrator transfer function in the same form of the ideal one:

$$H(z) = \frac{V_{out}(z)}{V_i n(z)} = \frac{C_S}{C_F}\frac{z^{-1}}{1 - z^{-1}} \tag{A.35}$$

A.3.1 Noise analysis

In order to study the effect of amplifiers' noise on the overall integrator performances, we need to consider the RTI noise $v_{n1,2}$ of each amplifier in the terms $V_{i1,2}$ and replace them in A.33:

$$\begin{aligned} v_{nout}^{(2)} = v_{nout}^{(2^-)} &+ \left(1 + \frac{C_T}{C_F}\right)(v_{n2}^{(2)} - v_{n2}^{(2^-)}) \\ &- \frac{C_T}{C_F}(v_{n1}^{(2)} - v_{n1}^{(2^-)}) - \frac{C_S}{C_F}(v_{n1}^{(1)} - v_{n1}^{(2^-)}) \end{aligned} \tag{A.36}$$

It is now possible to write the expression of the sampled output noise in the z domain:

$$\begin{aligned} v_{nout}(z)(1 - z^{-1}) = &\left(1 + \frac{C_T}{C_F}\right) v_{n2}(z)(1 - z^{-1}) - \frac{C_T}{C_F} v_{n1}(1 - z^{-1})) \\ &- \frac{C_S}{C_F} v_{n1}(z) z^{-1/2}(1 - z^{-1/2}) \end{aligned} \tag{A.37}$$

$$v_{nout}(z) = \left(1 + \frac{C_T}{C_F}\right) v_{n2}(z) - \frac{C_T}{C_F} v_{n1} - \frac{C_S}{C_F} v_{n1}(z) z^{-1/2} \frac{(1 - z^{-1/2})}{1 - z^{-1}} \tag{A.38}$$

With the inverse z-transform, we can write the following expression of the sampled output noise sequence:

$$\begin{aligned} v_{nout}(nT) = &\left(1 + \frac{C_T}{C_F}\right) v_{n2}(nT) - \frac{C_T}{C_F} v_{n1}(nT) \\ &- \frac{C_S}{C_F} \sum_{k}^{n} [v_{n1}(kT - T/2) - v_{n1}(kT - T)] \end{aligned} \tag{A.39}$$

where it is possible recognize two different kind of contributions: the first two terms are the sampled noise of A_1 and A_2 multiplied for proper capacitive ratios; the last term is given by the accumulation of the differences of two noise samples of A1. As a result, a part from the CDS mechanism, the time-discrete integration of A1 noise implies that

this is the leading contribution of the integrator noise. It is interesting also to evaluate the expression of the RTI noise:

$$\begin{aligned} v_{nRTI}(z) = &\left(1+\frac{C_T}{C_F}\right) v_{n2}(z) z(1-z^{-1}) - \frac{C_T}{C_F} v_{n1}(z) z(1-z^{-1}) \\ &- \frac{C_S}{C_F} v_{n1}(z)(1-z^{-1/2}) z^{1/2} \end{aligned} \tag{A.40}$$

$$\begin{aligned} v_{nRTI}(nT) = &\left(1+\frac{C_T}{C_F}\right)(v_{n2}(nT+T) - v_{n2}(nT+T)) \\ &- \frac{C_T}{C_F}(v_{n1}(nT+T) - v_{n1}(nT+T)) - \frac{C_S}{C_F}(v_{n1}(kT+T/2) - v_{n1}(kT)) \end{aligned} \tag{A.41}$$

Referring to the input, it is still possible to recognize the two different kind of contributions. In a similar way as discussed in [15], we can consider the two fictitious transfer functions that filters the time-continuous noise $v_{n1}(t)$ and $v_{n2}(t)$, before the sampling operation:

$$v_{nRTI}(f) = \left(1+\frac{C_T}{C_F}\right) v_{n2}(f) H_T(f) - \frac{C_T}{C_F} v_{n1}(f) H_T(f) - \frac{C_S}{C_F} v_{n1}(f) H_{T/2}(f) \tag{A.42}$$

$$H_T(f) = 2jsin(\pi f T_{ck}) e^{+j\pi f T ck} \tag{A.43}$$

$$H_{T/2}(f) = 2jsin\left(\frac{\pi}{2} f T_{ck}\right) e^{+j\frac{\pi}{2} f/f_{ck}} \tag{A.44}$$

$|H_{T/2}(f)|^2$ is periodic with period $2T_{ck}$ (where T_{ck} is the inverse of the clock frequency) and the sum of the odd and even harmonics give a constant contribution [15]. $|H_T(f)|^2$ is periodic of period T_{ck} and its contribution is noticeable only for $f \simeq f_{ck}/2$. It is easy to verify that the contribution related to $H_T(f)$ is negligible. Then, the RTI PSD of the integrator results in:

$$S_{RTI}(f) \simeq 2 S_{BB1} B_{eq-n1} \frac{2}{f_{ck}} = 2\frac{kT}{C_S}\gamma\frac{2}{f_{ck}} \tag{A.45}$$

Basically, the RTI PSD has the general expression of the KT/C noise from the sampling operation of the capacitor C_S, considering also the factor γ, that is the excess noise of the first amplifier. The noise contribution of the second amplifier is negligible, as well as the flicker noise of both amplifiers, thanks to the CDS operations.

A.3.2 Finite dc gain and offset

Performing detail calculations about amplifier finite dc gain A_1 and A_2[1] is very tedious and we do not have reach so far a close expression in the z domain as equation A.13 seen

[1] With A_1 and A_2 we will refer to both the amplifiers and their dc gain.

for the PI integrator. Basically, it would be sufficient to replace V_i with the expression which takes into account the finite gain of the amplifier (as A.46, which takes into account also the amplifier offset). Here, we propose a different approach that allows an easily evaluation of the finite dc gain and RTI offset of the integrator, as a function of the amplifiers' dc gain.

The general expression of the amplifier output voltage, taking into account both finite dc gain and offset, is:

$$V_o = -A(V_i + V_{io}) \tag{A.46}$$

Analysing the integrator behaviour for $z \to 1$ (dc behaviour) and constant inputs V_2 and V_1, due to the finite gain of the amplifiers we will reach a point where C_S do not transfer charge to C_T any more, and consequently C_T do not transfer charge to C_F and the output does not change. C_H as well is not subjected to voltage variations between the two different clock phases. Under these assumptions, it is easy to find the following expressions:

$$V_{C_S}^{(2)} - V_{C_S}^{(1)} = 0 \to V_2 - V_1 = V_{i1}^{(1)} - V_{i1}^{(2)} \tag{A.47}$$

$$V_{C_H}^{(2)} - V_{C_H}^{(1)} = 0 \to V_{o1}^{(2)} - V_{o1}^{(1)} = V_{i1}^{(2)} \tag{A.48}$$

$$V_{C_T}^{(2)} - V_{C_T}^{(1)} = 0 \to V_{i2}^{(2)} - V_{i1}^{(2)} = V_{o1}^{(1)} - V_{i1}^{(1)} \tag{A.49}$$

From equations A.47 and A.48 it is possible to write:

$$V_{i1}^{(2)} = -A_1(V_{i1}^{(2)} - V_{i1}^{(1)}) = A_1(V_2 - V_1) \tag{A.50}$$

$$V_{o1}^{(1)} = V_{o1}^{(2)} - V_{i1}^{(2)} = -A_1(V_{i1}^{(2)} + V_{io1}) - V_{i1}^{(2)} = -(A_1^2 + A_1)(V_2 - V_1) - A_1 V_{io1} \tag{A.51}$$

Replacing the expressions of $V_{o1}^{(1)}$ and $V_{i1}^{(2)}$ in A.49:

$$V_{i2}^{(2)} = V_{i1}^{(2)} - V_{i1}^{(1)} + V_{o1}^{(1)} = -(A_1^2 + A_1 + 1)(V_2 - V_1) - A_1 V_{io1} \tag{A.52}$$

$$V_{o2}^{(2)} = -A_2(V_{i2}^{(2)} + V_{io2}) = A_2(A_1^2 + A_1 + A_1)(V_2 - V_1) + A_1 A_2 V_{io1} - A_2 V_{io2} \tag{A.53}$$

From A.53 it is possible to state that the finite dc gain of the integrator is proportional to $A_2 A_1^2$. If we employ two amplifiers with the same dc gain $A_1 = A_2 = A_0$, the integrator finite dc gain is proportional to A_0^3. For this reason, as proposed in [102], this topology matches perfectly inverter-like design for low and ultra-low voltage design. In fact, even if the single amplifier shows a dc gain of few tens, the overall dc gain is above several thousands, that is enough large for many applications.

Concerning the referred-to-input offset, it is possible to write:

$$V_{io-RTI} = \frac{V_{io1} A_1 A_2 - V_{io2} A_2}{A_1^2 A_2} = \frac{V_{io1}}{A_1} - \frac{V_{io2}}{A_1 A_2} \tag{A.54}$$

Due to the dc finite gain, a residual offset is present, despite of the CDS mechanism above described. The offset contribution of the second amplifier results negligible compared to the contribution of the first amplifier. In inverter-like designs where the virtual ground of the circuit is V_{INV} and it is generated by means of a third inverter, the offset V_{io1} consists, actually, in the mismatch between V_{INV1} and V_{INV3} (the inversion voltage of inverter A_1 and of the additional reference inverter). As a result, minimum size inverters with low finite gain may lead to noticeable residual offset. It is easy to extend these considerations also for flicker noise: a residual flicker noise contribution from A_1 and from the reference inverter will not be perfectly rejected, due to the finite gain of A_1. The thermal noise power increase due to this phenomenon is typically negligible compared to the contribution previously evaluated.

Conclusion

This work aimed to provide some important considerations about the design of different Analog-to-Digital Converters, targeted for highly-specific applications. The full-custom design of these blocks, however, may inspire more general considerations about the analog-mixed design concerning high-resolution and high-accuracy acquisition interfaces, ultra-low voltage systems or extreme environmental conditions, as it could be cryogenic temperatures.

A general overview about the main characteristics of analog-to-digital converters helped to dive into the technical problems related to full-custom designs of these blocks, optimized for high-performance, specific applications. Among the several converter architectures, Δ-Σ ADCs have been deeply discussed, due to their importance in data acquisition systems for sensor interfacing. Two different converters have been developed: (i) a Δ-Σ converter compatible with conventional supply voltages, targeting high accuracy and high resolution for digitizing input signal with bandwidth included in the range from dc to few kilohertz (typical of temperature, inertial or gas sensors); (ii) a Δ-Σ converter designed for ultra-low supply voltages, with less strict specifications in terms of resolution but carefully designed for reducing the power consumption as much as possible. Measurements on the silicon prototypes realized in UMC $0.18\ \mu\mathrm{m}$ process confirm the effectiveness of the novel techniques employed and give useful information for future developments and improvements. Finally, the design of a cryo-CMOS SAR converter for quantum computing readout interface has been presented. Great attention has been spent on the contextualization of this project, highlighting the fascinating challenges involved with this new field of information engineering. More precisely, the critical issues related to the CMOS design for cryogenic applications have been investigated, focusing on their impact on the design of an high-speed analog-to-digital converter. Electrical simulations in Cadence environment showed the performances of the proposed converter, designed with TSMC $40\ \mathrm{nm}$ CMOS process.

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