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DESIGN AND EXPERIMENTAL VERIFICATION OF IC TECHNIQUES FOR HARSH ENVIRONMENTS: AUTOMOTIVE, AEROSPACE AND HEP CASE STUDIES

DOCTORAL THESIS

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"I am always doing what I cannot do yet,
in order to learn how to do it."
Vincent Van Gogh

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Summary

Today's incredible growth of the consumer electronics market is flanked by the pervasive diffusion of electronic devices in harsh environments. In these contexts, Integrated Circuits (ICs) have to withstand rugged conditions that affect the proper functioning of silicon devices. Different environments can be characterized by one or more harsh conditions that degrade the performances of the electronic devices. Although today's automotive and aerospace worlds are two of the most difficult environments where ICs can operate, the next generation of space and terrestrial vehicles will be ever-more managed by electronic systems. Indeed, they will be filled on a side by high-power systems used for electrical motors, traction, braking, and other functions, and on the other side by extremely sensitive sensors and circuits capable of detecting the minimal physical variation. This increment in the number of onboard electronic devices will require ever-more electric energy stored in batteries and ever-better management of them.

Today's onboard power management trend shows the coexistence of multi-levels voltage domains, such as 48 V, 12 V, and 5 V, to supply different electronic sub-systems. For these reasons, in this thesis work, techniques to withstand issues deriving from multi-voltage domains systems are proposed in an inductorless DC/DC converter design framework. The integrated DC/DC converter, designed in 0.35 µm HV technology, is able to convert a wide range of input voltages, from 6 V to 60 V, in two output points of loads, 5 V and 1.65 V, for sensors supply. At the best of the author's knowledge, this is the first silicon integrated inductorless DC/DC converter, in literature or market, able to convert such a wide input range. This wide range is managed using a multi-stage cascade architecture with reconfigurable switched capacitors stages and high-voltage MOSFETs. In addition, in response to strong fault-management requirements of safety-critical systems, an innovative and integrable fault-tolerant technique is proposed in this thesis. It, using the switched capacitors technique, is able to insulate the low-voltage loads from high-voltage inputs also in case of failures, avoiding the state-of-the-art use of cumbersome transformers.

The IC DC/DC converter was implemented in 6*6 mm^2 chip, and in response to the growing requirement of ever-more integration, the measurement campaign of the in-

ductorless DC/DC converter was focused on the comparison between the performances extracted from a classical 2D configuration, with external passives placed side-by-side with the IC, and an innovative 3D assembled structure, with silicon capacitors stacked on the chip of the DC/DC converter. The electrical measurements showed the feasible use of the compact 3D structure for area reduction purposes, maintaining nearly the same 2D conversion performances.

In order to verify compliance with the space environment, the designed IC DC/DC converter was exposed to cumulative dose and heavy-ions radiation tests. The first test, performed with X-rays exposure, showed a radiation-tolerant level up to 43 krad, highlighting the feasible use of the DC/DC converter for the Heart-Moon travels. The second test, used to generate random faults in the converter control strategy, showed the reliability of the insulation stage to prevent high-voltages damaging of the supplied loads.

Since the ever-growing requirement of compact systems, the electromagnetic interaction between different devices is one of the hardest challenges in today's electronic design. Being the switching DC/DC converter one of the main generators of electromagnetic disturbances, some techniques to mitigate the generation of these disturbances have been adopted, in this thesis, at the ICs design level. In particular, techniques such as input filter and soft-start have been implemented to reduce conducted interference, instead low-switching frequency, inductorless architecture and spread spectrum techniques have been used to mitigate radiated interference.

On the radiation side, the high-energy experiments, used by the particle physics for the verification of new theories, are characterized by radiation levels nearly three orders higher than that used for standard space applications. This extremely harsh condition heavily stresses the performances of state-of-the-art electronic devices used for particle detection. In order to guarantee the correct functioning of ICs when they operate in this challenging environment, in this thesis some Radiation Hardened By Design (RHBD) techniques to mitigate the radiation effects on silicon ICs are applied, such as current mode logic, double long MOSFETs and enclosed layout transistors. These RHBD techniques have been then used for the design of high-speed electro-optical modulator drivers in 65 nm CMOS technology. These multi-stage drivers, in addition to the rad-hard solutions, implement buffer chain and inductive peaking techniques for bandwidth extension. The drivers, realized in a 1*1 mm^2 chip, were directly bonded on a carrier board and electrically tested, showing 5 Gbps data rate performances. The electron-optical modulators targeted in this work are the Mach Zehnder Modulator and the Ring Resonator, both realized on silicon-photonic technology. These modulators have shown higher radiation hardness property than the classical VCSEL (Vertical Cavity Surface Emitting Lasers), typically used on standard applications. The system-level test, performed bonding the silicon drivers chip with the silicon-photonics modulators chip through aluminum bonding wires, confirmed the achievement of a data rate up to 5 Gbps. In response to the radiation-hard requirement, the drivers chip was exposed to X-ray, showing its ability to work up to 800 Mrad, level of radiation that, today, no electronic device in literature or industry is able to reach.

Sommario

L'odierna incredibile crescita dell'elettronica di consumo è affiancata dalla pervasiva diffusione dei dispositivi elettronici negli ambienti più ostili. In questi contesti, i Circuiti Integrati (ICs) devono fronteggiare condizioni avverse che influiscono sul corretto funzionamento dei dispositivi in silicio. Ambienti differenti possono essere caratterizzati da una o più condizioni che degradano le prestazioni dei dispositivi. Nonostante gli attuali mondi automotive e aerospace siano due degli ambienti più ostili dove i ICs possono operare, la prossima generazione di veicoli terrestri e spaziali sarà sempre maggiormente gestita da sistemi elettronici. I veicoli saranno costellati, da un lato, da sistemi ad elevata potenza per la gestione dei motori elettrici, usati per la trazione, la frenata ed altre funzioni, e dall'altro lato, da sensori e circuiti estremamente sensibili in grado di rilevare la più piccola variazione fisica. L'incredibile numero di dispositivi elettronici a bordo richiederà una sempre maggiore quantità di energia elettrica immagazzinata nelle batterie e una sua sempre migliore gestione. L'attuale tendenza nella gestione della potenza di bordo mostra una coesistenza di diversi domini di tensione per l'alimentazione dei diversi sottosistemi elettronici, come 48 V, 12 V e 5 V. Per queste ragioni, in questo lavoro di tesi, alcune tecniche per affrontare gli effetti derivati da sistemi costituiti da domini multi-tensione sono proposti insieme alla progettazione di un convertitore DC/DC senza induttore. Il convertitore DC/DC, progettato nella tecnologia 0.35 µm HV, è in grado di convertire un ampio range di tensioni in ingresso, da 6 V a 60 V, in due punti di carico, 5 V e 1.65 V, per l'alimentazione di sensori. Dalla conoscenza dell'autore della letteratura e del mercato, questo è il primo convertitore DC/DC senza induttore in grado di convertire un range di ingresso così ampio. Questo ampio range è gestito usando un'architettura multi-stadio con stadi a condensatori commutati riconfigurabili e MOSFETs ad alta tensione.
In risposta ai pressanti requisiti per la gestione dell'errore in sistemi critici, un'innovativa e integrabile tecnica tollerante ai faults è proposta in questa tesi. Essa, usando la tecnica dei condensatori commutati, evita l'utilizzo degli ingombranti trasformatori usati nello stato dell'arte. Il convertitore è stato realizzato in un chip 6*6 mm^2, e in risposta alla crescente richiesta di sempre maggiore integrazione, la campagna di misura del convertitore DC/DC si è focalizzata sul confronto tra le prestazioni ottenute da una

classica configurazione 2D, con i passivi situati a lato del chip, ed un'innovativa struttura 3D, con condensatori in silicio impilati sopra il chip. Le misure elettriche hanno mostrato la fattibilità dell'utilizzo della struttura 3D al fine di ridurre l'area occupata, mantenendo quasi le stesse prestazioni della configurazione 2D.
Per la verifica della compatibilità con l'ambiente spaziale del IC progettato, il convertitore è stato esposto a test di radiazione di dose accumulata e di ioni pesanti. Il primo test, eseguito con esposizione a raggi X, ha mostrato una tolleranza del convertitore DC/DC fino ad un livello di 43 krad, evidenziando la possibilità di un suo impiego per viaggi Terra-Luna. Il secondo test, usato per generare fallimenti casuali nella strategia di controllo del convertitore, ha dimostrato l'affidabilità dello stadio isolatore nella prevenzione dei danneggiamenti dei dispositivi alimentati dal convertitore. Data la sempre crescente richiesta di sistemi compatti, l'interazione elettromagnetica tra dispositivi differenti è una delle maggiori sfide nell'odierna progettazione elettronica. Essendo il convertitore DC/DC switching uno dei principali generatori di disturbi elettromagnetici, alcune tecniche per mitigare la generazione di questi disturbi sono state adottate in questa tesi, al livello di progettazione del chip. In particolare, tecniche come l'adozione di un filtro d'ingresso e il soft-start sono state implementate per ridurre le interferenze condotte, mentre techniche come una bassa frequenza di switching, un'architettura senza induttore e l'allargamento dello spettro sono state usate per la mitigazione delle interferenze irradiate.
Sul fronte radiazioni, gli esperimenti ad alta energia, usati nella fisica particellare per la verifica di nuove teorie, sono caratterizzati da livelli di radiazione quasi tre ordini di grandezza superi rispetto alle applicazioni spaziali standard. Queste estreme condizioni stressano pesantemente le prestazioni dei dispositivi elettronici dello stato dell'arte usati per la rilevazione delle particelle. Per garantire la corretta operazione dei ICs operanti in questo ambiente, in questa tesi sono state sviluppate alcune tecniche Radiation Hardened By Design (RHBD) per la mitigazione degli effetti sui ICs dovuti alle radiazioni, come la logica current-mode, una lunghezza dei MOSFETs doppia e l'enclosed layout dei transistors. Queste tecniche RHBD sono state utilizzate per la progettazione di drivers per modulatori elettro-ottici ad elevata velocità in tecnologia CMOS 65 nm. I driver multistadio, in aggiunta alle soluzioni per fronteggiare le radiazioni, implementano tecniche di buffer chain e inductive peaking per l'estensione della banda. I driver, realizzati in un chip 1*1 mm^2, sono stati connessi direttamente su una board e testati elettricamente, mostrando buone prestazioni fino a 5 Gbps. I modulatori elettro-ottici usati in questo lavoro sono il modulatore Mach Zehnder ed il Ring Resonator realizzati in tecnologia silicon-photonic, i quali hanno mostrato maggiori proprietà di resistenza alle radiazioni rispetto ai classici VCSEL (Vertical Cavity Surface Emitting Lasers), tipicamente utilizzati in applicazioni standard. I test a livello di sistema, eseguiti connettendo il chip in silicio dei drivers ed il chip in silicon-photonics dei modulatori attraverso bonds in alluminio, confermano il raggiungimento di una velocità di trasmissione di 5 Gbps. In risposta al requisito di tolleranza alle radiazioni, il chip dei drivers è stato esposto a raggi X, mostrando la sua abilità ad operare fino a 800 Mrad, livello di radiazione che oggi nessun altro dispositivo elettronico presente in letteratura o industria è in grado di raggiungere.

List of publications

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Contents

1 Introduction **1**
- 1.1 Open Challenges on ICs Operating in Harsh Environments 1
- 1.2 Thesis structure 3

2 IC Design Challenge in Automotive, Aerospace and HEP Environments **4**
- 2.1 Automotive 4
- 2.2 Aerospace 6
- 2.3 High Energy Physics 8

3 High-Voltage and Fault Mitigation Design Techniques **10**
- 3.1 Switched Capacitor Converters 10
- 3.2 Converter Architecture 12
- 3.3 Circuit/Transistor-Level Converter Sizing 14
  - 3.3.1 Eqivalent Output Resistance of each SC stage 14
- 3.4 Switches typologies 16
- 3.5 First DC/DC converter stage 20
- 3.6 Second DC/DC converter stage 24
- 3.7 Insulator stage 25
- 3.8 Linear Regulators 28
- 3.9 Gate drivers 28
- 3.10 Control Unit 29
- 3.11 IC Layout and Post-Layout Simulations 30

4 High-Voltage and Fault Mitigation Design Techniques Verification **33**
- 4.1 Testing Boards Implementations 34
- 4.2 Electrical Measurements 35
  - 4.2.1 Line Regulation 36
  - 4.2.2 Load Regulation 36
  - 4.2.3 Efficiency 37
  - 4.2.4 Power Supply Rejection Ratio 39
- 4.3 Insulator Test 41

4.3.1 Overvoltage Fault Test . . . 42
4.3.2 Single Event Effect Fault Test . . . 43
4.3.3 Total Ionizing Dose Effects . . . 45
4.4 Thermal Measurements . . . 46
4.4.1 Performances at Different Environment Temperatures . . . 46
4.4.2 Thermal Profile of the Converter . . . 46
4.5 Electrical Comparison to State-of-the-art . . . 49

5 Electromagnetic Interference reduction techniques, Development and Verification 51
5.1 Front-end and DC/DC Converter Models . . . 51
5.2 Design of an Anti-conducted EMI Filter . . . 52
5.2.1 Classic Approach . . . 53
5.2.2 EMI Filter Design . . . 53
5.2.3 Filter Effects on the Converter System . . . 58
5.3 Experimental Measurements of Conducted Electromagnetic Emissions . 62
5.4 Effects of SKIP Algorithm on the Conducted EMI . . . 63
5.5 Measurements of Radiated Interference . . . 65
5.5.1 EMC Standard Test . . . 68
5.6 Soft-Start Techniques to Reduce Peak Currents . . . 68
5.7 Electromagnetic Interface Comparison to State-of-the-art . . . 69

6 TID and SEU Mitigation Techniques 72
6.1 Total Ionizing Dose Effects . . . 73
6.2 IC techniques to face TID effects . . . 74
6.2.1 Enclosed Layout Transistors . . . 75
6.2.2 Minimum Length . . . 75
6.2.3 CMOS vs. CML approach . . . 76
6.2.4 1 Grad (SiO_2) MOSFET models development . . . 78
6.3 Single Event Effects . . . 80
6.4 IC techniques to face SEE effects . . . 81
6.4.1 CMOS-DFF and CML-DFF SEE Comparison . . . 82

7 High-speed Electro-Optical Modulator Drivers Design 87
7.1 MZM and RR . . . 87
7.2 Drivers Design . . . 89
7.2.1 Output stages design . . . 90
7.2.2 Pre-driver stages design . . . 91
7.2.3 Receiver . . . 92
7.2.4 Power Consumption and Power Supply Rejection Ratio . . . 92
7.2.5 SEE Simulations . . . 93
7.2.6 Chip Layout . . . 94
7.3 Chip-Board Co-Simulations . . . 95
7.4 Drivers Measurements . . . 97
7.4.1 Frequency Domain Measurements . . . 97
7.4.2 Time Domain measurements . . . 98
7.4.3 TID and SEE Measurements . . . 102
7.5 State-of-the-art Comparison . . . 106

8 Conclusions 107

Bibliography 110

CHAPTER 1

Introduction

1.1 Open Challenges on ICs Operating in Harsh Environments

In the last fifty years, electronics have pervaded every aspect of our lives. Its uncontrollable diffusion has involved every space of our daily life. From smartphones to smartwatches, from smart-televisions to smart-kitchens, from electric-bikes to electric-skateboards, every device around our life is or could be equipped with some electronic "intelligence". Consumer electronics has been, unquestionably, one of the most flourishing markets of the last years. But electronics is also making inroads in harsh environments: those environments that with their rugged characteristics, could reduce the lifetime of electronic devices. While many devices on the market are not designed for harsh environments, many others must operate effectively while being jostled, dampened, heated, irradiated, and more.
A lot of rugged conditions could be considered harsh for human life, but what environments should be labeled "harsh" for electronic Integrated Circuits (ICs) systems? These environments can be identified for the nature of the rugged physics phenomenons at which they are exposed:

- *Chemical Attack*: the materials used in the manufacture of ICs, such as silicon for dies, plastic or ceramic compounds for packages and metals for electrical connections, can be attacked by special chemicals in form of gaseous vapor and liquid. A classic example is the vulnerability of the wide diffused plastic packages to moisture. Indeed, thanks to the porosity of plastic mold, it can easily diffuse into the package, where, in case of temperature excursion, it can create delaminations, crack and popcorn effects (so-called for its classic 'pop' sound). These unwanted effects could directly damage the package leadframe or create wide access used by corrosive chemical elements to damage the internal die. For this reason, the ICs

are sold in moisture-proof packs and, if they are stored for an important period, they should be treated with decontamination processes [1]. Even more aggressive are the exhausts fume of combustion engines or the corrosive fume of lead-acid batteries that ICs devices have to face when operating in automotive environments.

- *Mechanical Stresses and Vibration*: even mechanical stress could seriously damage ICs. Being the ICs micro-systems composed of different materials, as a consequence of temperature or pressure changing, several stresses can appear. The bonding wires or solder bumps, used to connect the ICs to the outside world, are extremely sensitive to stress, which can reduce their conductive property and even break them under fatigue. Indeed, 32.3% of the failure of the ICs encapsulation is due to bonding faults and 15.5% to die cracking [2, 3]. The MEMSs (Micro Electron-Mechanical Systems), typically used as sensors for the revelation of accelerations, pressures, and angles, are especially sensitive to vibration and can experience damage under strong vibration and impact stresses.

- *Electromagnetic Disturbs*: since the advent of electronics, the main trend, towards the development of new technologies, has been the ever-more increasing integration. It started with the integration of as many transistors as possible on the same chip and it is followed with the integration of as many heterogeneous systems as possible in the smallest area. Complex systems integrated into an incredibly small area influence each other, creating unwanted system behaviors. The main physical interactions, between these systems, are due to electromagnetic fields, whose confinement in a limited area is extremely challenging. Therefore, this ever-increasing integration leads ICs to have to work surrounded by strong variable electromagnetic fields, which can induce voltage variations in some nodes of electrical circuits, altering the system functionality or disturbing the radio communication between transceivers. In order to limits these heavy disturbs, the European Community has released the CISPR standard [4]. It imposes strict limits on the maximum conducted and radiated interference emissions of each device, diversifying the limits value for residential, industrial, automotive, research and lightning environments. The difficulty to confine the electromagnetic disturbs and the strong requirements imposed by CISPR laws pave the way to new design techniques that go beyond the electrical ICs design. Some of these techniques are analyzed in this thesis in Chapter 5.

- *High-Temperature Environments*: since ICs are manufactured using high-energy processes, they are also susceptible to high-energy. Indeed, running an IC at high junction temperatures will degrade its working life. The rapid thermal changes, as previously reported, are also the main responsible for mechanical stress generation and its negative consequences. The temperature range, in which the IC device has to work, is one of the classical discriminators between consumer devices and ICs designed for harsh environments. Indeed, today's de facto temperature range for consumer standard is from 0 °C to 70 °C while the industrial standard constraint is from -40 °C to 125 °C, making challenging the ICs design [5].

- *Radiation and Ions Exposition*: radiation exposure and ions interactions heavily affect the ICs performance when they are in sufficient quantity and with enough

energy to interact with the silicon material. These interactions can reduce the performance of analog circuits and cause data loss in digital systems. The continuous exploration of new planets and deep space poses new challenges in radiation hardness electronics. Indeed, the Total Ionizing Dose (TID) level required in the space missions has increased from a few hundred krad to 1 Mrad in the last few years [6]. Radiation levels are even more demanding in the field of physics experiments, where the discoveries of new properties of matter require the use of ever-greater energies. The same discoveries and technologies carried out in physics experiments are then applied in medical physics, paving the way for new illness treatments. Therefore, the growing demand for higher radiation hardness levels opens the research for new techniques for radiation-tolerant systems, some of which are discussed in Chapter 6.

The design of ICs is incredibly demanding for the nature of the interaction between harsh conditions and the electrical world. Most workbenches are temperature controlled, static-free, dry and radiation-proof areas, but the real world is not as forgiving. It is filled with harsh conditions that make challenging the proper operation of ICs. Depending on the harsh application, the ICs designer has to address one or more of the previous rugged characteristics.

1.2 Thesis structure

In this thesis work, some techniques to improve the performances of ICs operating in harsh environments are developed. In particular, these techniques aim to increase the hardness and reliability of ICs operating in the automotive, aerospace and HEP (High Energy Physics) environments. In Chapter 2 the main challenges in today's Automotive, Space and HEP environments are reported, focusing on the effort paid by the research to address them.
In response to today's challenges, introduced in Chapter 2, Chapter 3 deals with the design of an inductorless DC/DC converter compliant with the automotive world, focusing on the development of high and low voltage compatibility techniques and their fault-tolerant solutions. This IC device and its implemented techniques are then experimentally verified with an accurate measurement campaign, reported in Chapter 4, with electrical and thermal results. Considering the strategic importance of the electromagnetic compatibility and its role in the interaction between ever-more integrate systems, the techniques developed to keep under control the electromagnetic emission end their verification are reported in the dedicated Chapter 5.
The continuous research of new physics theories requires extremely challenging verification experiments, which put under intensive stress today's state-of-the-art technologies, as reported in Chapter 2. In this framework, in Chapter 6 some ICs design techniques for enabling silicon technology to work in an extremely irradiated environment are analyzed. These techniques are then used in the design of the first 800 Mrad tolerant chip, whose design and tests are reported in Chapter 7. The conclusions on the developed techniques to sustain the functionality and the reliability of ICs operating in such hostile conditions are drawn in Chapter 8.

CHAPTER 2

IC Design Challenge in Automotive, Aerospace and HEP Environments

2.1 Automotive

Today, the automotive industry is a fast-growing market no longer driven by mechanical or hydraulic onboard systems improvements, but by the development of new safety and infotainment functions integrated into a vehicle. A quote from Daimler-Chrysler executives says that more than 80% of innovation in the automotive domain concerns electronic components [7]. In the last fifty years, the number of electronic devices and control units in the automotive environment has steadily increased, and today, hundreds of different ECUs can be found in a modern vehicle, each one specialized to provide a different task [8, 9]. This has led to the need to develop automotive-specific ICs, which have to operate in one of the harshest environments, being characterized by corrosive chemical species, strong vibrations, heavy electromagnetic disturbs and wide temperature swings, which have already been summarized in the Chapter 1. The pervasive diffusion of electronics in vehicles is confirmed by the 2020 market forecasts, where the 50% of the vehicle cost is estimated to be due to electronic devices [10]. According to current European regulations, since 2015, a target CO_2 emission of 130 g/km is required to carmakers. This threshold is even decreased to 95 g/km by 2020 [11]. Which corresponds to fuel consumption of around 4.1 l/100 km of petrol or 3.6 l/100 km of diesel. If the average CO_2 emissions of a manufacturer's fleet exceed its target in a given year, the manufacturer has to pay an excess emissions premium for each car registered. Therefore, an increased level of electrification in cars, towards fully electric vehicles (EVs), is needed to meet strict pollution limits.
In hybrid and electric vehicles, micro/mild power applications have appeared, like start-and-stop, regenerative braking and torque assist. These systems repeatedly stress the

onboard electrical systems with load dumps and transients each time that they are activated. For instance, the start-and-stop system, implemented in engine vehicles to increase gas mileage, shutting the engine off at stop signs and then restarting it, within a fraction of a second when the driver steps on the gas pedal, strong stresses the vehicle power bus in stop-and-go traffic. Therefore, even if, in principle, the vehicle is battery powered and thus has a stable and quiet DC source, the reality is quite different. The basic DC rail of the car is noisy, with large and sudden drops when starting the car (cold-cranking) which can drop the rail to a few voltages. At the other extreme, the rail can spike when loads are suddenly removed (called “load dump”) causing transients as high as 60 V.

In response to the ever-higher electrical power needed onboard of vehicles for the supply of the growing electrical systems and the ever-lower vehicle weight for fuel-saving, the automotive systems are migrating toward the 48 V DC power bus standard. After the first revolution of the automotive electrical bus, in 1965, when the power net doubled from 6 V to 12 V [12], today, the voltage level is further increasing from 12 V up to 48 V [13–15], to achieve the onboard power increment of factor four with equal current levels. For instance, the start-and-stop system, already used in 12 V vehicles, requires a power level up to 2 kW, which corresponds to 166 A and 90 mm^2 cable area. Using a 48 V DC power bus the current level is reduced to 41.5 A and the cable area is reduced to 25 mm^2. Therefore, the weight, space occupation, and cost of the onboard wiring system is reduced moving from 12 V to 48 V DC power bus [16, 17]. At the state-of-art, the progression towards the 48 V is characterized by the coexistence of the two voltage domains. Indeed, the major automobile manufacturers including BMW, Daimler, and VW are implementing a two voltage level network standard, inside the same vehicle [13]. Low power loads such as sensors, memories, processors, analog front-ends (requiring regulated voltages of few Volt, and current levels of few hundreds of mA) are typically supplied starting from the main 48 V power source after many conversion steps, each implemented using discrete and inductor-based DC/DC converters. For example, a first 48 V to 12 V unit is followed by another 12 V to 5 V unit, and finally, a dedicated point-of-load linear converter is used for each of the regulated voltages. Such an approach leads to cumbersome and costly conversion systems. On the contrary, an integrated solution could ensure reduced size and weight, and low cost in large volume markets.

Since the electronics on vehicles are widely used to control safety-critical systems, like braking and steering systems (e.g. X-by-wire systems), their devices have to guarantee the highest quality level and a "zero defect" rate during all the lifetime of those safety-related systems. The fault-tolerant protections have to be integrated into each device. These are typically provided with triple redundancy, spatial or temporal, or with error detection ed correction code in case of data transmissions [18]. For DC/DC switching converter, the fault-tolerant characteristic is guaranteed by the use of galvanic coupling in transformers. In the optic of all integrated DC/DC converter in a single IC, the use of these elements should be avoided, for their difficult integration property. It is for this reason that in Chapter 3 an innovative insulation solution is proposed as technique to make DC/DC converters fault-tolerant.

The ever increasing demand for new functions in a vehicle is making the space-saving a fundamental constraint for the design of future applications. In this direction, the elec-

tronic components are ever-more placed one side-to-side to the other, leading to electromagnetic compatibility problems. One of the most common and most electromagnetic noisy devices is the DC/DC switching converter. These converters are distributed in all the vehicles to efficiently provide the supply voltage to all the electric systems, starting from the main power bus (e.g. 12 V, 36 V, 48 V). Since their onboard extensive use and their generation of electromagnetic noise, the design of these DC/DC converters continues to be one of the challenges of today's electronics [19–22]. For these reasons some techniques for electromagnetic noise mitigation, in DC/DC integrated converters, are proposed in Chapter 5.
The ever-pressing request for integration is leading to new challenging technology solutions. The design of ICs, which is by its nature a planar technology, is evolving in a three-dimensional solution [23]. One of the most feasible 3D solutions is the stacking of more ICs one on the other, using interposer layers, as insulating layers, and Through Silicon Vias (TSV), as electrical conducting elements.
In this framework was born the ATHENIS3D FP7 EU project (Automotive Tested High-voltage and Embedded Non-volatile Integrated SoC platform with 3D technology) that partially founded this thesis work. It aims at providing new enabling technologies for high-voltage and high-temperature applications, tested for power systems of new hybrid/electrical vehicles. Innovation is exploited at the process/device level (3D chip stacking, wafer-level packaging, trench capacitors integrated into the interposer) and circuit-level (inductorless high-voltage DC-DC converter, high-temperature System-on-Chip platform) [24].
To this aim, this thesis work presents, in Chapters 3 and 4 the design, implementation and experimental characterization results of an inductorless DC/DC converter and the techniques implemented to address wide voltage conversion range.

2.2 Aerospace

Aerospace is a flourishing moving industry comprising aeronautics and astronautics. In just five decades from the Apollo 11 mission, which first landed humans on the moon, the space economy has grown from a handful of nations to over 60 nations active in space-related activities worldwide and the trend is still growing. The growing space market value is confirmed by the recently born notion of Space 4.0. Analogous to Industry 4.0, which is the collective term for transformations across automation and data exchange in manufacturing technologies and processes, Space 4.0 focus is on interconnecting science, industry, politics and society in new ways [25, 26]. In the Space 4.0, space is evolving from being the preserve of few nations governments to a situation in which there is a continuous increase in space partners, including industry, participation with universities and private companies, in digitization and global interaction. The growing variety of services, required by the increasing number of space actors, creates challenges in the satellite and space vehicles design. Current trends in satellites show a rapid increase in data traffic and digital processing. The throughput of next-generation digital telecommunications satellites will exceed terabits per second of data, which have to be processed on board. For instance, the high-resolution cameras and synthetic aperture radars need high-speed communications between the instruments and storage [27]. Optical technology, thanks to its high bandwidth-length product, the

lightweight cabling, and electromagnetic hardness, can potentially be the solution for data-rate increment in the satellite. In this direction, the European Space Agency (ESA) has recently released the new SpaceFibre standard for onboard satellite communication up to 6.25 Gbps [28]. Hence, new electro-optical space compliant circuits have to be designed to meet the growing speed demand.
Analogous to the automotive sector, described in the previous section, the satellites are space-hungry systems, where the ever-higher integration of heterogeneous functions creates electromagnetic interaction demanding issues. The electric energy generated by the solar cells array feeds the Power Conditioning and Distribution Unit, which is composed of several modules (regulator, protection devices, battery regulators, power distribution for equipment/propulsion, etc.) devoted to electric power management. Then the power is sent to different functional units using power bus with fixed voltages, typically between 28 V and 50 V. Finally, DC/DC converters inside each functional unit are used to obtain the desired voltage level (e.g., 5 V, 3.3 V, 1.65 V) to feed specific circuit modules. The switching activity of inductor-based DC/DC converters generates EMI (ElectroMagnetic Interference) emission that potentially poses a threat to the correct operation of sensitive electronic equipment [29, 30]. Since the fundamental role that EMI has on the onboard satellite devices, techniques to mitigate EMI generation should be adopted, as shown in Chapter 5.
In terms of space exploration, today's debate has been dominated by future human space travel. Should it be toward the Moon or Mars? Since 2005, there has been a trend in favor of the Moon, although plans for future Moon and Mars missions have been designed simultaneously. Indeed, NASA has expressed its intention to land American astronauts on the Moon by 2024 [31]. ESA chief Jan Worner with the idea of the 'Moon Village' makes the Moon the next goal of international collaboration in space exploration [32]. Even private companies like Blue Origin and SpaceX are focusing on making lunar exploration an economic opportunity [33]. The Moon choice is probably driven by the lower harsh conditions and cost that the missions should address concerning the Mars target. Indeed, one of the biggest challenges of solar system exploration is the variety of extreme environments that astronauts, satellites, and probes must encounter and survive. For example, exploration of the Venus surface requires systems and instruments that can withstand intense heat (480 °C) and pressure (92 bar). In these severe conditions, where the reliability of the silicon technology is questioned, one of the most promising solution able to operate in this environment is the new high-gap 4H-SiC JFET integrated technology. Recent studies on this technology have demonstrated the feasibility of a ring resonator able to withstand 460 °C at 93 bar for 60 days [34] and the promising performance of a highly sensitive high-temperature sensor operating at temperature up to 460 °C and more [35].
Instead, a spacecraft on Jupiter must be designed to handle an extremely harsh radiation environment. Indeed, the currently most radiated mission was NASA's Europa Clipper mission, which aimed to send a spacecraft into orbit around Jupiter to perform forty-five repeated close science flybys of the icy moon, Europa. The goal was to produce high-resolution images of Europa's surface and determine its composition. The spacecraft was expected to withstand a total ionizing dose of 2.7 Mrad(Si), throughout the mission. It was designed with 12.7 mm aluminum walls to house most of the spacecraft and payload reducing to 150 krad(Si) the TID inside shields. Therefore, the electronic

devices were designed with a Radiation Design Factor (RDF) of two, to be compliant to 300 krad(Si) at the part location [36, 37]. If the electronic devices of the next spacecrafts overcome the technical radiation-tolerant challenge lower shields thickness and weigh could be used, reducing the enormous spacecraft launch cost and enabling the exploration of new cosmic spaces characterized by high-radiation levels.
In the optic of design radiation hard electronic devices, one of the most challenging terrestrial applications is made by high-energy experiments of particle physics, which require devices able to withstand even much higher radiation levels than current space missions.

2.3 High Energy Physics

Particle physics is the branch of physics that studies the basic constituents of matter and their interactions. Its research focuses on subatomic particles, including electrons, protons, neutrons, photons, neutrinos, and muons. Since many elementary particles rarely appear and fast decay under normal circumstances in nature, to allow their study, they are generated and detected by high-energy collisions of other particles in particle accelerators. Particle physics aims to investigate the fundamentals of matter in order to address unanswered key questions about the nature and origin of the Universe and to find the final general theoretical model, which overcome the issue related to the discrepancies between the theory of general relativity and the quantum mechanical. The main instruments for High Energy Physics are particle accelerators, which employ electric and magnetic fields to accelerate and focus particle beam again a fixed target or another particle beam. The high-energy particle interaction generates new particles and events that are detected and studied. The CERN (European Organization for Nuclear Research), located near Geneva, Switzerland, is equipped with the LHC (Large Hadron Collider) that is, currently, the world's most energetic accelerator. The particle detectors, inside the LHC, are made by different layers of sub-detectors. The innermost layer (the nearest to the interaction point) is the tracking device, that aims to reveal the paths of electrically charged particles through the trails they leave behind, instead, the calorimeters, placed in the outer layers, have the task to measure the energy lost by particles that go through them. The detector includes magnetic fields that bend the path of charged particles in a way that it is possible to calculate the particle momentum which helps in identifying the particle type. The information about particles is extracted by the combination of charge detected by sensors and its trajectory inside the detectors layer. When a particle passes through sensors (i.e. complex silicon diode structure) release energy-generating charge. This charge is collected by the front-end electronics, which properly condition the information signals, performing amplification, shaping, buffering, analog to digital conversion, and then the information is transmitted to remote data acquisition systems for data analysis and storage. The most recent significantly LHC discovery is the decay of one Higgs boson into four leptons or two photons that led to the discovery of the Higgs boson, also called the "God Particle", in 2012, which validated the Standard Model [38]. The probability of generating one of these interesting events in the interactions of two beams is extremely rare and is proportional to the luminosity of the collider. It corresponds to the number of particles per second in one beam multiplied by the number of collisions per unit area in the other beam at the crossing point. To increase the probability to detect physically interesting events, the

CERN's roadmap forecast an increasing luminosity of the LHC up to 5e-34 $cm^{-2}s^{-1}$ in the High Luminosity LHC (HL-LHC), foreseen by 2025 [39, 40]. For example, the extremely rare generation of two Higgs bosons and their decay into two pairs of photons has a probability of one event every 21.4 months, considering the LHC luminosity in 2012. This probability will be reduced to 2.5 months in the next HL-LHC scenario. The increase of power in future accelerators experiments requires the re-design of the detector front-end electronics to face high data rates and high radiation levels, e.g. up to 5 Gbps for a module including 4 pixel-detector CHIPIX65 readout ICs, each up to 1.2 Gbps [41], and a TID in the range from 800 Mrad to 1 Grad (SiO2) in the inner layers of the Silicon Trackers. This value is three order of magnitude higher than high-speed rad-hard link designed at the state-of-the-art, such as the Versatile link in [42] having roughly the same speed of 4.8 Gbps but with a radiation hardness of 500 kGy (i.e. 50 Mrad (SiO2), being 1 Gy = 100 rad). To be noticed that concerning today's most radiation-hard spacecraft, see Section 2.2, the TID level required in the HL-LHC is more than three thousand times higher, creating extreme challenges in electronic design. To the best of the author's knowledge, today in literature, there are not electronic systems able to operate at 1 Grad TID and there are only a few data of single transistors measurements at such high TID. The 65 nm CMOS technology seems to be the promising technology for these TID levels, therefore in this thesis, in Chapter 6 the main effects that such extreme radiation level generates on this technology are highlights. In response to these effects, some radiation-hard techniques are proposed and verified in the drivers design discussed in Chapter 7.

CHAPTER 3

High-Voltage and Fault Mitigation Design Techniques

The state-of-the-art conversion from nominal 48 V to low output voltages with a few hundred mA load requirements is dominated by inductor-based DC/DC switching converters [15, 17]. They provide high power efficiency conversion, but, on the other hand, are cumbersome and difficult to be integrated into embedded systems. Linear regulators are typically used only in very low power systems since they have a low power efficiency that depends on the Vout/Vin ratio [43]. When the power source provides up to 60 V, and the required output regulated voltages amount to a few voltages, then the power efficiency of linear regulator amounts to a few per-cent points. Integrated solutions can be achieved by relying on SC (Switched Capacitor) DC/DC converters. They have been proposed in literature mainly for low-voltage inputs, e.g. step-down regulation of Li-ions battery input voltages (below 5 V) to low-voltage and low-power loads in consumer devices (e.g. smartphone) [44–48] or as step-up converters for non-volatile memories and energy harvesting [49, 50]. To overcome the state-of-the-art limits this chapter presents the techniques used to manage a wide voltage range from 6 V to 60 V in an inductorless switching DC/DC converter design framework. In addition, in response to strong requirements of fault-prevention, fault-detection and fault-management of safety-critical systems, an innovative and integrable fault-tolerant technique is proposed, avoiding the state-of-the-art use of cumbersome transformers [51].

3.1 Switched Capacitor Converters

Despite the evolution of integrated technology has made enormous progress, going to use special materials with ferromagnetic properties and moving from two-dimensional solutions to three-dimensional ones. The realization of integrated inductors with good

features still presents great obstacles [52,53]. This difficult integration of inductors and transformers in silicon technology and the growing need for ever-higher integration, drive the converter architecture choice towards the SC converter topology. The SC DC/DC converters are characterized by the repetitive change in the circuit structure, and by using only capacitors, as energy storage elements, which are more suitable for a complete converter integration.
Two types of capacitive elements are used in SC DC/DC converters: flying capacitors, used to transfer the charge from input to output ports, and buffer capacitors, which stores the charge at the output port and mainly influence the steady-state ripple characteristics and the wake-up phase of the converter [54, 55]. SC converters, in stationary conditions, can be modeled as in Fig. 3.1, which includes:

- an equivalent ideal transformer with a turn ratio VCR (Voltage Conversion Ratio).
- an equivalent output resistor R$_{OUT}$ representing all converter losses proportional to the load current.
- an equivalent parallel resistor R$_{ZL}$ representing the losses in the zero-load current condition.

The R$_{ZL}$ value depends on the power wasted by switches drivers and by auxiliary systems, such as the oscillator or the control system. The effect of the R$_{ZL}$ is typically negligible compared to the R$_{OUT}$ losses [47]. The value of R$_{OUT}$ depends on the switching frequency, on the values of the capacitors and that of the switches ON-resistance. Instead, the VCR value depends on the selected circuit topology. According to Eq. 3.1 when a load is applied to the converter an output voltage drop is observed, due to the output resistor R$_{OUT}$.

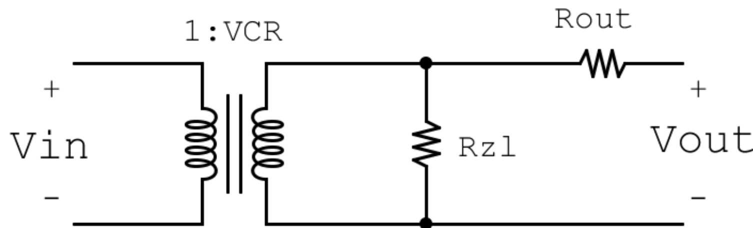

Figure 3.1: *SC converter equivalent model.*

$$V_{out} = VCR \cdot V_{in} - R_{OUT} \cdot I_{load} \tag{3.1}$$

As already highlighted, the strength of SC converters is their suitability for monolithic integration, as they only require native components for an integrated circuit technology: capacitors and switches. On the other hand, a lossless conversion can only be achieved by using an infinitely large amount of capacitance and ideal switches with zero ON-resistance, making R$_{OUT}$ in Eq. 3.1 negligible. In addition, while inductive DC/DC converters can implement a continuous voltage conversion ratio by using PWM (Pulse Width Modulation) technique, in SC converters the VCR is mainly determined by its topology, consisting of two or more specific configurations that are time alternated in a two-phase (or more phases) operation scheme. Therefore, only discrete

VCR values can be achieved in SC converters. The greater is the VCRs number used for the conversion, the smaller is the voltage oscillation step around the target voltage value. The Makowski and Maksimovic's theorem [54] explains the maximum number of VCRs that is possible to obtain in a network, as a function of the fly capacitors number:

> *"The realizable conversion ratio of a two-phase switched-capacitor dc-dc converter with a single dc voltage source, is given by a common fraction in the form:*
>
> $$M_i(k) = \frac{P[k]}{Q[k]}$$
>
> *Where P[k] and Q[k] are integers that satisfy:*
>
> $$Max[Abs(P[k]), Abs(Q[k])] < F[k]$$
>
> $$Min[Abs(P[k]), Abs(Q[k])] > 1$$
>
> *k is the total number of capacitors, and F[k] is the k-th Fibonacci number. The minimum number of switches to have all possible VCRs is equal to 3k+2."*

Since this theorem, it is possible to predict that using only one fly capacitor and a buffer capacitor, in an SC DC/DC converter circuit, the available VCRs are 1/2, 1 and 2, and a minimum number of five switches has to be used. While using two fly capacitors and a buffer capacitor the VCRs number increases to seven (1/3, 1/2, 2/3, 3/2, 1, 2, 3) and the minimum switches number grows to eight. In addition to the implementation of discrete VCRs, in order to achieve finer control of the output voltage, other control techniques can be realized, such as frequency sweep, PWM, switches ON-resistance control, SKIP [54]. The common denominator of these further techniques is their inefficiency action modality, indeed they regulate the converter output voltage changing the R_{OUT} of the model in Fig. 3.1. This, on a side, allows getting a fine control, but on the other side decreases the converter efficiency, exactly in the same way performed by linear converters.

3.2 Converter Architecture

Following the above-described design principles of the SC DC/DC converters, and the consideration in Chapter 2, an SC DC/DC converter was designed in 0.35 µm HV-CMOS AMS technology. As a case study, the DC/DC converter should regulate a wide input voltage range to two output points of load, 5 V and 1.65 V, for sensors and ECUs supply with power up to 2 W. In addition, it should ensure input-output insulation from input overvoltages or control strategy faults. In order to withstand the application requirements, the multistage converter in Fig. 3.2 is designed. The architecture is the cascade of three SC circuit stages and two linear regulators, whose aims are:

- regulating a wide input voltage range, from 6 V up to 60 V, to a value V_X of about 6 V.

- ensure high regulation performance from V_X to the two points of load, 5 V and 1.65 V.

- providing isolation between input and output for fault mitigation.

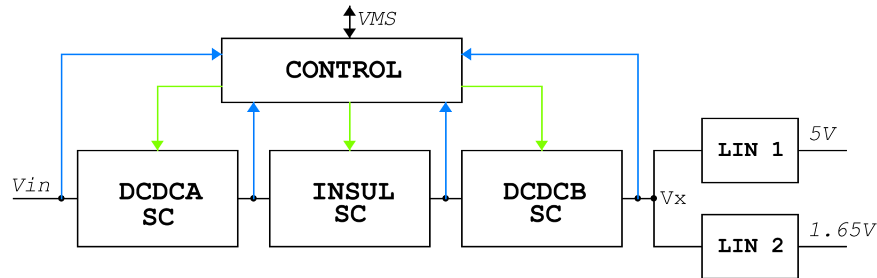

Figure 3.2: *Converter architecture.*

The use of a cascade of three SC stages allows distributing the wide input voltage on different voltage domains, making it easier for their management. The pre-regulated voltage, Vx in Fig. 3.2, is further regulated by two linear regulators, which work in parallel to achieve the two desired DC output values for ECUs and sensors supply. The linear regulators, in the last stage of the cascade, use a pass element to obtain the desired output voltage and an impedance modulation technique to achieve a low ripple level and good performance in terms of line/load regulation and PSRR (Power Supply Rejection Ratio). Since Vx is close to the target output voltages the linear converter efficiency, which depends on the ratio Vout/Vx still be acceptable. The control unit in Fig. 3.2 supervises the behavior of all stages, in all operating modes (waking phase, normal operation, under/over-voltage), and manages the VCRs selection taking into account the input voltage of each stage. In addition, it provides a communication interface for diagnostic and configuration towards an external host. The architecture, in Fig. 3.2, is scalable and parametric in terms of the number of SC stages in the cascade and of linear regulators working in parallel at the end of the cascade, adapting the converter to the application constraints. Indeed, together with the automotive world and satellites, displayed in Chapter 2, the number of applications moving towards 48 V power supply systems is growing rapidly: the networking and communication systems, today, use 48 V power buses to supply their devices [56] and the ETSI (European Telecom Standard Input) defines the 48 V level as the nominal voltage level but a wide range from 36 V to 60 V could be assumed by the bus [57].

With reference to Fig. 3.2:

- the first conversion stage (DCDCA) is a step-up/down converter designed to manage a wide input dynamic voltage.

- the insulator stage (INSUL) provides insulation between the input and the output ports of the system.

- the second conversion stage (DCDCB) reduces the output resistance of the SC converter part to ensure the correct operation of the point-of-load linear converters.

- two linear regulators meet the nominal outputs (1.65 V with a load current from 0 to 50 mA, and 5 V with a load current from 0 to 400 mA) and ripple requirements.

Table 3.1, for each SC stage in Fig. 3.2, shows the implemented conversion ratios and the voltage range where they are applied. For example, in ideal condition, neglecting the converter losses, if a 48 V is applied at the designed converter the stage DCDCA will work as step-down (VCR = 1/2) generating 24 V output voltage. This voltage will not be altered by the insulator and will be the input of the DCDCB, which will divide it for a factor 3 generating a Vx of 8 V. Then the two linear converters will generate the target output voltages.

Table 3.1: *VCRs and input-output voltages of the three SC stages and of the two linear converters.*

Stage	Input Voltage [V]	VCR	Output Voltage [V]
DCDCA	6 <Vin <15	2	12 <Vout <30
	15 <Vin <29	1	15 <Vout <29
	19 <Vin <60	1/2	14.5 <Vout <30
INSUL	12 <Vin <30	1	12 <Vout <30
DCDCB	12 <Vin <18	1/2	6 <Vout <9
	18 <Vin <30	1/3	6 <Vout <10
LIN 1	Vx >6	-	5
LIN 2	Vx >3	-	1.65

3.3 Circuit/Transistor-Level Converter Sizing

3.3.1 Eqivalent Output Resistance of each SC stage

The design of each single SC circuit is performed following a top-down approach. The constraints of each stage were derived considering the maximum equivalent output resistance of the whole converter system that allows meeting the system requirements. Eq. 3.2 shows the maximum equivalent R_{OUT} of the SC sub-system that allows a correct functionality in these worst conditions:

- minimum input voltage Vin_{min} = 7 V;
- maximum load current $Iload_{max}$ = 300 mA;
- minimum output of the 3 SC stages Vx_{min} = 5.3 V. The value of Vx_{min} is obtained considering the 5 V output plus 0.3 V drop on the pass-transistor of the LIN regulators.

$$R_{OUT-max} = \frac{V_{in-min} - Vx_{min}}{I_{load-max}} = 5.67\Omega \tag{3.2}$$

With the selected $R_{OUT-max}$, if the DC/DC converter is used to supply higher currents than $I_{load-max}$ used above, the correct convert functioning is guaranteed, but with higher input voltages than the target V_{in-min} level. Furthermore, if the input voltage

drops below 7 V, the converter continues to work providing lower current levels then $I_{load-max}$. For example, if the loads require 400 mA current, the minimum input voltage, to ensure the correct operation of the converter, is 7.57 V. Instead, if the input power bus drops to 6 V, the converter is able to provide currents below 125 mA.
The value in Eq. 3.2 is obtained considering a requirement of 5 V regulated output. For the 1.65 V output V_{x-min} is about 2 V, and with $I_{load-max}$ = 50 mA and V_{in-min} = 3 V a less stringent $R_{OUT-max}$ value of about 20 Ω is obtained.
Considering the equivalent model in Fig. 3.1 for a generic SC converter, the system in Fig. 3.2 is modeled like in Fig. 3.3 neglecting the R_{ZL} resistors.

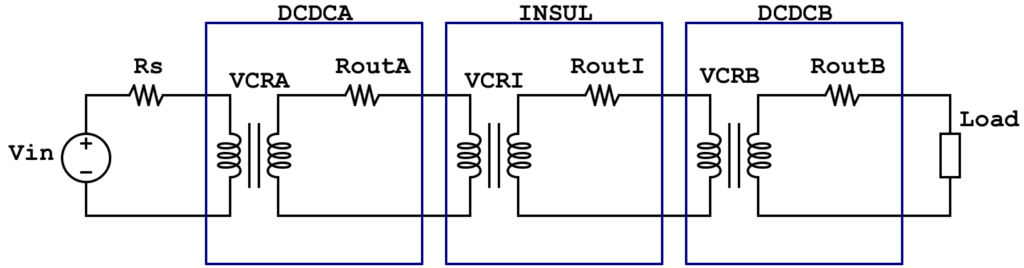

Figure 3.3: *Converter equivalent circuit.*

The overall equivalent output resistance is calculated as in Eq. 3.3. In the worst conversion condition, when V_{in-min} drops down to 6 V the DCDCA stage works in step-up mode (see Table 3.1) and the DCDCB stage performs a VCR = 1/2, then Eq. 3.4 can be derived.

$$R_{OUT} = [(R_s \cdot VCR_A^2 + R_{OUTA}) \cdot VCR_I^2 + R_{OUTI}] \cdot VCR_B^2 + R_{OUTB} \tag{3.3}$$

$$R_{OUT-MAX} = \frac{4R_s + R_{OUTA} + R_{OUTI}}{4} + R_{OUTB} \approx \frac{R_{OUTA} + R_{OUTI}}{4} + R_{OUTB} \tag{3.4}$$

The use of a cascade approach, with a step-down converter as the last stage, relaxes the equivalent resistance of the other SC stages, being it multiplied for the VCR_B^2 of the last stage, whose value in the worst case is equal to 1/4, see Eq. 3.4. Table 3.2 shows the resistance values chosen for each stage after iterative simulations and taking into account the different MOSFETs used. Indeed, the use of a cascade architecture allowed using different high-voltage MOSFETs in the converter design, and the lower is the maximum voltage that they can sustain and the lower is their ON-resistance, reducing conversion losses and increasing the converter performance.

Table 3.2: *Target output equivalent resistor of the 3 SC stages*

	DCDCA	INSUL	DCDCB
R_{OUT}	7.5 Ω	10 Ω	1.2 Ω

3.4 Switches typologies

The choice of the converter switches is a key element and depends on the maximum voltages required by the application. The use of N-MOSFETs is preferred for their lower ON-resistance compared to P-MOSFETs one (by a factor 2.5 due to higher mobility of electrons than holes, see Table 3.3). However, to avoid the use of charge pumps to turn on the transistors, N-MOSFETs are used only to replace the switches with the source connected to GND.

Table 3.3: *N- and P-MOSFET characteristics in 0.35 µm HV technology.*

	$\|V_{DS}\|$max [V]	$\|$Vth$\|$typ [V]	R_{ON} [k$\Omega \cdot \mu m$]
P-MOSFET	71	0.6	46
N-MOSFET	55	0.4	21

One of the main problems to design a circuit able to performs both step-up and step-down conversions (e.g. DCDCA stage) is the drain-source voltage polarity of its switch elements. Indeed, an incorrect polarization of pass elements leads to current injection in the substrate. Fig. 3.4 shows the electrical equivalent models of the N and P high-voltage MOSFETs (known in the literature as LDMOSFETs, Lateral Diffusion MOSFETs) in the 0.35 µm AMS technology. When these transistors are used as power switches the following issues arise:

- For the N-MOSFET in Fig. 3.4, if the bulk is connected at its source and the drain voltage is lower than the source voltage the current flows in the bulk-drain parasitic diode. In this case, the switch may remain ON regardless of the gate voltage. Moreover, the substrate-drain diode can turn ON and injects charge in the substrate. For the N-MOSFET, the countermeasure used to mitigate this effect is decreasing the ON-resistance of the N-MOSFET, thus reducing the negative V_{DS} on the MOSFET below the threshold voltage of the parasitic diode.
- For the P-MOSFET in Fig. 3.4, if its bulk is connected at the source of the MOSFET, then in some phases it can have a lower potential than the drain. In this case, the current can flow inside the drain-bulk parasitic diode and it is not possible to turn OFF the MOSFET using the gate voltage. Furthermore, the parasitic vertical PNP BJT may inject current in the substrate. This BJT has good emitter efficiency because the drain has P-plus doping and the thin well creates a short base. This current injection, if not avoided, could have destructive effects. To mitigate this issue two new circuit topologies are proposed hereafter.

Fig. 3.5 shows the first topology used for the design of the switches. In this configuration, the Mb MOSFET connects the bulk of the pass MOSFET (M MOSFET) to his drain (node A) to bypass the drain-bulk parasitic diode. The driver unit is connected between the gate and the source (node K) of the M pass element to handle its V_{GS}. Therefore, when the driving signal is low (OFF) the gate is connected at the source of the MOSFET and this creates a diode configuration.

The proposed solution is different from known approaches in the literature, where the diode configuration is made connecting the gate with the drain and hence V_{GS} =

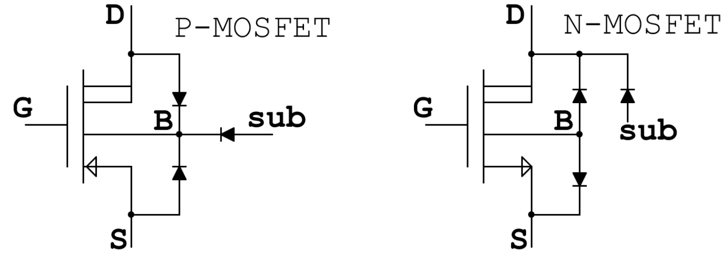

Figure 3.4: *HV-PMOSFET and HV-NMOSFET equivalent circuits.*

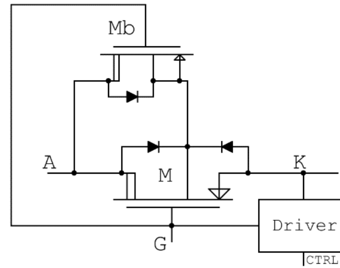

Figure 3.5: *MOSFET switch in controlled diode topology.*

V_{DS}. However, for the used HV-MOSFET, which should sustain V_{DS} values up to 70 V, this conventional solution cannot be adopted, since the maximum voltage on the gate-source junction can not exceed 3.6 V. Instead, the diode configuration in Fig. 3.5 is obtained connecting in the pass element M the gate with the source. This circuit solution protects the gate-source junction from high voltages. A reduction of the ON-resistance of the M pass element in Fig. 3.5 is obtained increasing the overdrive with a P-MOSFET driver.

Fig. 3.6 shows the operative modes of the circuit in Fig. 3.5. The dotted green and red lines are the test bench signals: the first is the voltage across the equivalent diode (V_{AK}), and the second is the control signal of the driver (V_{GK}). The solid blue signal I_{AK} in Fig. 3.6 is the current value inside the pass element M. If the V_{AK} voltage drop is higher than a threshold voltage Vth, the M and Mb MOSFET transistors turn ON thanks to the diode effect and the current flows regardless the driver state (solid blue signal I_{AK} from 0.0625 ms to 0.6 ms in Fig. 3.6). Of course, when the driving signal enables the driver, the MOSFET transistors are in deep conduction and their ON-resistance is lower, and the current increases (solid blue signal I_{AK} from 0.3 ms to 0.45 ms in Fig. 3.6). If the V_{AK} voltage drop is negative, the proposed circuit topology does not allow the flow of current (solid blue signal I_{AK} from 0.6 ms to 0.7 ms and from 0.85 ms to 1 ms) unless the driving signal enables the driver and the current is different from zero (solid blue signal I_{AK} from 0.7 ms to 0.85 ms in Fig. 3.6).

The Mb MOSFET drives the bulk of the M MOSFET to avoid that the drain-bulk parasitic diode turns ON and that the parasitic PNP bipolar transistor (drain-bulk-substrate) injects current in the substrate. If the bulk of the MOSFET has a small size, then its ON-resistance is high and consequently, the voltage drop is high. The size of the Mb in comparison with the size of M is chosen following the Eq.3.5.

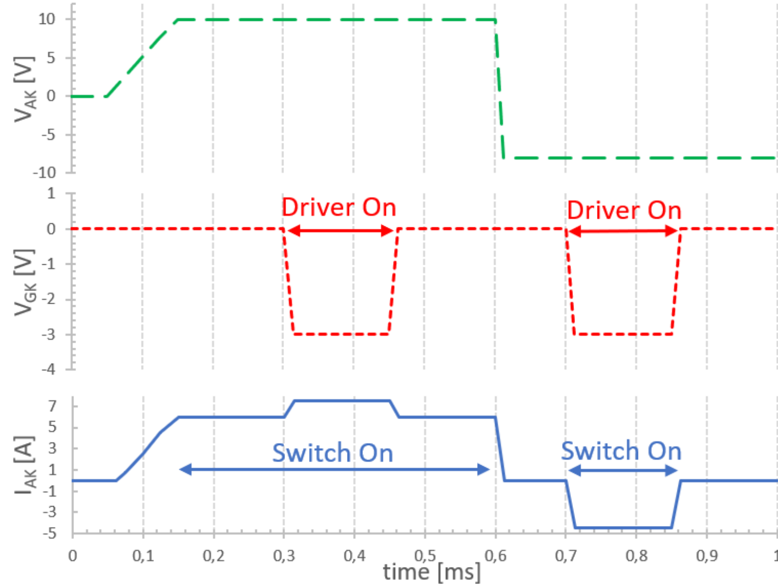

Figure 3.6: *Test of circuit in Fig. 3.5.*

$$M_{b-size} = \frac{M_{size}}{10} \tag{3.5}$$

The 1:10 ratio has been found considering the charge injected into the bulk and substrate (Qb in Table 3.4, the ON-resistance of the Mb device (R_{ON} in Table 3.4), and the voltage drop (Vdrop in Table 3.4) between the drain-bulk junction for different ratios of Mb and M. Table 3.4 shows some simulation results. For the small size of Mb (e.g. ratio 1/200) the voltage drop is too high, so the parasitic bipolar turns ON and injects charge in the substrate. Increasing the size of Mb (e.g. reducing the size ratio from 1/200 to 1/10) the voltage drop decreases and the charge injected in the substrate decreases. On the other side, by increasing the size of Mb the bulk width of Mb increases and, beyond the 1/10 ratio, a higher charge is required. Therefore, a 1/10 ratio is chosen to size the MOSFETs.

Table 3.4: *Mb and M MOSFETs size ratio.*

Size ratio	Qb [pC]	R_{ON} [Ω]	Vdrop [mV]
1/200	460	380	798
1/20	206	47	228
1/10	26	22	122
1/5	52	12	56

Not all the switches of this converter can be replaced with the circuit in Fig. 3.5, because they are also controlled by the V_{AK} voltage and not only by driving signals. One solution to solve this issue is the use, as in Fig. 3.7, of the back-to-back two-diode structure, with external drains to protect the low-voltage junctions (the voltage across the source-gate and the source-bulk junctions cannot exceed 3.6 V). Fig. 3.8 shows the signals of the operative modes of the back-to-back circuit in Fig. 3.7. The blue and

orange lines are the test bench signals applied at the switch. The light blue and dotted green signals are the voltages V_{AK} and V_{KB} on the single diode topology. The red signal I_{AB} is the current value that flows in the two-pass elements M0 and M1.

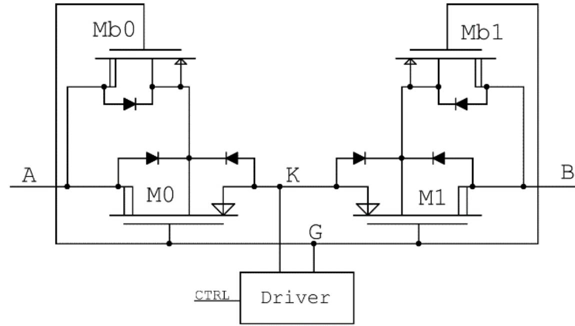

Figure 3.7: *Back-to-Back diode topology.*

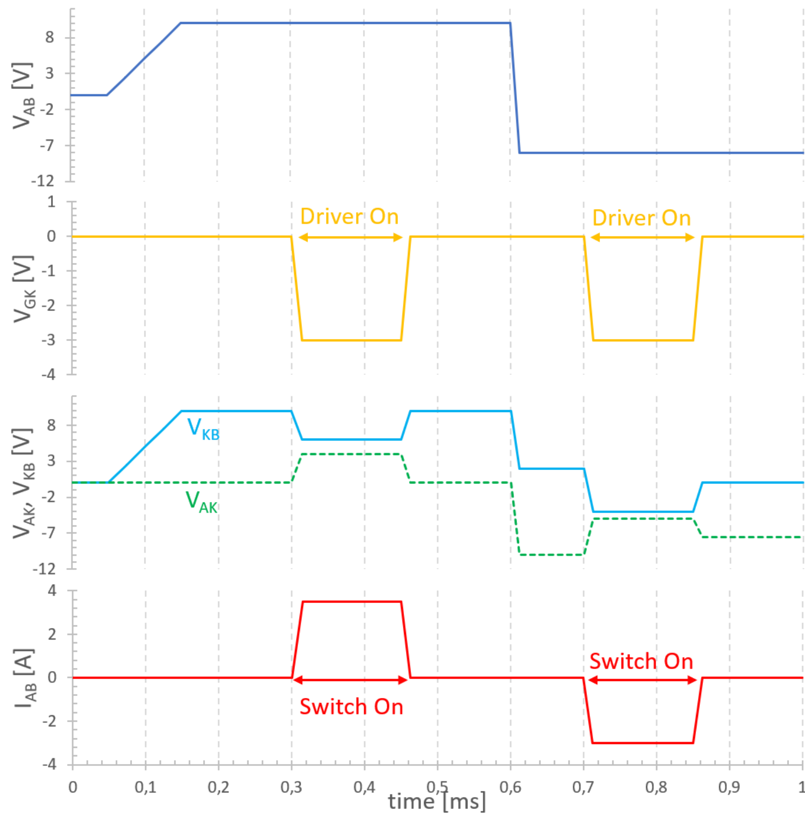

Figure 3.8: *Test of circuit in Fig.3.7.*

The advantage of the circuit in Fig. 3.7 respect to Fig. 3.5 is the following: the positive V_{AB} voltage that turns ON the M and Mb MOSFETs in Fig. 3.5, in Fig. 3.7 turns ON the M0 and Mb0 MOSFETs ($V_{AK} = 0$ so they are ON), but M1 and Mb1 are in inverse polarization ($V_{KB} \neq 0$) so the current cannot flows (red signal I_{AB} until 0.3 ms in Fig. 3.8). To turn ON the whole circuit of Fig. 3.7 it is necessary driving the elements with an external driver, which creates a controlled voltage drop between the gate and

the source of MOSFET. Indeed, in Fig. 3.8 between 0.3 ms and 0.45 ms when there is a V_{GK} swing of 3 V the current I_{AB} is different from 0. Similar behavior appears between 0.6 ms and 1 ms, when negative V_{AB} is applied, thanks to the symmetry of the topology in Fig. 3.7. The disadvantage of the circuit in Fig. 3.7 respect to Fig. 3.5 is that it adopts two series MOSFET transistors. Hence, a trade-off between area and efficiency is necessary when designing the converter. Concerning the charge injection issue, the two topologies, in Fig. 3.5 and Fig. 3.7, have a reduced injection of charge in the substrate compared to straightforward circuit configurations, for example, those using a single pass-transistor as in Fig. 3.4, or two series pass-devices. For the circuit in Fig. 3.5 the charge injection is mainly due to source-bulk parasitic diode, which turns ON for negative V_{AK} and V_{GK} = 0 (from 0.6 ms to 0.7 ms and from 0.85 ms to 1 ms in Fig. 3.6). The same effect appears for the circuit in Fig. 3.7 (from 0.15 ms to 0.3 ms, from 0.45 ms to 0.6 ms, from 0.6 ms to 0.7 ms and from 0.85 ms to 1 ms in Fig. 3.8). However, the charge injection is present mainly during the voltage transient because the bulk is 'floating' (the Mb MOSFET is OFF) and has a capacitance behavior. Hence, after a transient, the bulk of M is charged and has a voltage level close to M-source voltage so the flow of charge is stopped. In addition, for the structure in Fig. 3.7, the two source-bulk parasitic diodes are inside the structure. Hence, for positive V_{AB} and V_{GK} = 0 the source-bulk parasitic diode of M1 turns ON, but in series there is the ON-resistance of M0, which is not a so low resistance (V_{GK} = 0). This ON-resistance reduces the capacitive current peak inside the bulk of M1 and so reduces the charge injected in the substrate. Furthermore, the presence of the ON-resistance of M0 increases the transient time. This improves the charge redistribution in the bulk and the recombination of the charge injected in the substrate. Thanks to the symmetry of the structure of Fig. 3.7 these considerations are true also for the parasitic BJT of M0 for negative V_{AB} and V_{GK} = 0. Instead, in the topology in Fig. 3.5 the charge injected in the transient time is not reduced as in Fig. 3.7. In the proposed DC/DC converter, this switch topology (Fig. 3.5) is used to make three switches: S2 in DCDCA (see Section 3.5), S13 and S14 in DCDCB (see Section 3.6), which have the 'K' node connected with the output node of the stages. These nodes, in normal operating conditions, thanks to the output capacitor size (three times higher than the fly capacitors) have a nearly constant voltage level. The M-bulk voltage, when the switch is OFF, is very close to 'K' node voltage. While, when the switch is ON, the M-bulk voltage is connected to the 'A' node, which has a voltage close to 'K' node (the lower the switch ON-resistance, the closer the voltage values of 'A' and 'K' nodes). Therefore, in normal operating conditions, the bulk voltage of the M MOSFET changes slightly and this reduces the charge injected.

3.5 First DC/DC converter stage

The architecture chosen for the DCDCA SC stage is the two-phase serial-parallel converter showed in Fig. 3.9. It, using a small number of elements, only two capacitors and five switches, is able to perform both step-up and step-down conversion. Following the ON-OFF switching indications, provided in Table 3.5, the converter performs three different VCRs modifying its network topology. The VCR selection is managed by the control stage observing the stage input voltage. The switching elements of this

stage are composed of 70 V P-MOSFETs available in the 0.35 µm technology. The only switch replaced with an N-MOSFET is the switch S3 in Fig. 3.9, thanks to its low-voltage gate driving signal. Although its appetible use for its low ON-resistance, it can be responsible for the substrate injection problem. When the current flows from its source to its drain the parasitic diode drain-substrate may turn ON and injects current into the substrate. In this case, to avoid this dramatic effect the adopted countermeasure was designing the S3 switch to obtain as lower ON-resistance as possible. This in order to keep the MOSFET drain voltage lower than the parasitic diode threshold voltage in all the switching phases.

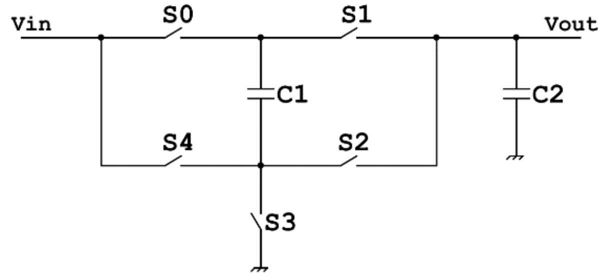

Figure 3.9: *DCDCA converter stage topology.*

Table 3.5: *Phases for the DCDCA converter stage.*

VCRs	Phases	ON Switches	OFF Switches
X1/2	1	S0-S2	S1-S3-S4
	2	S1-S3	S0-S2-S4
X1	1	S0-S3	S1-S2-S4
	2	S1-S3	S0-S2-S4
X2	1	S0-S3	S1-S2-S4
	2	S1-S4	S0-S2-S3

The voltage drop on the switches S0 and S1 in Fig. 3.9, when the converter performs both step-down and step-up conversions, changes from positive to negative and vice versa. Hence, the back-to-back circuit in Fig. 3.7 is needed for S0 and S1. Although the voltage in the switch S2 is both positive and negative, it is replaced with a single diode topology, as in Fig. 3.5, because the positive V_{AK} phase coincides with its conduction phase. The S4 switch is replaced with a single P-MOSFET because its source-drain voltage is always positive. Fig. 3.10 shows the transistor-level scheme of the DCDCA stage.

The main technique used to size the switches and the capacitors in Fig. 3.10, is based on the Charge Flow Analysis. This analysis studies the converter in two well-defined operating regimes: the Slow Switching Limit (SSL) and the Fast Switching Limit (FSL) [47,55,58]. In SSL, the converter operates at a frequency much lower than the time constants of the converter, thereby allowing the full charge and discharge of the fly capacitor. The losses are dominated by the charge transfer between capacitors. The equivalent resistor R_{SSL} can be expressed as in Eq. 3.6, where f_{sw} is the switching frequency and k_{SSL} is a coefficient that depends on the VCRs of the converter. In FSL,

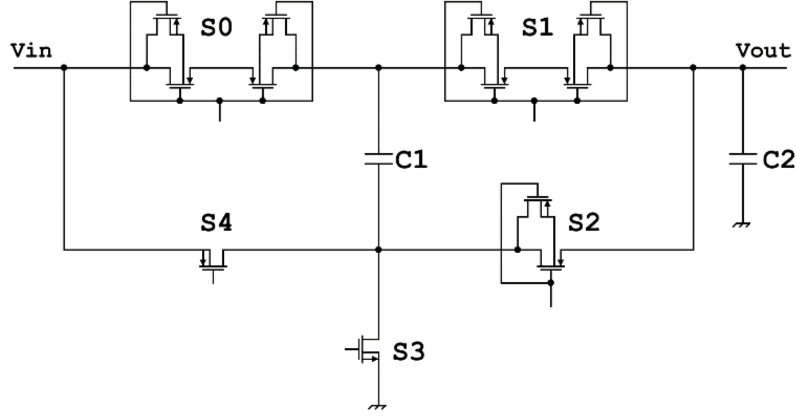

Figure 3.10: *Transistor level schematic of DCDCA converter stage.*

the converter operates at a switching frequency much higher than the time constants of the converter, limiting the charge and discharge of the transient time of the capacitors. Conduction losses are due to the ON-resistance of the switches. The equivalent resistor R_{FSL} can be calculated as in Eq. 3.6, where SW are the active switches in that specific VCR configuration, R_{ON-i} is the ON-resistance of the i-switch and k_{FSL-i} is a coefficient that depends on the converter configuration. The total equivalent output resistor can be evaluated with experimentally-derived Eq. 3.7.

$$R_{SSL} = \frac{k_{SSL}}{f_{sw}} \sum_{i \in C_{fly}} \frac{1}{C_{fly-i}}, R_{FSL} = \sum_{i \in SW} (R_{ON-i} \cdot k_{FSL-i}) \tag{3.6}$$

$$R_{OUT} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{3.7}$$

According to the values in Table 3.2 the first stage is sized to obtain $R_{OUT} \leq 7.5$ Ω, considering the network coefficients listed in Table 3.6. The switching frequency is fixed to 90 kHz to reduce radiated EMI disturbs, which will be analyzed with more details in Chapter 5. Since Eq. 3.7 and the fixed switching frequency, the R_{SSL} depends only on the fly capacitors value and on the selected VCR, as shown in Fig. 3.11. The capacitance value is selected with a trade-off between the R_{SSL} value and the size/cost of the capacitor to meet the target $R_{OUT-Max}$. From Fig. 3.11 choosing a Cfly equal to 3.3 µF a R_{SSL} value of 0.8 Ω for VCR = 1/2 and 3.3 Ω for VCR = 1 and VCR = 2. The value of the output buffer capacitor, 10 µF in this work (much lower than the 5 mF in [51]), influences the output characteristics and is typically higher than the fly capacitor.

Table 3.6: *k_{SSL} and k_{FSL} coefficients for the DCDCA stage.*

	VCR = 1/2	VCR = 1	VCR = 2
k_{SSL}	0.25	1	1
k_{FSL}	0.25	1	1

The R_{FSL} value depends on the ON-resistances of the switches and on the network topology. The MOSFET transistors used for the switches are sized to meet the equiv-

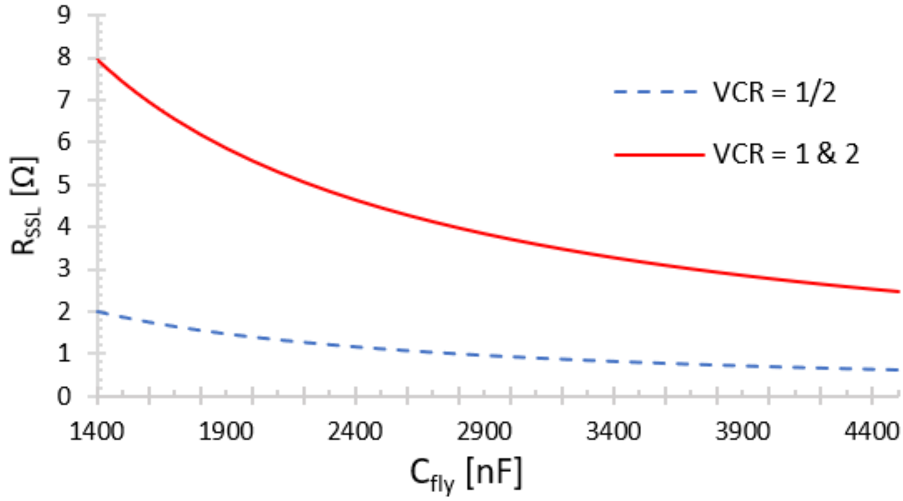

Figure 3.11: *First Stage R_{SSL} as a function of Cfly and VCRs.*

alent R_{OUT} specification in Table 3.2, taking into account the occupied area. For the first sizing of the converter, a hypothesis is made: all the switches are composed of a single MOSFET with the same size (the ON-resistance is then calculated from Table 3.3). Thanks to this initial hypothesis, it was possible to evaluate in the Eq. 3.8 the power losses due to R_{FSL}, depending on the MOSFET width W and R_{SSL}. In Eq. 3.8 I_{out} is the output current of the SC converter stage. The obtained value is then compared to the driver switching power calculated according to Eq. 3.9. In Eq. 3.9 z is the number of elements that switch in every period (it depends on the VCRs, see Table 3.5), $\triangle V_{GS}$ is fixed by the driver at 3 V, f_{sw} is the switching frequency (90 kHz), C_{GS} is the MOSFET gate capacitance and depends on the width size W. Fig. 3.12 shows a comparison of the two power contributions as a function of W.

$$P_{SSL\&FSL} = \sqrt{R_{SSL}^2 + R_{FSL}^2(W)} \cdot I_{out}^2 \tag{3.8}$$

$$P_{driver} = z \cdot \triangle V_{GS}^2 \cdot f_{sw} \cdot C_{GS}(W) \tag{3.9}$$

From Fig. 3.12 it is clear that the driver contribution can be neglected compared to $P_{SSL\&FSL}$ values. Therefore, the larger is the MOSFET size and the lower is the dissipated power. However, a trade-off has to be found between area and power consumption when sizing the MOSFET. After an iterative analysis, carried out in the Cadence's environment and considering real switches topology and their parasitic elements in the 0.35 µm technology, the switches size listed in Table 3.7 are obtained. The results in Table 3.7 highlight the large size of the switch S3, which is the N-MOSFET that needs a very low ON-resistance to reduce the substrate injection current, as previously described. The size of the MOSFET devices and the value of the ON-resistances for switches S0 and S1 are higher than those for S2 and S4. Indeed, S0 and S1 adopt the scheme in Fig. 3.7, which is characterized by a series topology. Once determined the size of the fly capacitor (3.3 µF in this case) and the size of the MOSFET transistors in Table 3.7, it is possible to calculate in Table 3.8 the R_{OUT} of the converter in three different operating modes. The constraint R_{OUT} <7.5 Ω in Table 3.8 is met.

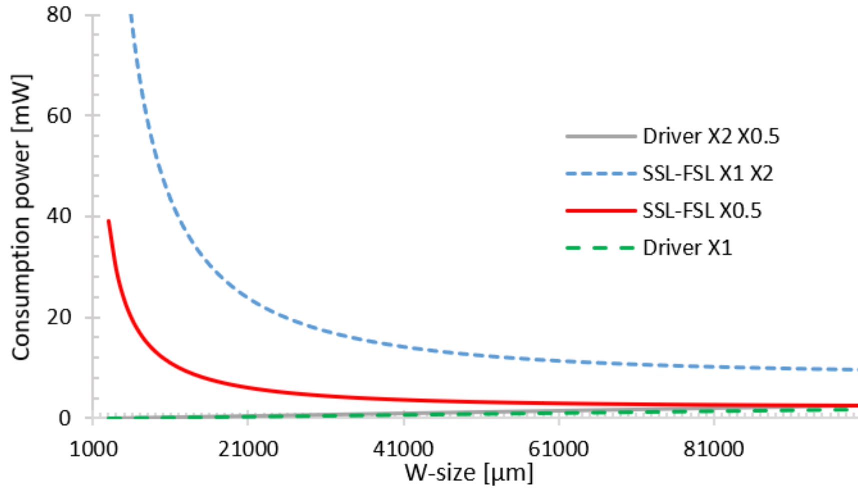

Figure 3.12: *Consumption power in function of MOSFET size W (Iload = 165 mA).*

Table 3.7: *Size and ON-resistance of the switches, DCDCA converter stage.*

	Size [µm]	$R_{ON-SWITCH}$ [Ω]
S0 (M0)	40000	2.3
S0 (M1)	40000	
S1 (M0)	40000	2.3
S1 (M1)	40000	
S2	30000	1.53
S3	80000	0.26
S4	25000	1.84

Table 3.8: *Output equivalent series resistances.*

VCR	R_{SSL} [Ω]	R_{FSL} [Ω]	R_{OUT} [Ω]
1/2	0.8	1.6	1.79
1	3.3	5.1	6.09
2	3.3	6.7	7.47

3.6 Second DC/DC converter stage

Following the sizing technique used to design the DCDCA, in Section 3.5, the last SC conversion stage, labeled DCDCB, is sized. The selected topology, shown in Fig. 3.13, uses two flying capacitors and a buffer capacitor. This topology is able to perform up to seven VCRs but only the VCRs equal to 1/2 and 1/3 are used in the converter. The status of the switches for the two conversion ratios are listed in Table 3.9, alternating the two phases. The hard requirement on the equivalent output resistance of this stage, listed in Table 3.2, makes challenging its design. The selected topology allows using two simple N-MOSFETs, for the switches S15 and S16, which having low ON-resistance help the output resistance reduction. The switches S10, S11 and S12 are replaced with simple P-MOSFETs, while for the switches S13 and S14 a diode topology, showed in Fig. 3.5, is adopted, as shown in Fig. 3.14. The values of the chosen capacitors are 3.3

μF for the two flying capacitors (with a maximum operating voltage of 30 V) and 10 μF for the output capacitor (whit a maximum operating voltage of 10 V). For this third SC stage, since the input and output voltage ranges are limited to maximum 30 V and 10 V respectively, MOSFET transistors with a lower sustainable voltage than the ones used in DCDCA, are adopted. The selected MOSFETs, having a low ON-resistance, allowed meeting the strong output resistance requirement with a low area consumption, as shown in Table 3.10.

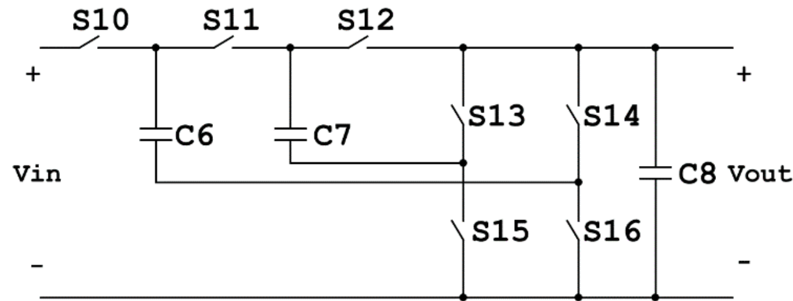

Figure 3.13: *DCDCB converter stage topology.*

Table 3.9: *Phases of the DCDCB converter stage.*

VCRS	Phases	ON Switches	OFF Switches
X1/2	1	S10-S11-S13-S16	S12-S14-S15
	2	S10-S12-S15-S16	S11-S13-S14
X1/3	1	S10-S12-S14-S15	S11-S13-S16
	2	S11-S13-S16	S10-S12-S14-S15

Table 3.10 shows the size and ON-resistance of the switches used in the DCDCB stage to meet the constraint in Table 3.8, considering the K_{SSL} and K_{FSL} values of 0.09 for VCR = 1/3 and 0.25 for VCR = 1/2.

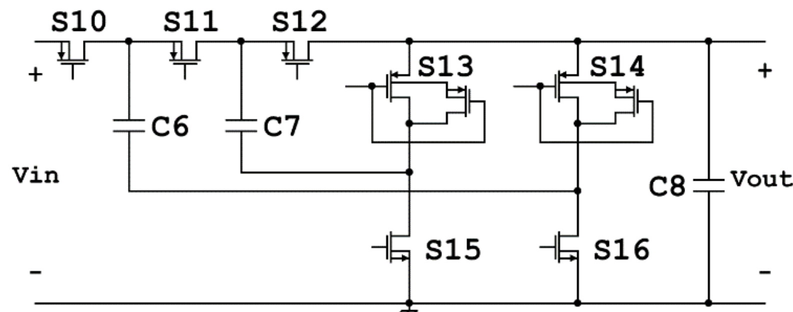

Figure 3.14: *Transistor level schematic of DCDCB converter stage.*

3.7 Insulator stage

One of the safety requirements of the automotive and aerospace electronics adopted for critical systems is the design of fault-free systems. Some fault-tolerant techniques can

Table 3.10: *Size and ON-resistance of the switches, DCDCB converter stage.*

Switch	Size [µm]	$R_{ON-SWITCH}$ [Ω]
S10	48000	0.6
S11	48000	0.6
S12	48000	0.6
S13	28500	0.6
S14	28500	0.6
S15	28000	0.5
S16	28000	0.5

be applied already at the physical level. The DC/DC switching converters to avoid the propagation of malfunctions (e.g. over-voltages) at the input towards the low-voltage output ports, typically use the magnetic coupling of transformers. The proposed inductorless converter overcomes the input-output isolation issue using an innovative SC circuit solution, which using only switches and capacitors is more integrable friendly. The insulator stage works with a unitary VCR according to the scheme in Fig. 3.15, which uses two flying capacitors, a buffer capacitor, and five switches. The presence of this stage, which does not participate in conversion, allows meeting the fault-tolerant constraint, but on the other hand, it affects negatively the efficiency performances and silicon area occupation of the whole converter. The insulation property between input and output is ensured by electrostatic coupling of the two capacitors connected in series, C3, and C4 in Fig. 3.15. This stage works alternating turning-ON and turning-OFF of switches during two phases as listed in Table 3.11. In the first phase, Vin recharges C3, whereas C4 provides charge to the output, avoiding a direct connection between input and output. In the second phase, C3 and C4 are connected, but C3 is disconnected from the input and C4 is disconnected from the output. Hence, also in this phase, a direct connection between input and output is avoided. Thanks to the adopted cascade stages architecture, the first conversion stage reduces the wide input voltage range to voltages lower than 30 V (see Table 3.1) allowing the use, for this stage, of the 50 V P-MOSFETs characterized by a 25% lower ON-resistance than the 70 V P-MOSFETs devices in Table 3.3.

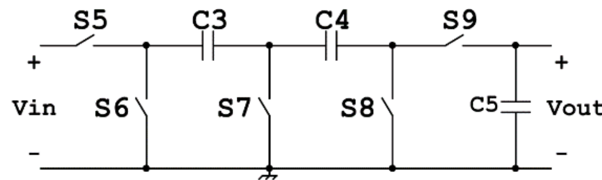

Figure 3.15: *Insulator stage topology.*

Table 3.11: *Phases of the insulator stage.*

VCRS	Phases	ON Switches	OFF Switches
X1	1	S5-S7-S9	S6-S8
	2	S6-S8	S5-S7-S9

Although the proposed insulator stage does not use a cumbersome transformer but only silicon native components, some integration issues still be present in the selected 0.35 µm HV technology. Indeed, the switches S7 and S8, in Fig. 3.15, are not directly replaceable with simple N-MOSFETs for their strong negative V_{DS}, which will be the source of substrate injection currents. If P-MOSFETs are used, it would be mandatory the presence of negative voltages to drive the transistors, and hence the use of charge pumps. In order to face this issue, these two switches are replaced with two external off-chip Schottky diodes, as shown in Fig. 3.16. If a multi-well or SOI (Silicon On Insulator) technology had been used for the converter, the whole insulator stage would have been integrated into the silicon chip. Being the switch S6 crossed by the only one-direction current, it was replaced by a simple N-MOSFET. The switch S9 has to work with both positive and negative voltage on its terminals so a back-to-back diode topology, as in Fig. 3.7, is chosen. Considering the voltages and currents managed by the switch S5, it was replaced with a simple P-MOSFET. Following a design approach similar to that in Section 3.5, the insulator stage transistors and capacitors were sized to meet the equivalent output resistance constraint of Table 3.8. The switching frequency is the same as the first stage (90 kHz) while both the K_{SSL} and K_{FSL} have a unitary value. The values chosen for the capacitors are the same as the first DCDCA stage, 3.3 µF for flying capacitors C3 and C4 and 10 µF for the buffer capacitor C5 (maximum operating voltage 50 V). The main difference compared to the DCDCA sizing is the presence of two flying capacitors in series, which doubles the R_{SSL} value. Instead, the R_{FSL} value is similar, since the reduced ON-resistance of 50 V P-MOSFET components is compensated by the increased resistance due to the use of the external Schottky diodes. The values of the switches used in this stage are listed in Table 3.12.

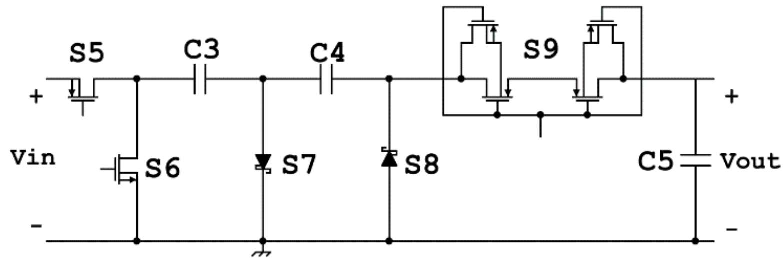

Figure 3.16: *Insulator stage transistor level circuit.*

Table 3.12: *Size and ON-resistance of the switches in the insulator stage.*

	Size [μm]	$R_{ON-SWITCH}$ [Ω]
S5	39500	0.9
S6	30000	0.9
S9 (M0)	39500	1.8
S9 (M1)	39500	

3.8 Linear Regulators

The linear regulators used are two LDOs (Low Drop Out regulators), selected to work with a minimum drop between Vout and Vin, reducing the converter efficiency losses. Particularly, they are reused IP (Intellectual Property) whole integrated into a silicon chip. For the 5 V linear regulator, the pass element is a P-MOSFET, which is integrated into the chip since this application considers loads of few Watts. The minimum voltage drop on the pass element is 300 mV to ensure good performance. Hence, the minimum output voltage of the DCDCB is fixed to 5.3 V. In both cases (linear regulators for 5 V and 1.65 V) the error amplifier is made by a P-type folded cascode stage plus an A-class output stage to drive the pass element and the internal reference is obtained through an integrated bandgap circuit. This type of linear regulator may have a stability issue that is typically overcome with the ESR (Equivalent Series Resistance) of the output capacitors. The ESR inserts a low frequency zero in the frequency response. This is why in literature electrolytic capacitors with high ESR are used. In this work, to avoid the use of cumbersome electrolytic capacitors, the Ahuja's compensation technique is used [59], introducing a polo-zero singularity with a feedback network in the folded cascode amplifier.

3.9 Gate drivers

Using MOSFET transistors with big size to reduce the ON-resistance increases the gate capacitance and so increases the switching losses, as shown in Eq. 3.9 and Fig. 3.12. In addition, big gate capacitance increases the switching time and so the losses due to no-zero switch resistance. To reduce this effect fast drivers are used to drive the switches. The driver for P-MOSFET transistors follows the principle showed in Fig. 3.17. The device M is the MOSFET that works as a switch, and the driver is in the green rectangle. When the OFF signal arrives, the M1 turns ON and thanks to a fixed current M2 is turned ON, therefore the gate of M is connected to its source and M is OFF. When the ON input signal arrives, M4 turns ON and thanks to a fixed current in the resistor Rb of Fig. 3.17, the gate-source voltage of M is fixed to keep it into saturation zone. For a high-speed discharge of the M gate capacitance, in the first phase, the gate of M is connected to GND. The discharge time depends on the potential difference between the initial voltage and the final voltage. When the gate-source voltage is below a threshold this effect is stopped and only the M4 device fixes the V_{GS} of M. The use of active drivers to impose the gate voltage is needed by rapid transient signals, of tens of Volts, present in the system. These signals can disturb the gate voltage through parasitic effects (mainly due to parasitic capacitors). However, this type of driver requires power also in steady-state. The two currents flowing in M1 and M4 are fixed in a range from 10 µA to 40 µA depending on the signal value present on the drain and source of the M P-MOSFET. The total static power required from all P-MOSFET drivers of the system is 390 µW.

The drivers used for the N-MOSFET transistors are designed using two not-gates (see Fig. 3.18) to buffer the gate of the MOSFET that works as a switch (M). The use of this simple driver is possible because all the N-MOSFET devices in the system have the source connected to GND. Increasing the MOSFETs size of the not-gates their ON-resistances decrease and so the speed to turn ON/OFF the M device increases. The

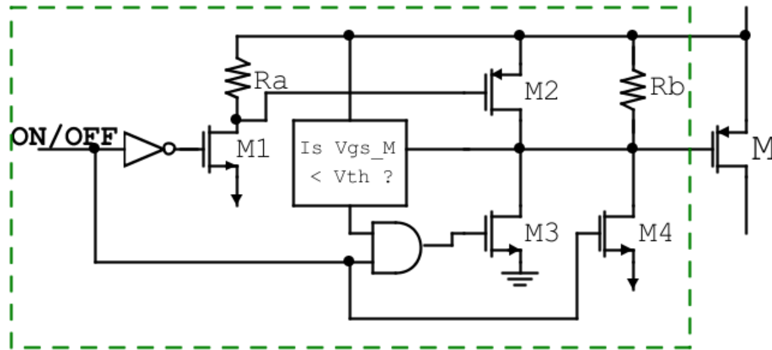

Figure 3.17: *P-MOSFET driver principle.*

second not-gate has a bigger transistor size than the first one to drive the big M N-MOSFET. In addition, the size of N-MOSFET of the second not-gate is about 20 times bigger than the P-MOSFET size because a stronger action to keep off M is required. The voltage swing on the M-drain amounts to tens of Volts in fast transients. This behavior can turn ON the N-MOSFET through the gate-drain parasitic capacitance. Hence, a low resistance path between the M-gate and GND is required.

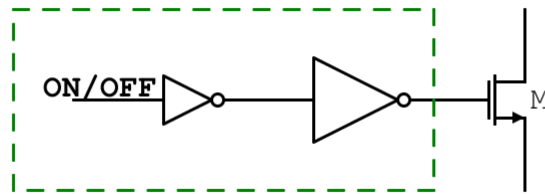

Figure 3.18: *N-MOSFET driver principle.*

3.10 Control Unit

The on-chip control unit in Fig. 3.2, starting from a 32 MHz ring oscillator, generates the switching phases. The control system plays an important role by changing the operative mode of the converter. Two nested control algorithms are implemented to control the desired output voltages: conversion ratio reconfiguration and SKIP-mode control. The conversion ratio reconfiguration technique drives each switch of the converter with a synchronous digital signal according to system condition and input voltage. These control signals change to obtain the different converter topologies and so the different values of VCR discussed in Tables 3.1, 3.5, 3.9 and 3.11. To this aim, integrated comparators are used. The SKIP algorithm works independently of the converter topology control. When the output voltage of each stage in the cascade of Fig. 3.2 is above a fixed value, the stage is frozen and the signals used to drive that stage stop following the usual timing. The SKIP control operates independently for each stage. Integrated comparators are used to detect out-of-range voltage values at the output of each stage. The effect of the SKIP algorithm is to limit the output voltage of each stage to use

lower voltage MOSFETs. The DC/DC converter chip has also a sleep mode to increase its efficiency. The current consumption in sleep mode is below 5 µA. The control unit receives start commands and sends acknowledgments and status/diagnostic flags to the external host through a digital serial interface (a custom interface in this chip version, which can be substituted with a standard link such as I2C or LIN).

3.11 IC Layout and Post-Layout Simulations

The multi-stage converter architecture discussed in the previous sections was realized in AMS 0.35 µm HV-MOSFET technology. Concerning other technologies for integrated design of power converters, the considered 2P/4M 0.35 µm technology offers transistors with a high V_{DS}, able to sustain up to 70 V in this work, but at low cost, e.g. 1/3 of the price vs. a 0.16 µm BCD for CMP or Europractice multi-project wafers.
Fig. 3.19 shows the layout of the chip. It is optimized to reduce the problems due to substrate injection currents. The HV components are placed at a distance above 100 µm each other. Each free space is filled with ground contacts to create low resistance paths, preventing latchup issues. The power MOSFETs, used for the switches, are made with tens of parallel HV-MOSFETs. The switches that required bulk drivers are created with finger-filled architectures to homogenize their effects. To simplify the direct bonding of the chip on the testing boards, PADs of size 0.77 mm * 0.5 mm are used.

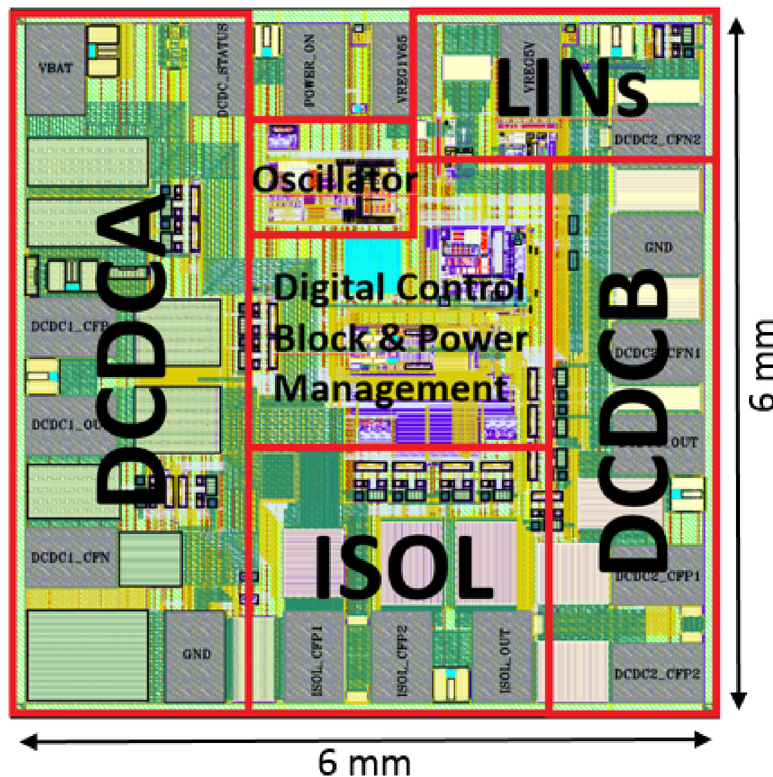

Figure 3.19: *Chip layout. The placement of the DC/DC converter stages is highlighted (ISOL stands for INSUL stage.)*

These PADs are much bigger than the PADs required by the current or voltage levels

present in the system. Therefore, the area of this prototype chip (6 mm * 6 mm) is bigger than the area needed in case of a series production of the chip using smaller PADs (an estimated area about 22 mm^2). All I/Os in Fig. 3.19 are protected against ESD problems with clamping circuits up to 4 kV. The digital and analog power buses are separated to reduce interference problems and all the ground paths are connect together only at the PADs to use their capacitive filter effects.
The whole SC converter can perform six conversion ratios in the full input voltage range. This allows reducing the input voltage value close to the V_{Xmin} target (6 V). Fig. 3.20 shows the post-layout simulation of the output voltage of each stage as a function of the input voltage. The simulations in Fig. 3.20 show the effects that the VCR reconfiguration and the SKIP control algorithm have on system behavior. The voltage peaks, in Fig. 3.20, are due to the VCRs changing while the flat behaviors are due to the SKIP control technique that limits the maximum output voltage of each stage. Each stage is influenced by the VCR of the following stage since the VCR affects its loading current value. Fig. 3.21 shows the contribution of each stage on

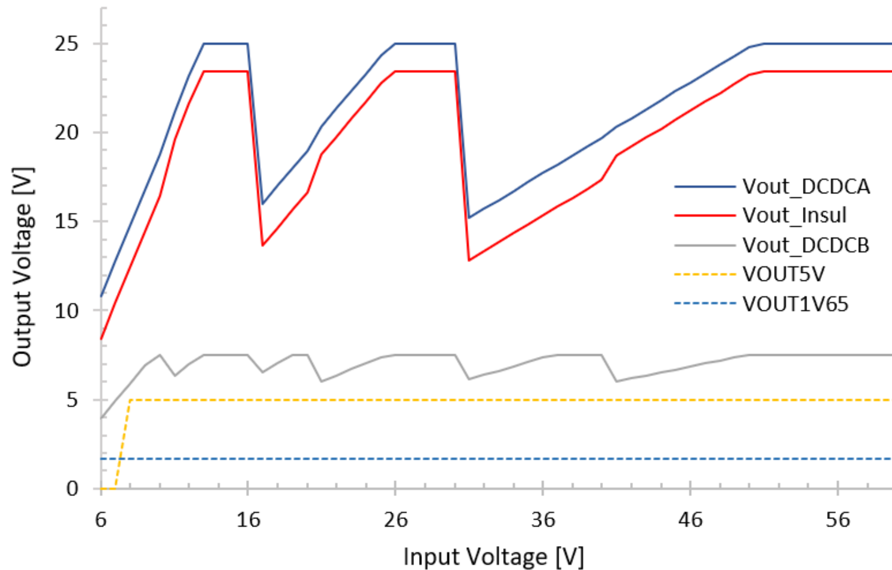

Figure 3.20: *Output voltages of all cascade stages as a function of input voltage considering 300 mA of load for 5 V output and 20 mA of load for 1.65 V output.*

power efficiency and the green line in Fig. 3.21 is the total power efficiency. The power efficiency of the SC stages is always in the range 80% to 99% and that of the 5 V linear regulator is from 67% to 84%. However, the combined contribution of the cascaded stages leads to an overall power efficiency from 40% to 64% along the wide input range from 6 V to 60 V. The 1.65 V linear regulator has a power efficiency always lower than 30% but its negative impact on the overall efficiency is mitigated by the fact that its load current is one order of magnitude lower than the 5 V linear regulator.

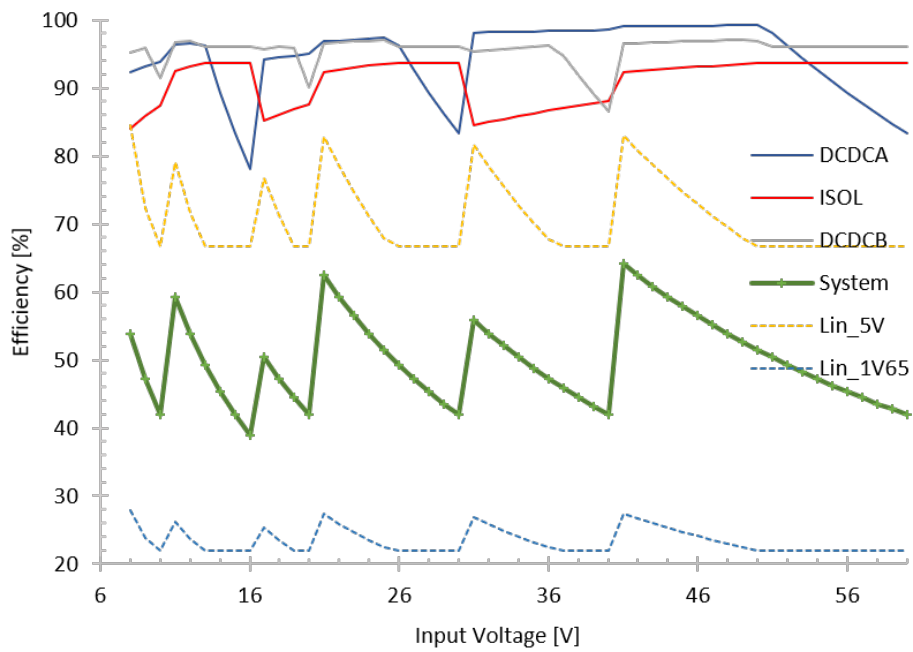

Figure 3.21: *Stages efficiency comparison. The data are extracted from simulations @ 300 mA of load for 5 V output and 20 mA of load for 1.65 V output.*

CHAPTER 4

High-Voltage and Fault Mitigation Design Techniques Verification

In this Chapter, the techniques for high-voltage management, discussed in Chapter 3, like the cascade architecture, the use of different switches typologies and the appropriate MOSFETs types choice for different voltage domains, are verified in the switching DC/DC converter measurements framework. Considering the growing requirement of ever-more integration, the measurement campaign was focused on the comparison between the performances extracted from a classical 2D configuration and an innovative 3D assembled structure of the inductorless DC/DC converter. The experimental verification was performed to verify how the high-voltage techniques, described in Chapter 3, affect the converter performances. In particular, measurements of line regulation, load regulation, efficiency, PSRR and output time response are performed on both DC/DC converter outputs.
Since the safety-critical requirements of the automotive and aerospace electrical circuits, particular attention is paid on the tests of the INSUL stage. Which aims to mitigate the effects generated by faults in the driving strategy of the SC circuits, and to face the faults generated by power system issues that force the converter to work outside its safe operating range (e.g. overvoltages in power buses).
Thermal measurements were performed to verify the capability of the DC/DC converter to work in rugged thermal conditions. A comparison between the performances of the encapsulated use of the inductorless DC/DC converter in a ceramic DIP-24 package and its suitable use in an innovative 3D stacked structure is also shown.

4.1 Testing Boards Implementations

In order to verify the techniques presented in Chapter 3 some testing boards with different converter assembled structures were developed:

- 2D structure in a dual-in-line (DIP-24) ceramic package, typically used in industrial and automotive products, see Fig. 4.1;
- 2D structure with the naked chip directly bonded on the board, see Fig. 4.2;
- 3D structure with a capacitor stacked on top of the naked chip, see Fig. 4.3.

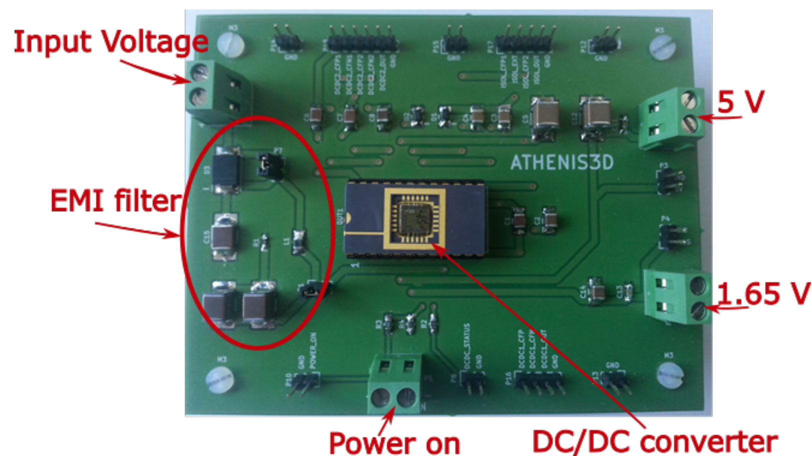

Figure 4.1: *Testing board with 2D converter IC in DIP-24 ceramic package.*

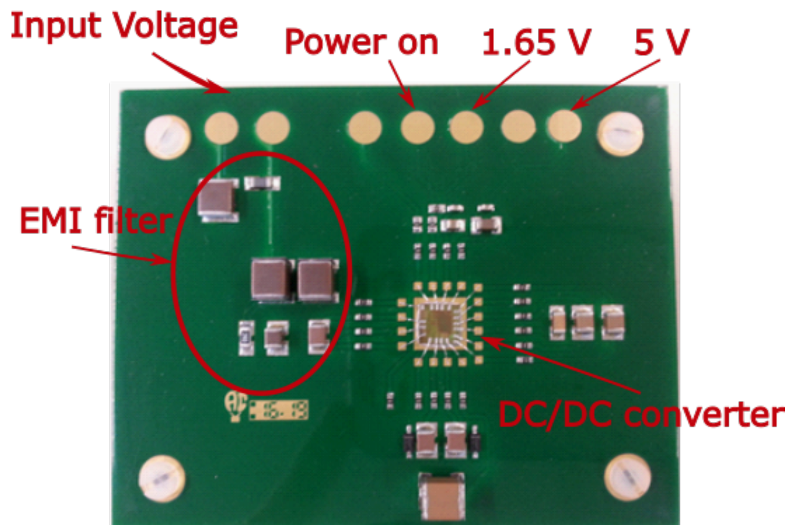

Figure 4.2: *Testing board with 2D converter directly bonded on the board.*

Fig. 4.1 shows the testing board with the chip encapsulated inside the DIP-24 ceramic package and the external components to test the converter. This board aims to test each stage of the converter and the whole converter to verify the techniques proposed in Chapter 3, taking into account packaging effects.

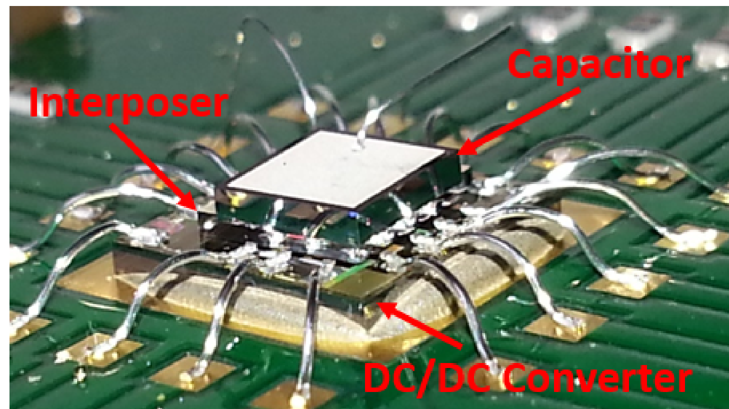

Figure 4.3: *Zoomed-in view image of the 3D converter structure.*

Fig. 4.2 shows the naked converter IC directly bonded on the board to avoid the thermal and electromagnetic shield effects of the package chosen. To exploit an ever-more integrate solution for space-saving (see Chapter 2), the DC/DC converter die is stacked with capacitors in the last solution presented in Fig. 4.3. This 3D configuration is obtained stacking, on the converter chip, the silicon TSV-based capacitors developed by Fraunhofer IISB [60] partner with trench technology, using an interposer layer to electrically insulate the two dies (DC/DC converter and capacitor), as shown in Fig. 4.3. The capacitor has top and bottom contacts. The top contact is directly contacted with a bonding wire while the bottom pin is soldered with the metal layer on top of the interposer, which is then contacted with another bonding wire.
On the testing boards in Figs. 4.1 and 4.2, a removable input filter, designed to reduce conducted EMI, whose detailed design is discussed in Chapter 5, is inserted with some measurement points.
In Table 4.1, the instruments used for the converter electrical characterization are listed. The converter is designed to have a sleep modality, which decreases the consumption power when its outputs are not required (below 5 µA for the wake-up sensing). This required the use of two power supplies during the test, a QXP1200L to generate the 48 V power bus voltage, and an E3631A to simulate the power-ON signal received by an ECU. When the power-ON signal is detected, the internal oscillator, the digital control block, and the converter stages are activated. A simple custom interface indicates at the ECU when the IC DC/DC converter has terminated the starting transient phase and the output voltages, 5 V and 1.65 V in this case, are regulated and meet the system constraints. The testing setup also includes a waveform generator 33120A useful for PSRR analysis, oscilloscope and a spectrum analyzer for time-domain signal analysis, a variable electronic load for load regulation tests and a temperature control system InTEST ATS-750-M-9 for thermal analysis.

4.2 Electrical Measurements

This section displays the main methods used to characterize the converter and verify the high-voltage techniques implemented inside, from an electrical point of view. In particular, the measurements are focused on the different results obtained from the

Table 4.1: *Instrumentation used for testing.*

Purpose	Instrument Code	Setting
Input Power Supplier	QXP1200L	6 V - 60 V
Waveform Generator	Agilent 33120A	2 Vpp 10 Hz - 15 MHz
Power-On Generator	Keysight E3631A	0V - 12 V
Oscilloscope	TDS 3054B, DSO7104A	-
Electronic Load	LD 300DC	0 - 300 mA on 5 V 0 - 20 mA on 1.65 V
Thermal Analysis	InTest ATS-750-M-9	-

classical 2D configuration in Figs. 4.1 and 4.2 and the innovative 3D structure in Fig. 4.3.
On the electrical side, not being a considerable difference between the configurations with and without the package, for better results readability, the electrical measurements made on the package configuration of Fig. 4.1 are not reported in this section.

4.2.1 Line Regulation

The line regulation measurement is performed in different conditions of the converter to discover all possible issues. The input voltage was swept from 6 V to 60 V, and the output current was set to a wide range of values, from 0 A to 250 mA for 5 V output and from 0 A to 20 mA for the 1.65 V output. Both 5 V and 1.65 V output voltages were measured. This test campaign allowed testing all configurations of interest in the converter operating with different VCRs. Figs. 4.4 and 4.5 show the line regulation measurement on the 5 V output and on the 1.65 V output, respectively. A line regulation reduction is shown on the 5 V output for low-voltage input values and currently higher than 100 mA. For the 5 V output and 250 mA load, a slight voltage drop appears with 16 V input voltage. This effect is more highlighted in the 3D converter test in Fig. 4.6. Indeed, for the 5 V output, the line regulation shows a voltage drop of about 0.5 V for 16 V input voltage and 250 mA loads. This is due to an increment in the bonding resistance in the 3D structure. This voltage drop can be fully recovered by proper tuning, in a calibration phase, the threshold of the ADC used to decide the VCR. From a comparison with Fig. 3.20 is observable that this voltage drop is generated by the threshold used by the control block to discriminate the VCR = 1/2 and VCR = 1 of the DCDC1 stage. Hence, an increment of this threshold is required in the next chip version.

4.2.2 Load Regulation

For the load regulation, the two output voltages are measured with various loads and input voltages. This test is widely used in literature also for diagnostic purposes [61]. The output load current is swept from 0 mA to 20 mA for 1.65 V output and from 0 mA to 300 mA for 5 V output. Figs. 4.7 and 4.8 show a maximum variation, compared with the nominal voltages (5 V and 1.65 V), below 2% for every test conditions. Highlighting that the two output voltages can be used to power sensors and ECUs, which require a low-voltage-controlled power supply. Fig. 4.9 shows the load regulations of the 5 V and 1.65 V nominal output voltages for the converter in the 3D structure. The

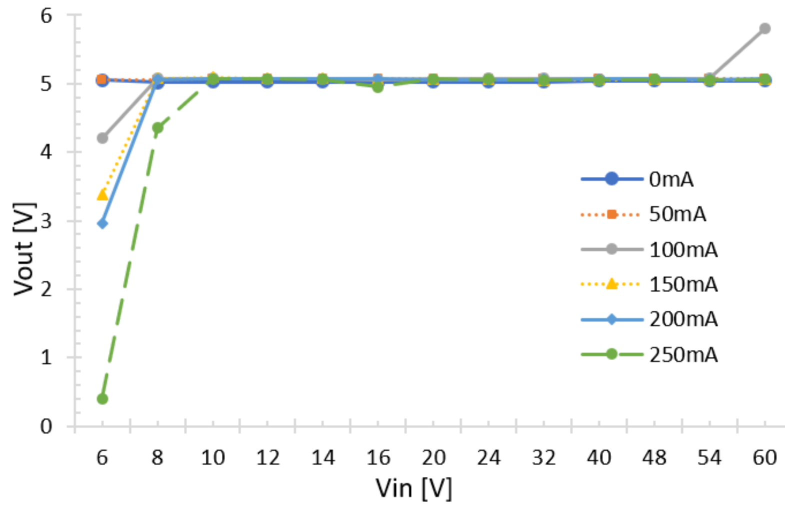

Figure 4.4: *5 V output line regulation results.*

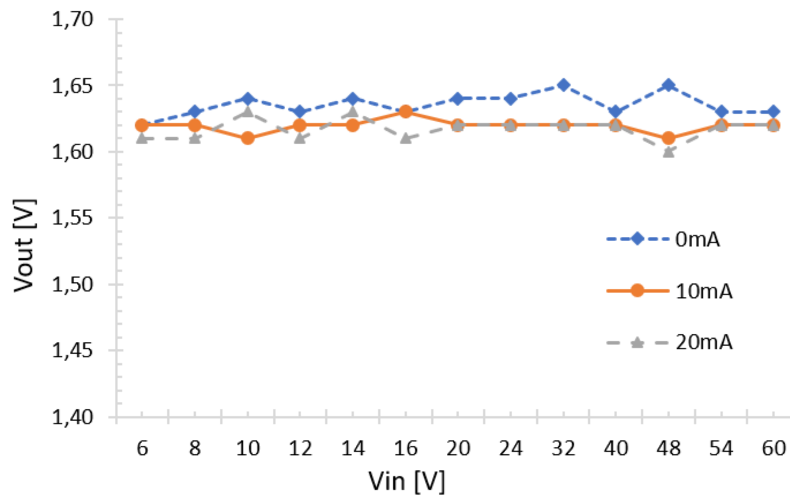

Figure 4.5: *1.65 V output line regulation results.*

measurement, performed with 48 V input voltage, not highlight significant performance differences between the 2D and the 3D structures.

4.2.3 Efficiency

The efficiency is calculated with the classical ratio between output power and input power measured for both the 2D and 3D structures. The efficiency of an SC converter is strictly related to the input voltage, as shown in Figs. 4.10 and 4.11, where every peak represents the changing of the conversion ratio. The mean efficiency value, of this converter, is lower than the mean achievable with an inductor-based converter. This is also due to the presence in the proposed IC of the two integrated LDOs. The output voltages of the state-of-the-art switching converters are affected by ripple, indeed, in most applications, off-chip linear regulators are used in cascade to the switching converter to decrease this issue. This solution, decreases the global efficiency of the converter, as

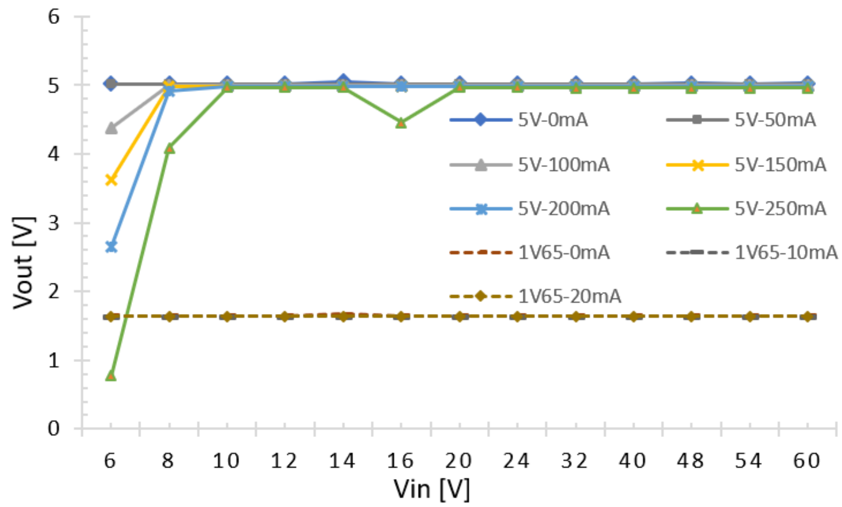

Figure 4.6: *Line regulations (5 and 1.65 V) for the 3D structure.*

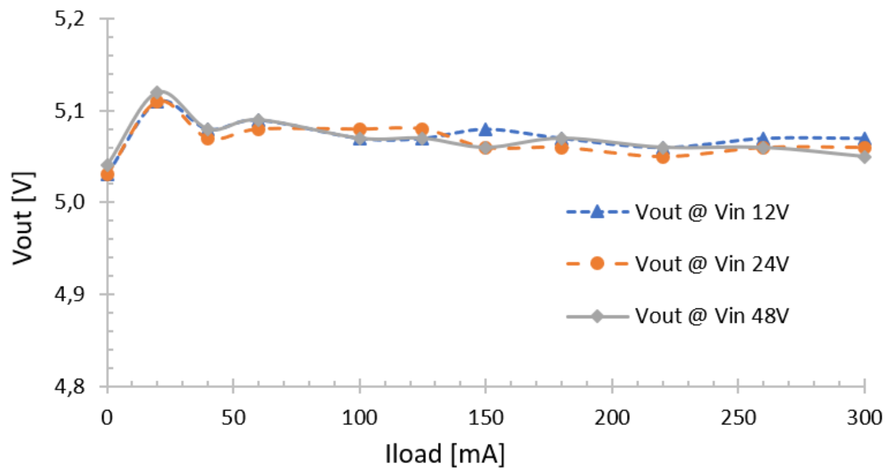

Figure 4.7: *5 V output load regulation.*

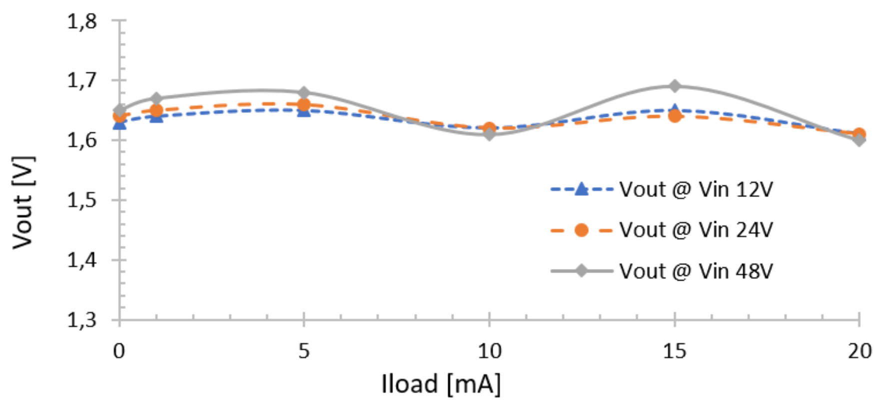

Figure 4.8: *1.65 V output load regulation.*

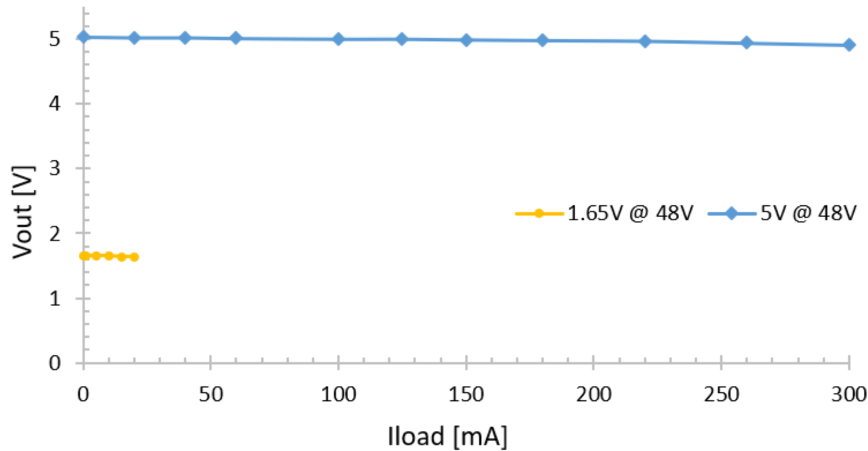

Figure 4.9: *Load regulation of the two outputs for the 3 D structure.*

happened for the integrated solution analyzed in Chapter 3.
The similar efficiency results of the 2D and 3D structure in Figs. 4.10 and 4.11, respectively, show the feasibility of the compacted 3D solution approach. In both result sets an efficiency values increment for higher load currents is explained with a grater load power requirement with respect to the power consumed by the auxiliary blocks (such as the oscillator, switch drivers, control system, and power management), which absorb power independently of the load currents.
Fig. 4.12 shows an efficiency comparison between the IC converter implementing the techniques discussed in Chapter 3 and the LTC3245 SC converter (the only commercial SC converter that is able to operate in the target voltage range, at the best of the author's knowledge) [62]. As shown in Fig. 4.12, the LTC3245 shows three peaks of high efficiency located at a lower input voltage range (below 15 V). Instead, the high-voltage techniques implemented in the target IC converter ensure a higher efficiency for a wide input range. The dashed line in Fig. 4.12 represents the efficiency of an ideal linear converter in the same input voltage conditions. The efficiency gap between the proposed converter and a pure linear converter increases at high input voltage levels. The proposed converter is a good compromise between classic inductor-based switching converters and linear converters.

4.2.4 Power Supply Rejection Ratio

The PSRR is measured with two different setups. The first is the classical approach where a low amplitude variable frequency signal is added to the input pin of the DC/DC converter. The second setup is realized to simulate the real operative condition in an automotive environment.

Classical Setup

Using a waveform generator (listed in Table 4.1), a sine signal with an amplitude of 2 Vpp is added to the input voltage and the output voltage ripple is measured, neglecting the ripple due to normal operation of the converter. The graphic in 4.13 shows the PSRR, calculated using the Eq. 4.1, as a function of the frequency.

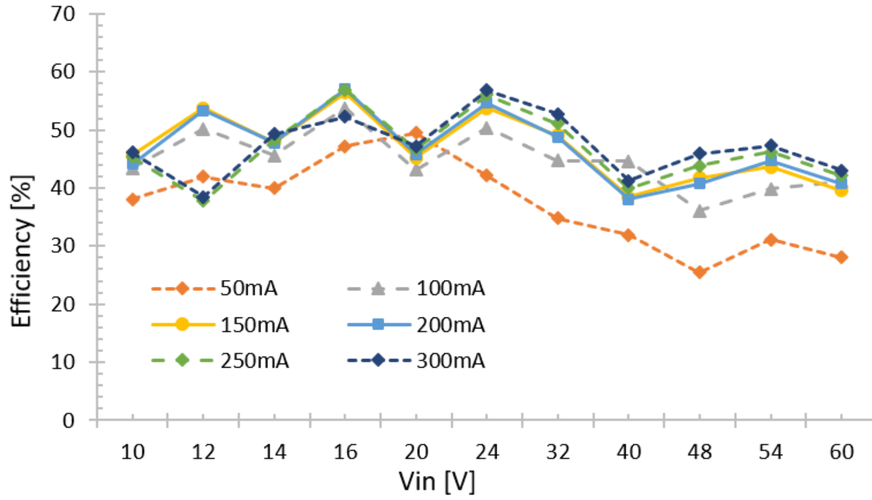

Figure 4.10: *Efficiency results of the 2D structure.*

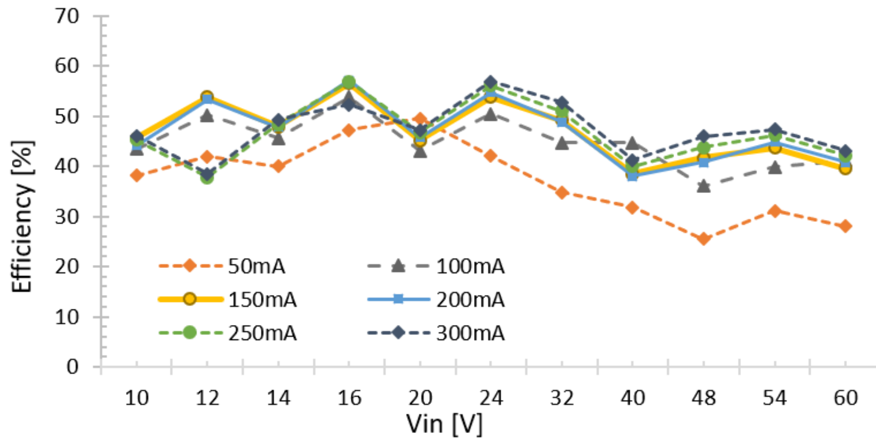

Figure 4.11: *Efficiency results of the 3D structure.*

$$PSRR(dB) = 20log\frac{V_{pp-out}}{V_{pp-in}} \tag{4.1}$$

Automotive-Aerospace Vehicle Setup

This is a test to simulate the behavior of the converter in a real vehicle environment. The frequency of the electric engine in hybrid/electric vehicles changes with the velocity but it is around 300 Hz in normal condition, hence a sine disturb of big value (10 V peak to peak) at that frequency is added to the input voltage. This is performed using a waveform generator and an amplifier, designed to operate at high voltage with an offset up to 45 V. The results in Table 4.2 highlight that the converter has -60 dB PSRR, for wide input voltage range and typically automotive-aerospace disturb frequency.

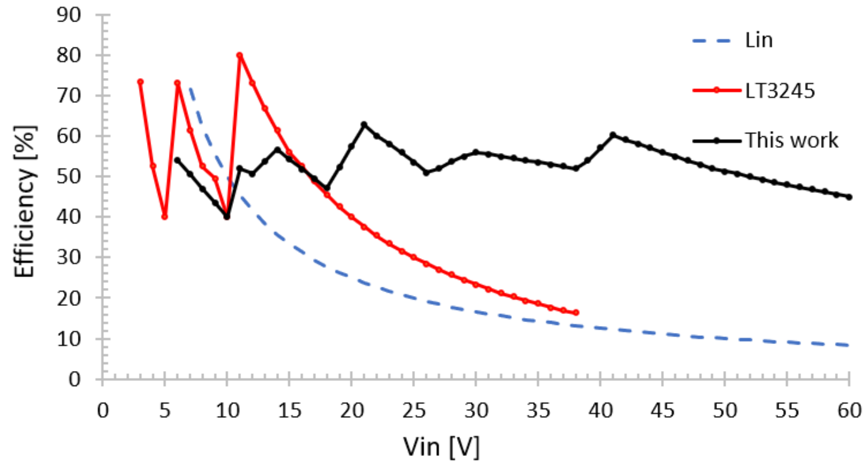

Figure 4.12: *Efficiency comparison.*

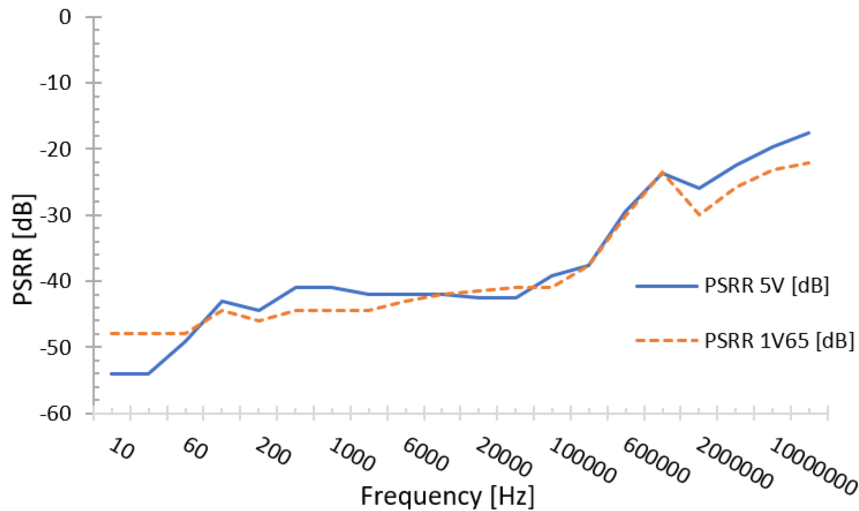

Figure 4.13: *PSRR results (load currents: 300 mA at 5 V and 20 mA at 1.65 V).*

Table 4.2: *PSRR results in automotive conditions.*

Battery Voltage	Input Disturb	Output Ripple	PSRR
45 V	10 Vpp	10 mVpp	-60 dB

4.3 Insulator Test

When the converter works in a harsh environment with high electromagnetic fields and high temperature, the control system or some switches can fail. This failure can damage the converter itself and the loads supplied by it. The DCDCA is the stage most exposed to problems related to over-voltages and substrate charge injection for the high-voltages managed (swings of tens of volts in few microseconds).
If a failure in the control system occurs or an over-voltage, above 75 V, is applied at the converter, some first stage switches can fail to create unwanted paths. In particular,

the blue solid lines in Fig. 4.14 represent the paths that short the high input voltage to ground, saving the low voltage loads. Instead, the red line in Fig. 4.14 represents the path from input to output that can damage the output loads. Without the INSUL stage, the charge following the red line goes toward the output because the switches of the DCDCB stage can not sustain such high voltage levels. As reported in Chapter 3, the MOSFETs used for the DCDCA switches can sustain a voltage above 70 V, instead, the maximum voltage sustained by the DCDCB switches is limited at 30 V.

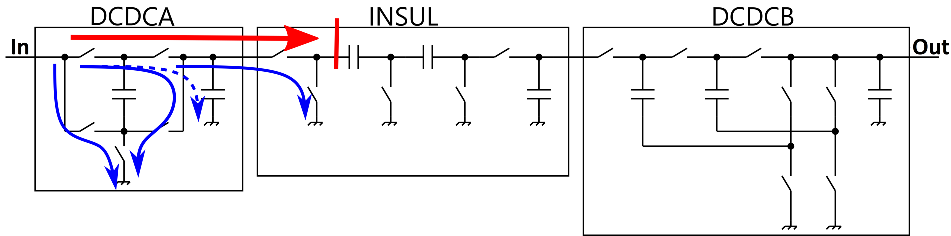

Figure 4.14: *Converter model with the INSUL stage between the two converters stages.*

The insulator works using two techniques: the first is used when the INSUL input voltage is below 50 V (breakdown voltage of the INSUL MOSFETs), and the second is used for higher voltages. The first technique is based on the SKIP control algorithm, which keeps the INSUL output voltage below 28 V. The INSUL output voltage is measured and when it achieves 28 V value, the INSUL stops its switching, preventing that voltages above 28 V damage the DCDCB stage. In this condition, if the DCDCA driving error is a sporadic event, the converter can still work. In the case that the INSUL input voltage exceeds 50 V, some switches of the INSUL stage can fail. However, thanks to series capacitors the high and low-voltage domains are separated. (The red path is interrupted by the two series capacitors as in Fig. 4.14). In addition, if an AC high-voltage is applied to the converter, the series capacitors can be bypassed, but the buffer capacitor of the DCDCA has value three times higher than the value of the series capacitors. Therefore, the buffer capacitor of the DCDCA stage low-pass filters the AC voltage to GND (blue dotted line in Fig. 4.14).
In the worst case, if there are no "blue" paths because the switches are open failed, the input voltage is not shorted to GND. In such a case, the load safety is ensured by the series capacitors dielectrics, which have to be chosen to sustain the maximum voltage used in the system. For this application, the used capacitors are able to sustain 100 V with an insulation resistance of 151 MΩ. Therefore applying 100 V at the input, there are only 662.25 µA across the insulator.

4.3.1 Overvoltage Fault Test

Fig. 4.15 shows the breaking test of the INSUL stage. The first stage (DCDCA) was removed and the input voltage was applied at the insulator. As shown in Fig. 4.15, the output voltage follows the input one until 28 V (normal working condition), then the output voltage is kept constant by the SKIP algorithm. It is worth noting that in this condition, the DCDCB and the LINs are still working, so if the DCDCA fails disappears the converter returns to work in nominal conditions. Also, the DCDCB uses the SKIP algorithm, to limit its output voltage at 5.8 V (yellow line in Fig. 4.15), thus reducing

the power dissipated on the pass transistors of the two linear regulators. When the input voltage exceeds 54 V, a failure in the INSUL stage appears and the output voltages (5 V and 1.65 V) fall down. Thanks to series capacitors, the high voltage is not forwarded to the loads.

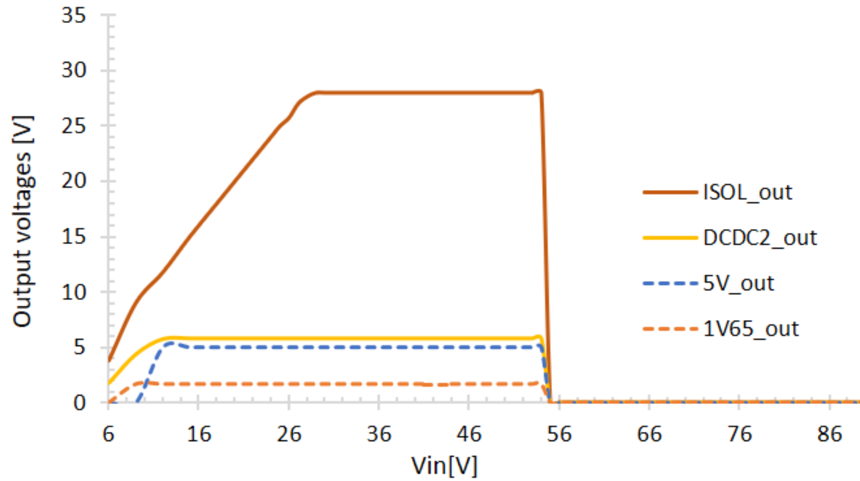

Figure 4.15: *Failure test of the INSUL stage.*

4.3.2 Single Event Effect Fault Test

The insulator stage can prevent damaging effects generated by failures in the control algorithm of the SC stages. For example, considering the high-voltage managed by the DCDCA, if the converter input voltage is 25 V, the DCDCA should work with unitary VCR and the DCDCA output should ideally be 25 V (see Table 3.1). Referring to Fig. 3.9 and to Table 3.5, both unitary and double VCRs have the same first phase but the second phase differs for turning on the switches S1 and S3 for VCR = 1 and for turning on the switches S1 and S4 for VCR = 2. If a fault appears with 25 V input voltage and in the second phase the switch S4 is activated, instead of the switch S3, the DCDCA works in step-up modality, hence 50 V is generated at the DCDCA output. Without the INSUL stage, such voltage can easily damage the DCDCB stage and the load.
Even easier to appear could be the fault of the switch S1 (see Fig. 3.9) in step-down modality. For instance, if 48 V is applied to the converter, it operates with VCR equal 1/2, but if the switch S1 is turned on also in the first phase (see Table 3.5), the 48 V is forwarded through following DCDCB input (in case the INSUL stage is not implemented), damaging the 30 V MOSFETs. It is guessed that a fault in the driving strategy on the DCDCA can easily damage the DCDCB and the loading devices. Hence, thanks to the techniques implemented in the INSUL, the faults in the control algorithm can be mitigated.
In the optics to use the inductorless DC/DC converter in aerospace environments, considering the compatible power bus voltage range, which is from 28 V to 50 V for satellite, and the strategical importance to have a compact device, see Section 2.2, the classic sources of faults are the SEE (Single Event Effect) generated by high-energy particles interaction. As will be detailed discussed in Chapter 6, the particle energy transferred to

the silicon creates electron-hole pairs that could be able to flip the data stored in digital cells, hence it can modify the driving strategy of the proposed converter. Therefore, the fault-tolerant property of the inductorless insulating stage was experimentally tested using heavy ions tests at INFN National Laboratories of Legnaro (PD). The IC converter was hit by three types of ions with different LET (Linear Energy Transfer) to reproduce faults in the driving strategy. In order to perform the test, the DC/DC converter was placed in a vacuum chamber and remotely controlled. Its 5 V output, which is the most sensitive output, was measured to detect faults. No effect was registered during the test performed with Oxygen (O^{16}) with LET = 3.16 Mev·cm^2/mg, hence tests with higher LET were then performed. Fig. 4.16 shows the failure test of the INSUL stage when it was exposed to Si^{28} with LET = 8.8 Mev·cm^2/mg and a flux equal to 20 kions/s. The results show some voltage drops on the 5 V output. The errors generated in the driving strategy of the SC stages converter have created some faults that have discharged the buffer capacitors, decreasing the output voltage. The faults were generated and recovered by the DC/DC converter in a few milliseconds. To be noticed that thanks to using the INSUL stage no overvoltage phenomena occurred during the test, hence the loaded devices were not damaged.

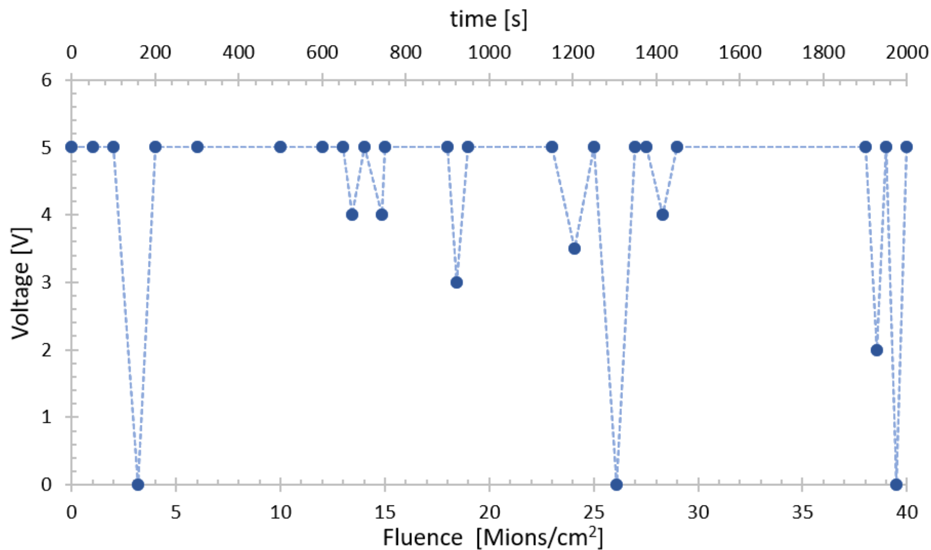

Figure 4.16: *Failure test of the INSUL stage using Si^{28} with LET = 8.8 $Mev \cdot cm^2/mg$ and flux = 20 kions/s.*

The test performed with a higher LET ion (Ni^{58} with LET = 28.4 Mev·cm^2/mg), shown in Fig. 4.17, displayed greater effects on the output voltage with respect to the previous test. All the voltage drops fall up to zero voltage, highlighting the heavy effect that this ion has on the IC converter. Furthermore, at the same test time, a higher fault rate was recorded even though the ions flux was four-time lower. However, thanks to the fault mitigation techniques implemented in the inductorless insulator stage no overvoltage appeared at the IC converter output. The purpose of this test was only to verify the insulation techniques of the INSUL stage. The DC/DC converter fault rate can be improved by implementing SEE tolerant techniques in the digital control block, such as the classic triple redundancy. Therefore, the use of the proposed INSUL stage in

couple with digital radiation-hard techniques for the driving intelligence could create a SEE tolerant DC/DC converter suitable for aerospace applications.

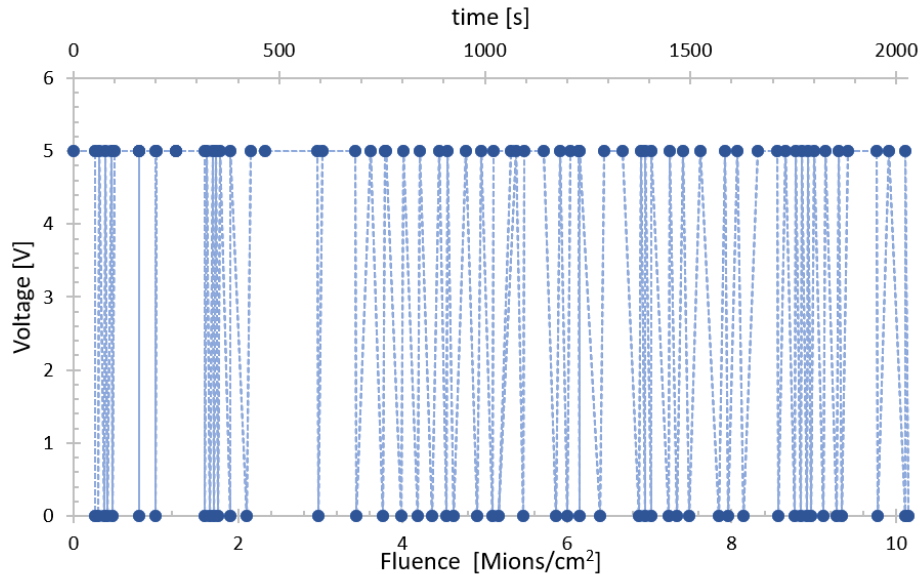

Figure 4.17: *Failure test of the INSUL stage using Ni^{58} with LET = 28.4 $Mev \cdot cm^2/mg$ and flux = 5 kions/s.*

4.3.3 Total Ionizing Dose Effects

In Section 2.2, the fundamental role played by the cumulative radiation in a space environment was highlighted. The electronic devices for NASA's Europa Clipper mission were designed to sustain a total dose of 300 krad. However, the dose value collects by a spacecraft is strongly correlated to the mission.
The TID test of the converter was performed using the X-ray Seifert RP 149 machine at the X-ray facility of INFN Padova. The bare die of the DC/DC converter was placed under the X-ray beam and was remotely controlled by measuring the 5 V output. The converter showed to proper work up to 43 krad; after that TID level, the measurements performed on the 5 V output showed a decreasing value up to zero.
The post-irradiation converter measurements highlighted that the DCDCA stage was the heavier affected by cumulative dose. This stage, having to sustain the highest voltages of the converter, uses the 70 V MOSFETs to implement the switches. The lateral diffusion of these devices, used to sustain high voltages, is covered by thick field oxide, which, as will be displayed in Chapter 6, is particularly sensitive to radiation. The positive charge collected in the field oxides changes the doping of the lateral diffusion increasing its resistance, see Fig. 4.18. This increment in the switches resistance appears in all the LDMOS used but is more evident in the DCDCA for the highest voltage MOSFETs used and for the implementation of the diode back-to-back configuration with two series MOSFETs (see Fig. 3.7).
In [63] the TID levels, extracted by simulations, for a CubeSat satellite in slow transition from the Earth to the Moon are reported. In particular, the results show that for low transfer with a thrust force of 0.0005 N/kg, approximately 8-26 krad (Si) TID should

be expected depending on the position within the spacecraft. For a faster transfer to the Moon with a thrust force of 0.001 N/kg, the expected range of the TID became 4–14 krad (Si). Therefore, the radiation-tolerant property of the proposed converter makes its use suitable for the Earth to the Moon transition scenario.

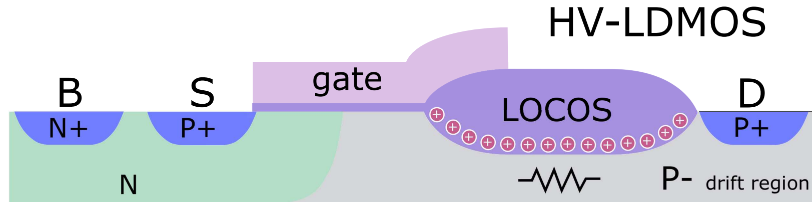

Figure 4.18: *HV-LDMOS section with charge trapped in the field oxide. This positive charge increase the resistance of the drift path.*

4.4 Thermal Measurements

A thermal measurement campaign was performed to characterize the behavior of the converter at different working temperatures.

4.4.1 Performances at Different Environment Temperatures

The temperature-controlled environment measurements were performed using the advanced temperature source InTEST ATS-750-M-9 (see Fig. 4.19). The ambient temperature was swept from -25 °C to 100 °C using 25 °C steps, and the electrical performance of the converter was measured. Fig. 4.20 shows the load regulation of 5 V output for six different working temperatures. In the range from -25 °C to 100 °C, the output voltage shifts from 5.06 V to 4.96 V with a mean voltage/temperature coefficient of 0.212 mV/°C. Fig. 4.21 shows the load regulation of the 1.65 V output. The output voltage shifts from 1.655 V to 1.637 V with a mean voltage/temperature coefficient of 0.33 mV/°C. Fig. 4.22 shows the efficiency variation for different working temperatures. Fig. 4.22 highlights that the efficiency shifts only for some input voltages: 8 V, 16 V, and 32 V. These voltages are near to the VCRs thresholds of the first stage converter. Therefore, this test allowed to understand that the first stage is the most influenced by temperature changes.

4.4.2 Thermal Profile of the Converter

The efficiency of the converter is about 50%, so at the maximum load the converter needs to dissipate nearly 2 W. This increases the temperature of the converter and the temperature of the other systems placed close to it. The converter was put in a controlled environment at 27 °C in still air and the temperature was measured on the converter top, using an infrared thermometer. The increase in temperature depends on the thermal resistance between the die and the environment.
Therefore, this test is done for the three structures presented in Section 4.1 in Figs. 4.1, 4.2 and 4.3, to compare different power dissipation performances. Fig. 4.23 shows the temperature measurements on the top of the naked die in different working conditions. Four input voltages are used because changing the VCRs the switching topology

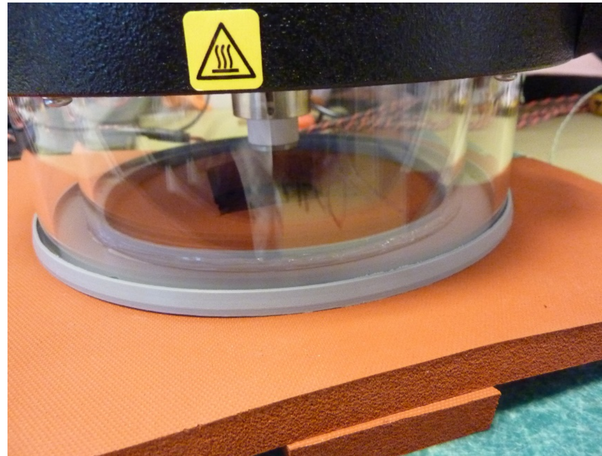

Figure 4.19: *Temperature control system (InTEST ATS-750-M-9).*

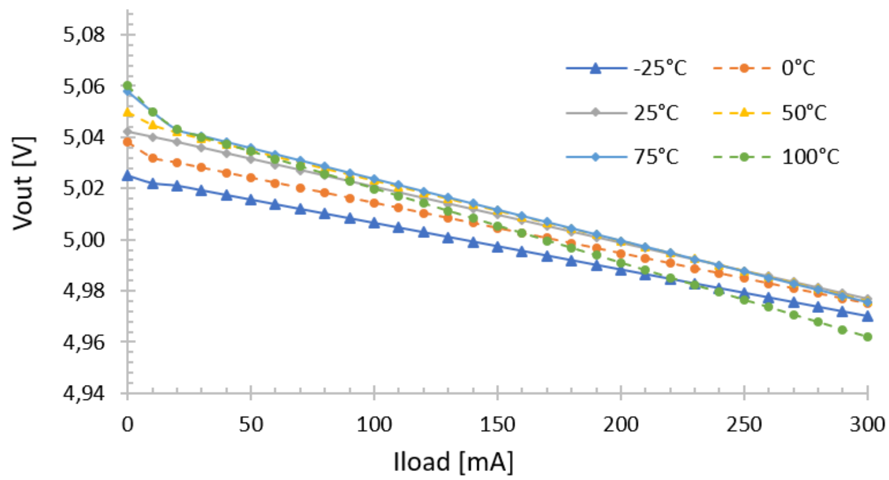

Figure 4.20: *Thermal variation of 5 V load regulation at Vin = 48 V.*

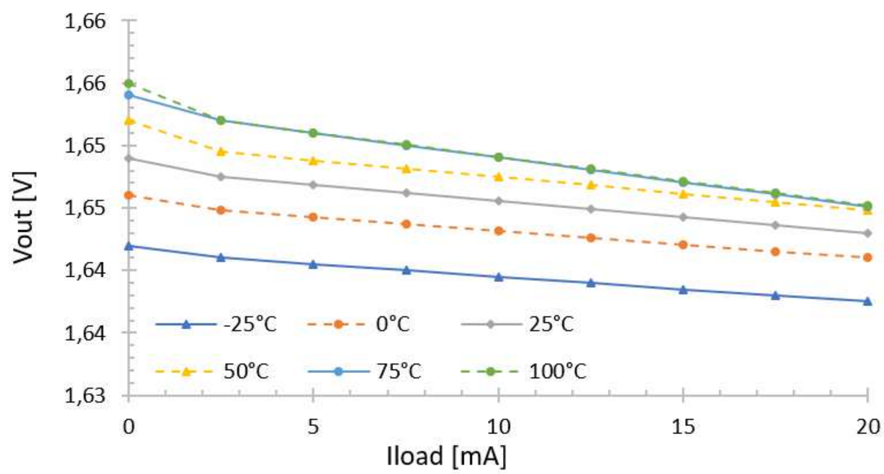

Figure 4.21: *Thermal variation of 1.65 V load regulation at Vin = 48 V.*

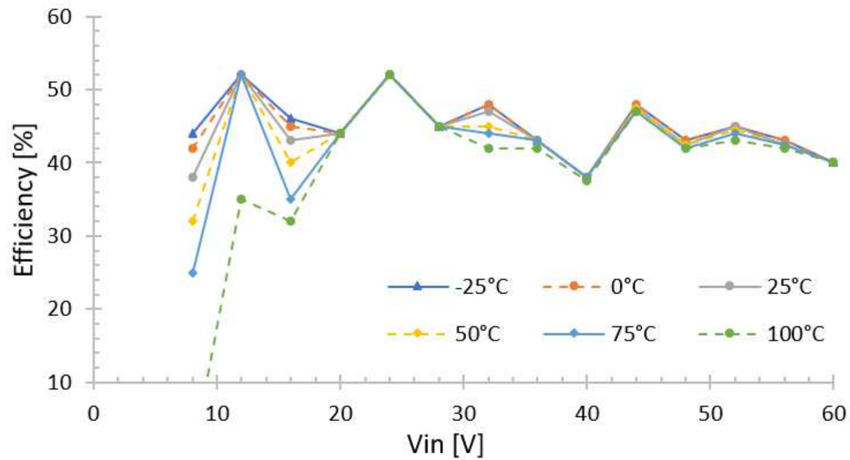

Figure 4.22: *Thermal measurement. Efficiency results at Iload = 300 mA.*

changes. Increasing the load current, the temperature increases because of the dissipated power increases. In Fig. 4.23, the temperature of the 3D structure (naked chip plus capacitor stacked on top) is few degrees lower than the 2D structure (only naked chip). This is justified by the fact that the temperature measured with the infrared thermometer is that of the stacked capacitor, which is lower than that of the converter die. Fig. 4.23 shows the temperature profiles of the chip packaged in a DIP-24 ceramic package. The values are close to the temperature measured with the naked chip. In this case, the maximum load current is exceeded 100 mA above. The proposed converter, also in case of current overload, has a working temperature within its safe operating area.

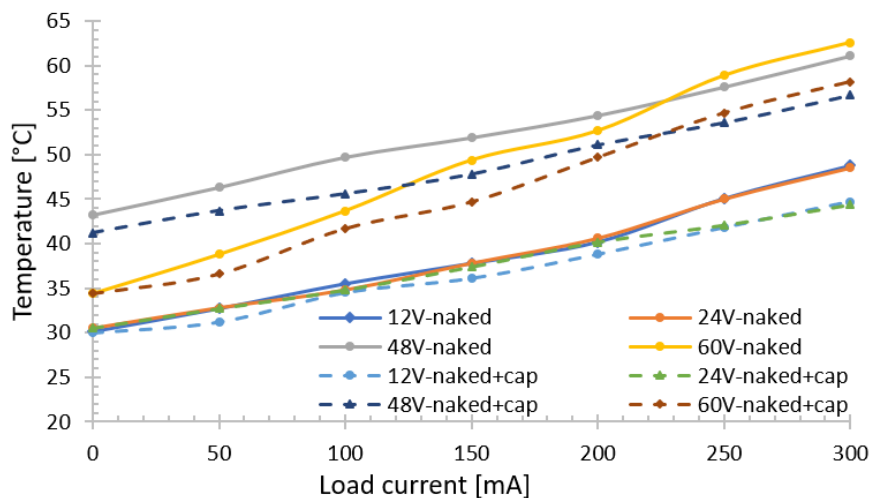

Figure 4.23: *Temperature profiles of the naked chip in 2D and 3D structures.*

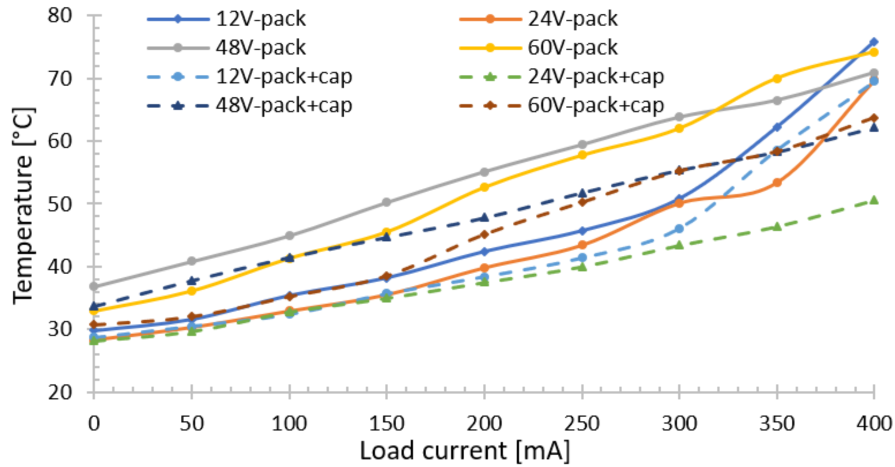

Figure 4.24: *Temperature profiles of the packaged chip in 2D and 3D structures.*

4.5 Electrical Comparison to State-of-the-art

When compared to the state-of-the-art, see comparison in Table 4.3, versus converters from industry [51, 62] or academia [64–67], the DC/DC converter proposed in this work (in 2D or 3D version) stands for the following aspects. At the best of the author's knowledge, this is the first work aiming at a fully integrated solution for 48 V DC/DC converters ensuring regulation performance in a wide range from 6 V to 60 V. The state-of-the-art is dominated by architectures using multiple converters (e.g., 48 V–12 V, 12 V–5 V, and then point of load converters from 5 V to the low-voltage output), which leads to cumbersome and costly systems. Moreover, most converters at state-of-the-art [14, 68–72] are based on discrete solutions mounted on a board, using off-chip discrete power devices and cumbersome inductors and transformers, e.g., up to 12 μH in [68]. In [70] and [72], a first transformer-based LLC converter is used for 48 V–12 V regulation, and then a multiphase buck converter with 200 nH inductors is used to define a 1.8 V output load. Discrete GaN devices are used as power switch in [70], and also in the 48 V–12 V in [71] and the 48 V–2 V in [64]. With respect to known inductor-based converters, regulating up to 60 V, e.g., PT4467 in [51], with an efficiency of 70% for load currents below 1 A, this design allows for a printed circuit board (PCB) saving of a factor ×5. Indeed the PCB of this converter can be manufactured with about 2.5 cm^2 instead the PT4467 requires at least 13 cm^2. Besides inductors, the PT4667 requires also an off-chip 5 mF capacitor. Moreover, the inductor-based PT4667 48 V switching converter in [51] needs at least 36 V input. This work instead presents a new approach that exploits SC together with integrated passive devices and integrated power switch to achieve a fully integrated implementation of a direct 48 V DC/DC converter. By avoiding the use of inductors/transformers, the proposed design also enables future system-on-package implementations with an area occupation below 1 cm^2, one order of magnitude lower than [51], where trench capacitors are integrated into passive interposers, assembled in 3D fashion with the DC/DC converter chip. Instead, integrated converter solutions that at the state-of-the-art exploit the SC approach are often limited to voltage levels of few volts at input and output sides. For example, an integrated

converter with 10 µF and the 10 µH discrete passives are proposed in [73], a 2.5 V or 200 mA load is regulated from an input 1.8 V source. Similar work is proposed in [74]. Hence, they are not able to sustain a wide input voltage range, from 6 V up to 60 V, such as the proposed work. Indeed, they are typically used or in step-down mode to regulate a 5 V (produced by other converters) to a low-voltage input, or to boost a low-voltage source in energy harvesting applications or inside flash memories. Moreover, in the proposed work, the INSUL stage avoids direct electric connection between input and output, another new feature versus state-of-the-art integrated SC converters. For example, with respect to other SC converters, the proposed design sustains a wider input range, from 6 V to 60 V, while the LTC3245 DC/DC [62] converter, addressing similar load voltage and currents (250 mA, 5 V), is limited to max 38 V and is missing an isolation stage. Other works are limited at a maximum input voltage of 42 V, see [55]. With respect to the LTC3245, the proposed design achieves better efficiency for inputs above 18 V. The voltage change of this work, around the regulated output, is ±30 mV on a range of 400 mA, while for the SC LTC3245 converter is ±60 mV on a range of 250 mA. The proposed design achieves a PSRR of -60 dB, thanks to on-chip linear converters at the last stage of the cascade. Other state-of-the-art switching converters such as [62] and [51] do not declare their PSRR and need an off-chip LDO regulator to reach values comparable to this design. Direct 48 V to low-voltage converters are proposed in [65] and [66]. In [66], a wide input range of 18 V-54 V is regulated in a 1.2 V, for a power load of about 10 W, using an inductor-based step-down converter with a switching frequency of 100 kHz, a 1000 µF discrete capacitor, and a 60 µH discrete inductor. Other direct 48 V to few volts converters are proposed in [64] and [67]. In [64], a seven-level flying capacitor multilayer converter is presented, which regulates a 48 V input supply to a 2 V output, with a load current from 1 A to 10 A. The converter in [65] uses an off-chip GaN powertrain. In [67], a monolithic converter is implemented in 180 nm high-voltage BiCMOS technology. A 48 V input supply source is regulated in a 5 V output with 50 mA load, 10 MHz switching frequency, and 500 nH output inductance. Peak efficiency of 80.9% is achieved at 12 V input.

Table 4.3: *Comparison to the state-of-the-art, *3 V to 60 V.*

	This Work	[51]	[62]	[64]	[65, 66]	[67]
Type	SC+linear	Inductive	SC	SC	Inductive	Inductive
In-Out insulation	Yes	Yes	No	Yes	Yes	N/A
Input range [V]	57*	39	35	N/A	36	N/A
PSRR [dB]	-60	Off-chip LDO needed			N/A	N/A
Output voltage [V]	1.65 / 5	3.3 / 5	5	2	1.8	5
Max load current [A]	0.4	30	0.25	10	10	0.005
Efficiency peak [%]	63	86	81	55 to 85	60 to 90	N/A
Stand-by current [µA]	5	5000	4	N/A	N/A	N/A
Temp. range [°C]	-40, 150	-40, 100	-40, 150	-40, 150	XX	XX
Note on integration	See [a]	See [b]	See [c]	See [d]	See [e]	See [f]

[a] Partially 3D integrated capacitors
[b] Discrete passives (5 mF capacitor needed)
[c] Discrete passives (two 1 µF and 10 µF capacitors needed)
[d] Discrete GaN and passives (seven 4.7 µF capacitors and 1 µH inductor needed)
[e] Discrete MOSFETs and passives (eight 10 µF and 1 mF capacitors, 60 µH and 9.39 µH inductors needed)
[f] Discrete passives (500 nH inductor and 10 µF capacitor needed)

CHAPTER 5

Electromagnetic Interference reduction techniques, Development and Verification

In the trend of ever-more integration of different functions in a reduced area, the ICs should work side-by-side with other ICs. The unwanted interaction between different systems should be kept under control. This is easily suitable for electrical signals flowing in the conductive path. Instead, generation and control of electromagnetic disturbance still be one of the major electronics challenges, as discussed in Chapter 2 for automotive and aerospace environments. This chapter presents the design and verification of electromagnetic interference reduction techniques for switching mode power supplies (SMPS) with low switching frequency (such as 90 kHz in the practical example of the 48 V DC/DC converter analyzed in Chapter 3). The switching approach allows increasing the DC/DC converter efficiency, but, on the other side, it makes more challenging the control of EMI emissions. The state-of-the-art methods exhibit a tendency of splitting the design process into two loosely coupled components: the design of the converter [21, 75, 76] and the design of the techniques to reduce EMI [19, 20]. This leads to oversize EMI filter components, thus increasing the size, weight, and cost of the power converter solutions.

5.1 Front-end and DC/DC Converter Models

To understand the electromagnetic effects of the DC/DC converter, and of the other front-end elements, it is necessary to model them, as shown in Fig. 5.1. The front-end consists of an equivalent model of a battery, a line impedance stabilization network (LISN), the equivalent model of the cable used for connecting the converter with the battery, and the EMI filter. The battery model considered consists of an ideal 48 V battery and a 5 mΩ equivalent series resistance. The LISN network is made by a DC

decoupling capacitor of 100 nF and a resistance of 50 Ω, while a 5 nH inductor and a 1 µF capacitor are inserted to filter the noise generated from the battery [75]. The equivalent cable model is composed of a 5 µH inductor in series with a resistor of 2 mΩ, which are typical values for automotive applications.

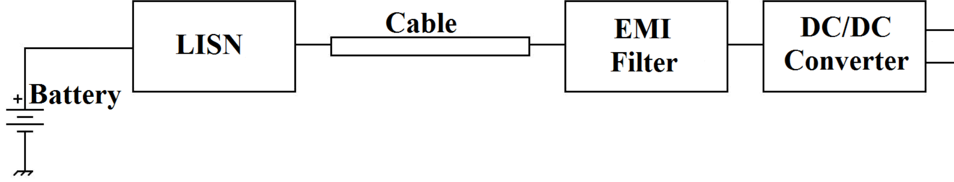

Figure 5.1: *System model for the EMI analysis.*

Thanks to the knowledge of the DC/DC converter architecture and its functionality, described in Chapter 3, it is known that the first stage, called DCDCA in Fig. 3.2, manages the highest voltage of the system, and hence it is the main source of EMI, both conducted and radiated emissions. The two high-voltage techniques, topology reconfiguration, and SKIP mode algorithm, implemented in the converter to face high-voltage issues affect the EMI values:

- The topology reconfiguration technique changes the voltage conversion ratio of the converter depending on the input voltage. The first stage can be driven to do three different VCRs: 1/2, 1, and 2. Every VCR has a different impact on the conducted EMI. The worst-case for EMI emission is the step-up operating mode of DCDCA. In this condition the converter requires input charge in both switching phases, shifting the EMI problem from 90 kHz (switching frequency below the range of interest) to 180 kHz, inside the interest range (frequency > 100 kHz). Moreover, considering the ideal SC model [76–79], the relation between input and output currents in Eq. 5.1 is derived. Hence, considering a constant output current, the maximum request of input charge is when the converter (DCDCA in this case) works with VCR = 2.

$$I_{IN} = VCR * I_{OUT} \tag{5.1}$$

- The control system, Fig. 3.2, drives each switch of the converter with a synchronous digital signal according to the system condition and the input voltage. The SKIP algorithm works independently from the converter topology. When the output voltage of each stage is higher than a fixed value, the SKIP control algorithm holds the status of the converter stage blocking the switching of the MOSFET transistors. This creates a spread spectrum effect as will be detailed in Section 5.4.

5.2 Design of an Anti-conducted EMI Filter

The first technique used to face conducted EMI emission is the classical use of an input EMI filter. Based on the approach discussed in [19], a differential mode is used for the EMI emission analysis. The EMI conducted limits set forth by the CISPR 22 Class B regulation for the frequency range of interest are about 56 dBµV [4, 75]. For

the case study application, to meet the EMI requirement, a filter insertion loss (IL) of about 45 dB is needed. In addition, the filter has entrusted the aims to protect the DC/DC converter from a transient voltage above 70 V, which can damage the IC device. Therefore, in the worst-case considered for the target application, when an input voltage step between 0 V to 60 V with a rapid transient (10 µs) is applied to the converter the overvoltages at the IC input have to keep lower than 70 V. The filter constraints are summarized in Table 5.1.

Table 5.1: *Requirements for EMI filtering.*

	Value	Units	Conditions
Insertion Loss	45	dB	Frequency > 100 kHz
Max input voltage	70	V	Vin transient from 0 V to 60 V in 10 µs

5.2.1 Classic Approach

The filter design approach, typically adopted in the current state-of-the-art, does not take into account the SMPS model, the cable, and the LISN impedances. This may lead to possible oversizing of the filter components. The classic filter topology, which is usually used to reduce the conducted EMI, is the LC network designed to obtain the required IL. Considering that for every pole of the filter the attenuation reduction is expressed by Eq. 5.2, then, for $f_m \gg f_p$, Eq. 5.3 can be derived.

$$|IL|_{dB} = \frac{\beta}{2} log(1 + \frac{{f_m}^2}{{f_p}^2}) \tag{5.2}$$

$$f_p \approx \frac{f_m}{10^{\frac{IL}{\beta}}} \tag{5.3}$$

Taking into account the frequency value of the maximum interference amplitude (f_m), 180 kHz in our case, and the attenuation of an LC filter of 40 dB/decade (β), then the frequency of the two conjugate poles from Eq. 5.3 is about 13.5 kHz. Using a capacitor of 44 µF (a commercially available value), then the inductor value is about 3.16 µH. Hereafter, it is shown that considering the effect of the cable, the LISN, and the converter impedance, it is possible sizing a filter that complies with the conducted limits in Table 5.1, but which employs inductors with values smaller than those used in the state-of-the-art [19, 20].

5.2.2 EMI Filter Design

High filter inductance values produce a high-voltage overshoot when signals with steep edges, typically generated by switches, are applied to the system. Hence, to meet the second requirement listed in Table 5.1, small inductance values have to be used. In addition, great inductance values are obtained with a high number of wire coils, which create a no negligible ESR reducing the whole converter efficiency. The time-domain simulation of an LC filter constituted by 1 µH inductor, its 40 mΩ ESR, a 44 µF capacitor, and its 10 mΩ ESR (typical value for ceramic capacitors), in a steep step input signal condition, shows the strong oscillation shown in Fig. 5.2. The proposed filter

solution consists of four passive elements, as shown in Figs. 5.3 and 5.4: two capacitors, a small inductor, and a resistor. To reduce the oscillations while keeping the same system efficiency, a damping resistor is inserted in series with C_{filter}. This resistor reduces the oscillation but introduces a zero at the frequency shown in Eq. 5.4, such that a bigger capacitor is required to filter. Fig. 5.4 shows the complete electrical model of the system, with the battery, the LISN, the used cable, the proposed filter, and the first stage of the converter used as a case study. The use of only the first converter stage allows reducing the simulation time.

$$f_z = \frac{1}{2\pi \cdot R_{filter} \cdot C_{filter2}} \tag{5.4}$$

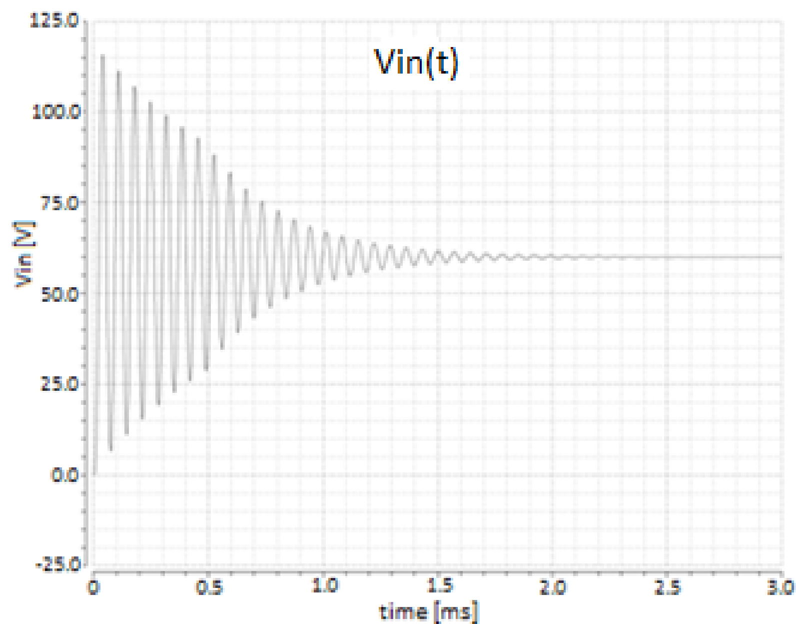

Figure 5.2: *Time-domain response of the low resistive filter, taken at the converter input.*

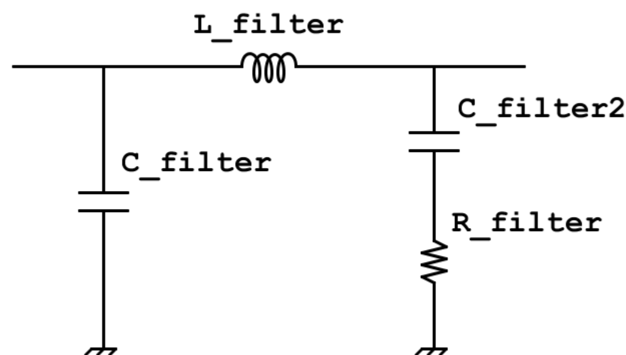

Figure 5.3: *Proposed filter topology.*

The parametric simulations in Figs. 5.5 - 5.8 show the effects of the filter elements on the system frequency response, i.e., representing the magnitude A(f) expressed in

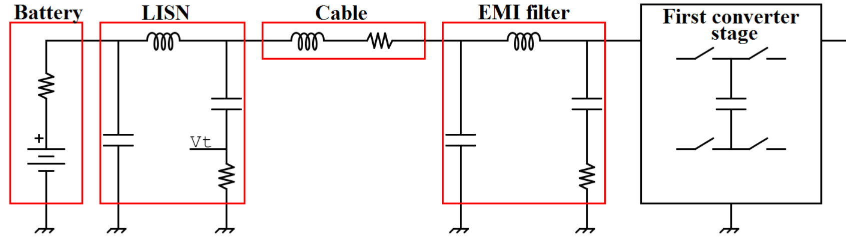

Figure 5.4: *Electrical system model with the proposed filter.*

decibels as a function of L_{filter} in Fig. 5.5, $C_{filter2}$ in Fig. 5.6, C_{filter} in Fig. 5.7, and R_{filter} in Fig. 5.8. All the simulations were made considering ceramic capacitors with 10 mΩ ESR around 180 kHz and monolithic inductors with 40 mΩ ESR at the same frequency. The simulation presented in Fig. 5.5 shows the effect of L_{filter}, where higher values move the second pair of conjugate poles at lower frequencies. This helps to reduce the EMI, but it worsens the overvoltage on the converter input pin when the system is in steep signals conditions. Higher values of C_{filter} improve the filtering but not as much as the previous elements. The resistor introduced to reduce the oscillation during transient alters the behavior of the filter. The two pairs of poles are joined and the newly introduced zero reduces the slope of the filter.

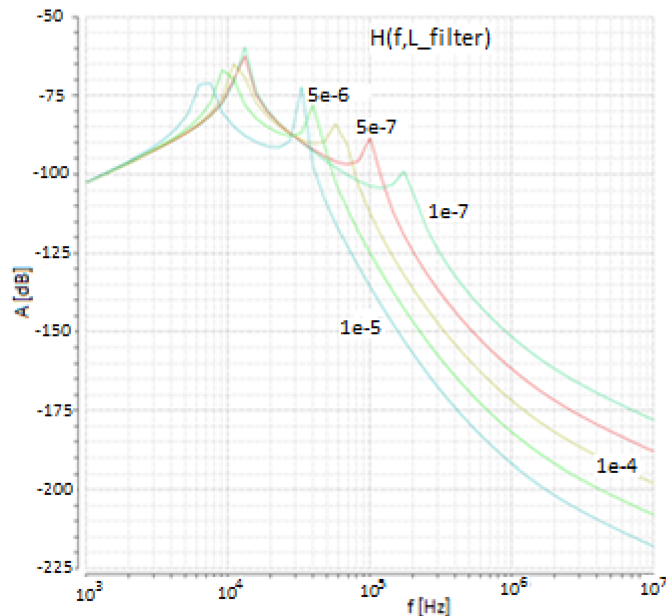

Figure 5.5: *System frequency response as function of L_{filter} (the inductor parametric values are expressed in henries).*

Voltage overshoot during transients due to signals with steep edges, typically generated by switches, can be reduced by employing big values of $C_{filter2}$ and small values of L_{filter}. However, their values will influence the frequency response of the system and this should be compensated by an increase in the C_{filter} value. Performing some parametric simulations, it is possible to find the optimal R_{filter} value, which creates a minimum in the overvoltage characteristic (see Fig. 5.9). This is the value that sets the

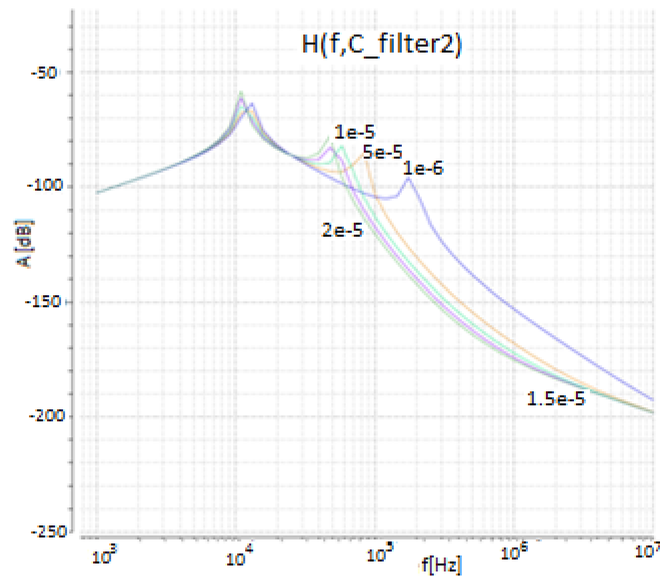

Figure 5.6: *System frequency response as function of $C_{filter2}$ (the capacitor parametric values are expressed in farads).*

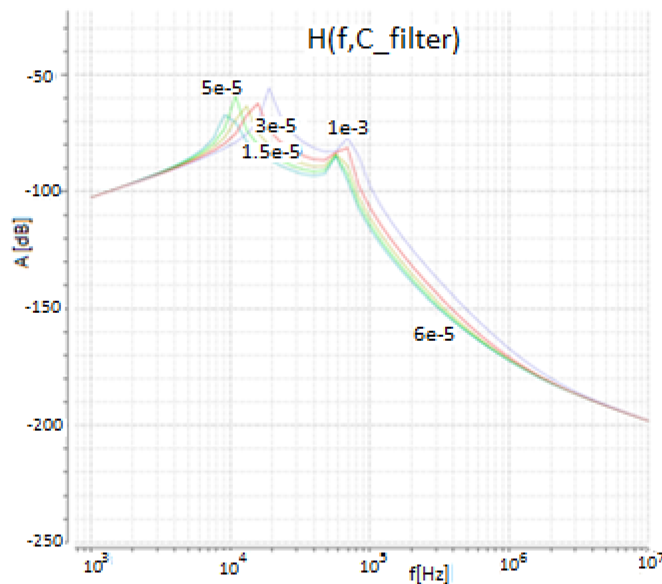

Figure 5.7: *System frequency response as function of C_{filter} (the capacitor parametric values are expressed in farads).*

zero (introduced by $C_{filter2}$ and R_{filter}) close to the complex conjugate poles. Thanks to parametric simulations, the values of the filter components listed in Table 5.2 were calculated. With these values, the filter was devised to satisfy the requirements reported in Table 5.1. It is worth noting, from Table 5.2 and Fig. 5.10, that the system requirements of Table 5.1 are met using an inductor value of 1 µH (reduced by a factor higher than three versus the 3.16 µH inductor calculated with the classic approach). Table 5.3 shows the list of commercial passive elements that verified the requirements of Table 5.2, which are used to implement the EMI filter in the testing board of Fig. 5.11. An

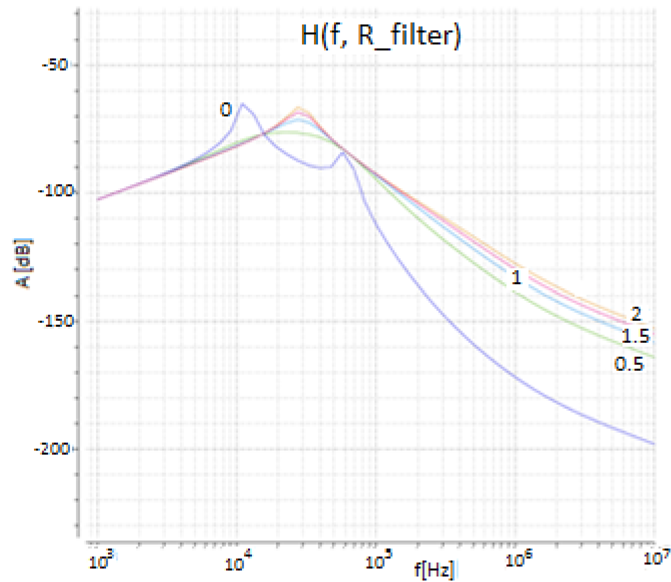

Figure 5.8: *System frequency response as function of R_{filter} (the resistor parametric values are expressed in ohms).*

ESR of the L_{filter} higher than that used in simulations leads to a reduction of overvoltage but affects the efficiency of the filter. An ESR of the C_{filter} higher than that used in simulations, on the one side, has the positive effect of reducing the overshoot, but on the other side, it degrades the filter response. In Table 5.2, the parasitic element ranges, which still allow meeting the requirements of Table 5.1, are identified. The results obtained with the designed filter in terms of the EMI noise and of the time response are shown in Figs. 5.10 and 5.12.

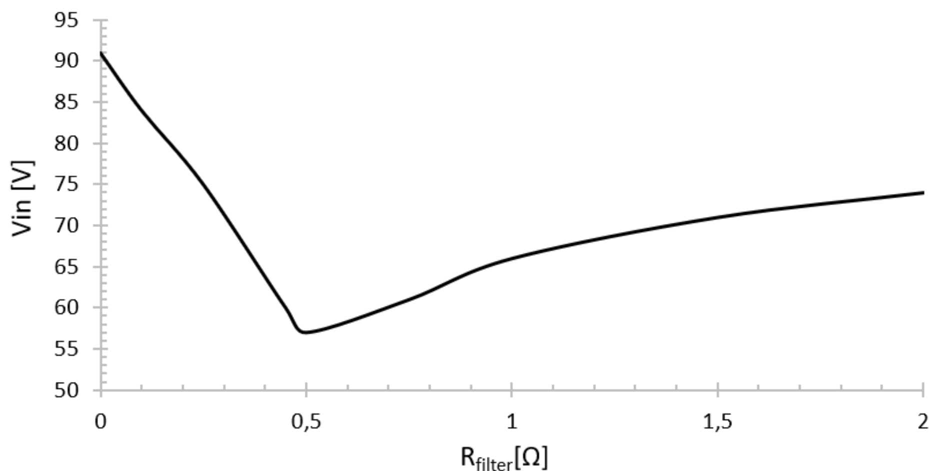

Figure 5.9: *System overvoltage as function of R_{filter}.*

Table 5.2: *Components of the EMI filter*

	Value	Electrical Rating	ESR range
C_{filter}	10 µF	100 V	Max 20 mΩ
$C_{filter2}$	44 µF	100 V	Max 20 mΩ
L_{filter}	1 µH	2 A	25 mΩ < ESR < 160 mΩ
R_{filter}	0.5 Ω	125 mW	-

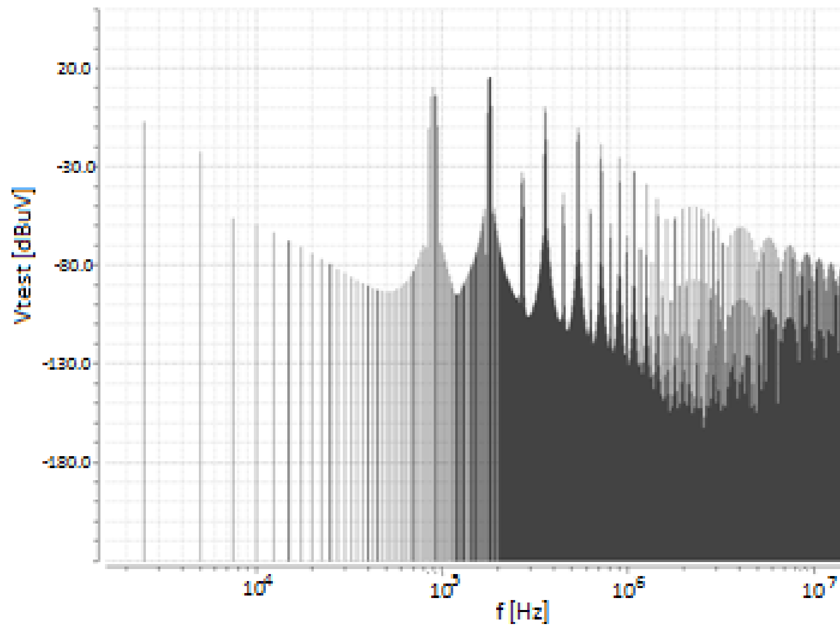

Figure 5.10: *EMI noise result (within the required limit).*

Table 5.3: *List of commercial components used for the input EMI filter in the testing board of Fig. 5.11*

	Part Number	Producer	Size [mm]
C_{filter}	KCM55QR72A106KH0	Murata	6.1 * 5.3 * 3.7
$C_{filter2}$	KRM55WR72A226MH	Murata	6.1 * 5.3 * 6.4
L_{filter}	LQM31PN1R0M00	Murata	3216
R_{filter}	RK73H2BTTD2R00F	KOA	3217

5.2.3 Filter Effects on the Converter System

The control system, implemented in the converter (see Chapter 3), creates a feedback network optimized to obtain the best converter performance. When cascading an EMI filter before the converter, the EMI filter could destabilize its frequency response. According to Middlebrook's extra element theorem [80], applied to a three-port electrical network, the transfer function between two ports changes if the impedance view from the third port changes. This change can be taken into account with a correction factor that depends on the impedance view inside the third port and from the third port. In the considered converter system of Fig. 5.13, the three ports are the input, the output, and the port used by the control system. In small signals condition, the input port can view a short (equivalent model of the voltage generator for small signal conditions) or, when the EMI filter is inserted, the output impedance of the filter. Hence, the frequency re-

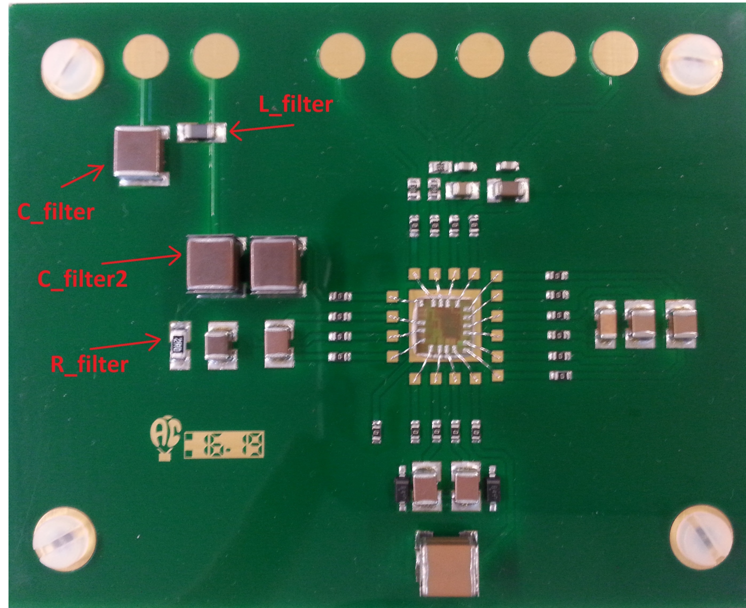

Figure 5.11: *Testing board already showed in Chapter 4 with the EMI filter elements highlighted.*

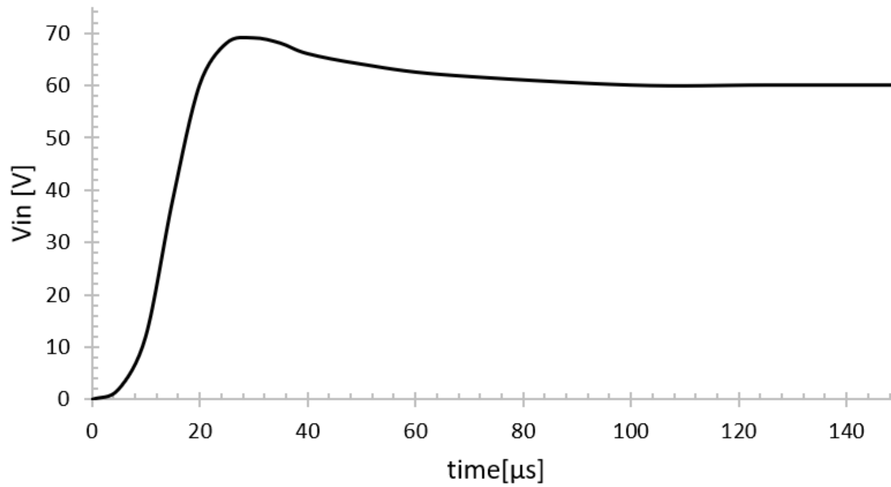

Figure 5.12: *Time-domain simulation (within the required limit).*

sponse between the output converter port and the control port, H(s) in Fig. 5.13, could change when inserting the EMI filter. To avoid this, the input impedance of the converter should be much higher than the output impedance of the EMI filter, as proved in [21] and [81].

In addition, this condition ensures that the insertion of the EMI filter does not cause stability issues. At low frequency, the SC converter is modeled as an ideal transformer plus an output resistor. Hence, considering a resistive load, the input impedance is real and can be expressed by Eq. 5.5. Some simulations to evaluate the input impedance of the converter in a frequency range from 10 Hz to 100 MHz were carried out. Fig. 5.14 shows the converter input impedance for two VCRs (VCR = 1/2 on the left axis and VCR = 2 on the right axis) used in the SC design. The impedance in Fig. 5.14 has a

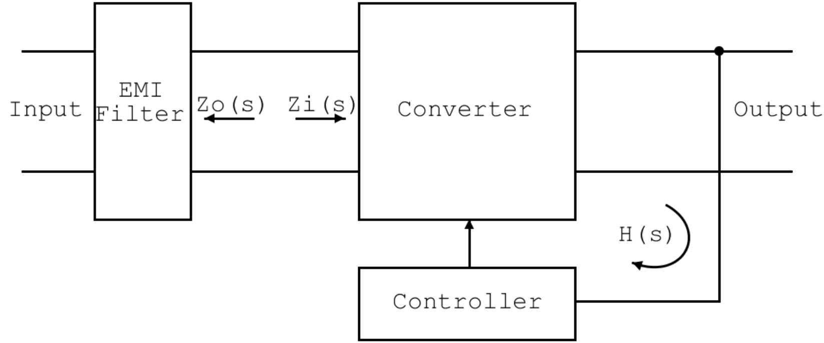

Figure 5.13: *System model.*

pole-zero behavior. The resistive effect is evident for low frequencies (below 100 Hz) and for high frequencies (beyond 10 kHz for VCR = 2 and beyond 1 MHz for VCR = 1/2).

$$R_{in} = -(\frac{n_1}{n_2})^2 \cdot (R_{out} + R_{load}) \tag{5.5}$$

The frequency behavior of the input impedance of the proposed inductorless converter of Fig. 5.14 is different from the behavior of the classic inductor-based switching converters. Indeed, the inductive element increases the input impedance for high frequency and creates a low impedance peak (as a resonant peak) that can cause the converter instability according to the theory in [21,22,75,80,82]. In addition, as described in Section 5.1, the worst case for EMI noise is the step-up mode (VCR = 2). This is also the worst case for stability, since in Fig. 5.14, the input impedance for VCR = 2 is smaller than the other cases (Z_{in} of the converter is about 35 Ω below 100 Hz and 22 Ω over 10 kHz).

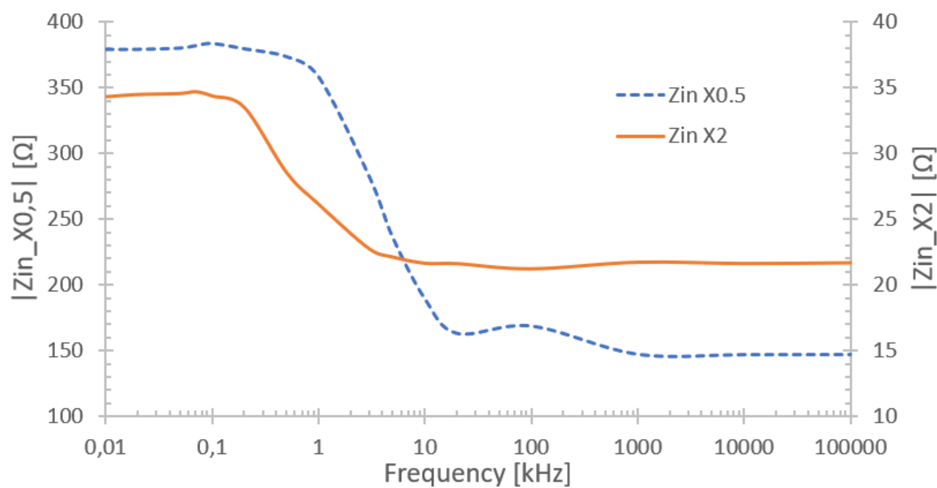

Figure 5.14: *Input impedance of the converter for two operating modes. The axes are split in the left axis for VCR = 1/2 and in the right axis for VCR = 2.*

Fig. 5.15 shows the output impedance of the EMI filter. At low frequency, the impedance is dominated by the inductor ESR, while around 10 kHz, a peak appears

due to resonance condition, and at a higher frequency, the $C_{filter2}$ ESR predominates. In the considered frequency range, the output filter impedance is much smaller than the converter input impedance. Therefore, the Middlebrook's condition is verified and the filter affects neither the converter frequency response nor its stability. The equivalent model of the converter highlights an input negative resistance (see Eq. 5.5). This can be observed considering a constant output power and the following equations, where η is the efficiency of the converter and I_{in} and V_{in} are the input current and voltage of the converter.

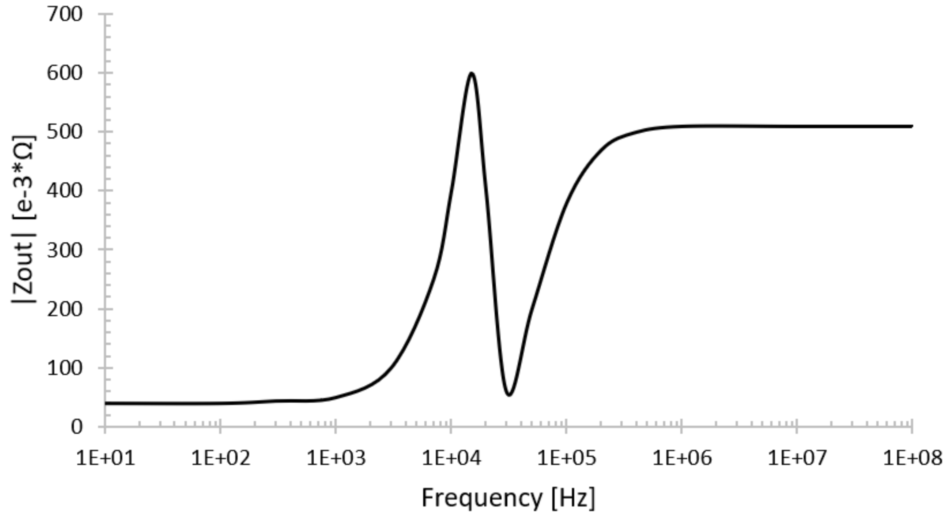

Figure 5.15: *Output impedance trend of the EMI filter.*

$$P_{out} = \eta \cdot P_{in} \tag{5.6}$$

$$I_{in} = \frac{P_{out}}{\eta \cdot V_{in}} \tag{5.7}$$

$$R_{in} = \frac{1}{\frac{\delta I_{in}}{\delta V_{in}}} = -\frac{\eta \cdot V_{in}^2}{P_{out}} \tag{5.8}$$

If the output impedance of the EMI filter has a real part comparable with the negative input resistance of the converter, a null resistance loop appears, and so, an oscillation can sustain itself. To avoid this effect, at least one of the two conditions in the Eq. 5.9 has to be verified:

$$|Z_i(f)| \ll |Z_o(f)| or |Z_i(f)| \gg |Z_o(f)| \tag{5.9}$$

The first condition in Eq. 5.9 is the same with the Middlebrook's condition. The designs of the filter and of the on-chip converter was implemented using this rule (see Figs. 5.14 and 5.15). Hence, it is verified that the filter does not change the frequency response of the converter and does not introduce instability issues. The stability of the cascade EMI filter converter was also verified by accurate simulations in the Cadence's CAD environment plus exhaustive experimental measurements on the testing board. Concerning the impact on power efficiency of the EMI conductive filter, the ESR of

the inductor in the filter leads to a power loss and hence to a power efficiency drop. The power losses can be estimated multiplying the ESR value with the squared value of the average current flowing in the filter. In the proposed filter (see Table 5.3), a 1 μH inductor from MURATA whose ESR is 40 mΩ is used. Since steady-state input currents are in the order of 100 mA, the power dissipation is below 1 mW. This value has a negligible impact versus power levels provided to the loads, which are in the order of a few watts. Moreover, the proposed design leads to a reduction of the inductor to be used versus the state-of-the-art. Reducing the inductor size, the ESR and the negative impact on power efficiency are also reduced.

5.3 Experimental Measurements of Conducted Electromagnetic Emissions

In this section, the previous technique used to design the EMI filter is validated with experimental results. The testing board in Fig. 5.11 is designed to obtain a clear characterization of the device, avoiding the influence that different packages may have on the measurements. Therefore, it is equipped with a glued bare chip bonded directly on the PCB. The types of package pins, such as ball grid array, quad flat package, dual inline, or others, could increase the resistance of critical paths and modify the effect of electromagnetic emissions (ceramic or plastic compound can influence it). The SMD filter elements, selected in the previous simulative analysis and listed in Table 5.3 are used to create the input filter, as highlighted in Fig. 5.11. The measurements were performed considering the equivalent cable model, a LISN, and the spectrum analyzer Anritsu MS2665C, which allows displaying the signal frequency components taken on the 50 Ω resistor. The switching mode of the device under test changes with the input voltage and the load current. Hence, different configurations were used, like those listed in Table 5.4, to identify critical conditions. Table 5.4 shows the amplitude values of the second and third harmonics of the test signal in the LISN without the use of the filter. Table 5.5 shows the results with the same setups using the filter proposed in this thesis. From the experimental results, the first harmonic is around 88 kHz (that is 2 kHz below the nominal value, but it can be compensated through a proper trimming of the internal oscillator) and it is out of the range of interest (requirements listed in Table 5.1). Instead, the second and third harmonics, around 179.2 kHz and 270.4 kHz, respectively, are within the constraint frequency range.

The most critical values, highlighted in red in Tables 5.4 and 5.5, appear with low battery voltage. This is due to the step-up operation mode of the first DC/DC converter stage (DCDCA). In all other cases, the converter operates as a step-down, so the worst values are around the fundamental harmonic, out of the range of interest. The proposed filter limits the conducted EMI under the CISPR 22 constraint for all the wide range of setup. A comparison between the measurements without and with the filter is done to understand the effects of the filter and its IL. Table 5.6 shows the IL of the filter. In Table 5.6, the measured IL of the filter is around 40 dB–45 dB for the second harmonic, for battery values up to 24 V. The measured IL of the filter decreases with the increase in input voltage (see Table 5.6 at 48 V or 60 V). However, the obtained IL keeps the conducted EMI under the constraint (see Table 5.5) since, at 48 V or 60 V, the EMI values without the filter in Table 5.4 were lower than those at 8 V, 12 V or 24 V.

Table 5.4: *EMI conducted results measured without the use of the input filter. The most critical values are higlighted in red.*

Set-up		EMI measurement results without the filter	
$V_{BATTERY}$ [V]	I_{LOAD} [mA]	II Harmonic [dBm]	III Harmonic [dBm]
8	0	-33.05	-33.06
8	150	-9.97	-22.77
8	300	-7.04	-19.21
12	0	-26.88	-27.57
12	150	-14.04	-25.51
12	300	-9.00	-18.59
24	0	-48.89	-40.78
24	150	-20.77	-19.19
24	300	-16.32	-15.25
48	0	-38.69	-26.88
48	150	-26.26	-23.18
48	300	-20.31	-20.09
60	0	-40.33	-41.15
60	150	-30.21	-33.55
60	300	-26.27	-32.83

Table 5.5: *EMI conducted measurement results obtained with the use of the input filter for different converter set-ups.*

Set-up		EMI measurement results with the filter	
$V_{BATTERY}$ [V]	I_{LOAD} [mA]	II Harmonic [dBm]	III Harmonic [dBm]
8	0	-80.03	-94.19
8	150	-54.87	-93.95
8	300	-51.61	-99.04
12	0	-76.40	-87.53
12	150	-58.15	-87.65
12	300	-52.75	-89.81
24	0	-88.31	-88.56
24	150	-64.96	-68.77
24	300	-60.14	-63.29
48	0	-67.09	-76.05
48	150	-59.88	-66.08
48	300	-55.73	-61.52
60	0	-68.85	-75.77
60	150	-60.10	-66.57
60	300	-59.37	-63.81

5.4 Effects of SKIP Algorithm on the Conducted EMI

The effect of the reconfiguration topology algorithm in the conducted EMI was already shown in Section 5.1 and was used to identify the worst case. In this section, the effect of the SKIP algorithm in conducted EMI is discussed. The SKIP control holds the status of the converter stages, and therefore it changes the switching signal waveform. The effects that this control has on the switching signals depend on the condition of the system, on the input voltage, and on the output current, which can be variable. This algorithm expands the spectrum components in a wider frequency range, reducing the harmonic peaks. This effect is displayed in the MATLAB simulation results reported in Figs. 5.16 and 5.17. The harmonic values are reduced using the SKIP control technique

Table 5.6: *IL of the proposed filter.*

Set-up		EMI measurement results with the filter	
$V_{BATTERY}$ [V]	I_{LOAD} [mA]	II Harmonic [dBm]	III Harmonic [dBm]
8	0	46.98	61.13
8	150	44.90	71.18
8	300	44.57	79.83
12	0	49.52	59.96
12	150	44.11	62.14
12	300	43.75	71.22
24	0	40.42	47.78
24	150	44.19	49.58
24	300	43.82	48.04
48	0	28.40	49.17
48	150	33.62	42.90
48	300	35.42	41.43
60	0	28.52	34.62
60	150	29.89	33.02
60	300	33.10	30.98

(the first harmonic value is reduced of about 6.54 dB, the second of about 5.80 dB). This effect is clearly observed in the experimental measurements. The first stage of the converter uses this SKIP algorithm to limit at 25 V its output voltage, hence, for input voltage above 50 V, this control system is activated (the last three setups reported in Tables 5.4, 5.5 and 5.6). The two spectrum waveforms taken during the experimental measurements are presented in Figs. 5.18 and 5.19. In Fig. 5.18, it is clearly observable the discrete spectrum of the periodic signal, while in Fig. 5.19, the effect of the SKIP technique is shown.

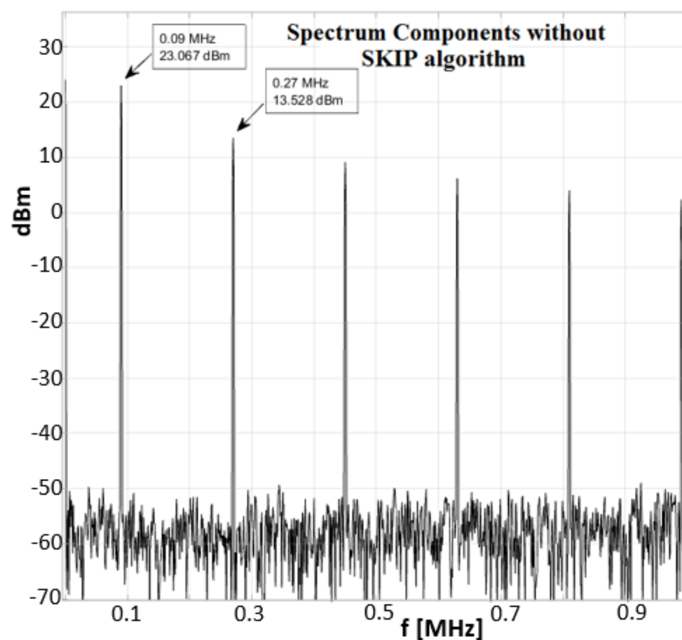

Figure 5.16: *Simulation results obtained without the SKIP algorithm.*

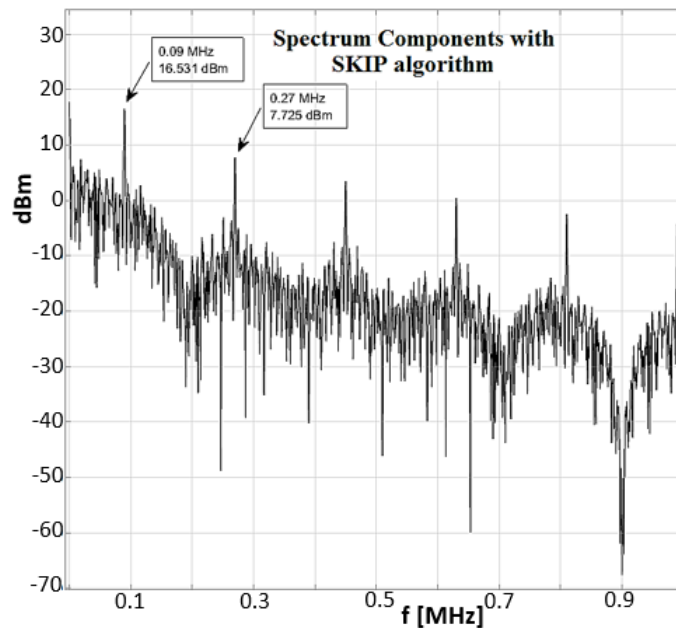

Figure 5.17: *Simulation results obtained with the SKIP algorithm.*

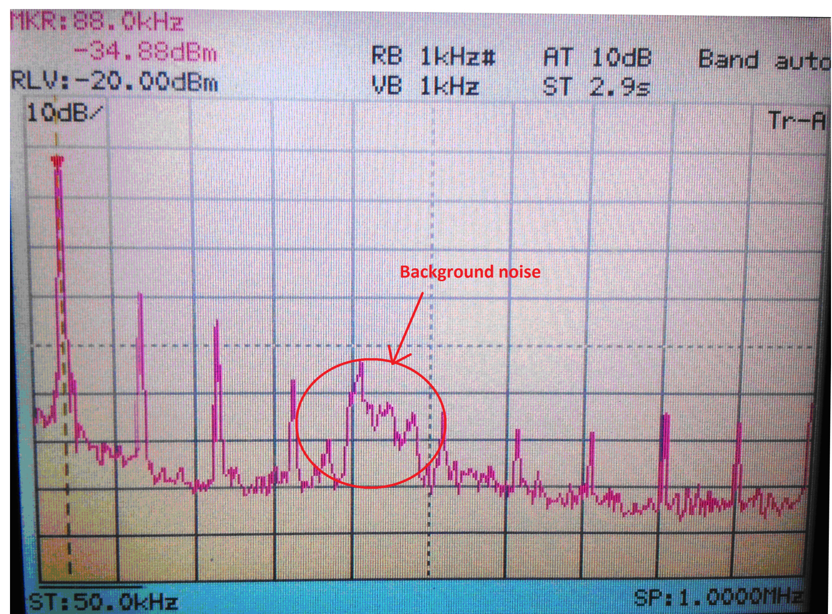

Figure 5.18: *Test signal spectrum in normal converter operating condition.*

5.5 Measurements of Radiated Interference

From literature, and from the practical experience of industrial partners, with switching frequencies below 100 kHz, the effect of radiated emissions can be neglected with respect to the conducted emissions. Therefore, the main switching frequency of the DC/DC converter used in this research was set to 90 kHz. Then, this assumption was confirmed by experimental measurements of electromagnetic emissions. The use of

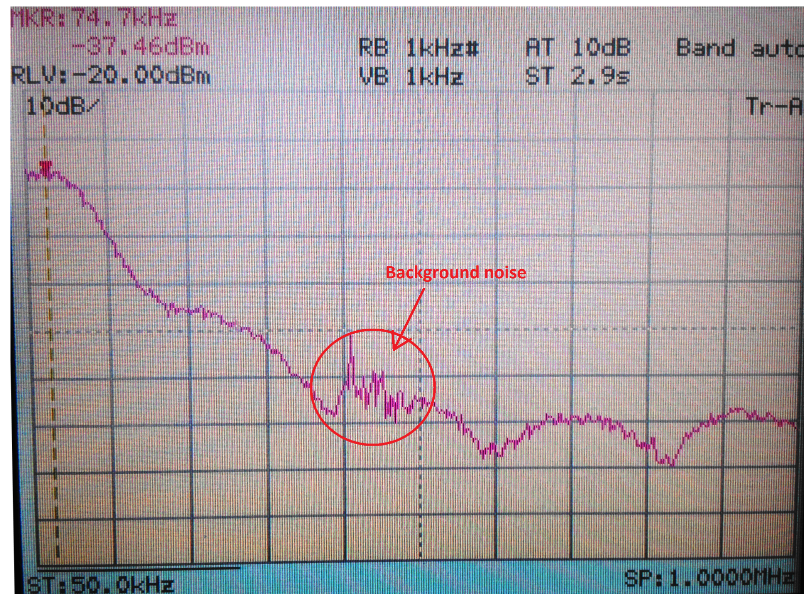

Figure 5.19: *Test signal spectrum modified by the presence of SKIP control.*

a testing board with the bare die allows obtaining real emission results without the shielding effect of the package. These measurements were made in an anechoic room (see Fig. 5.20) with a near-field sensor Hameg HZ530 (mono-pole), placed at a distance of 1 m from the board operating in different setups of the switching converter. Indeed, at the working frequencies of the switching converter, few tens of kilohertz, the radiated emissions are near-field coupling. Fig. 5.21 shows the results of this test with 48 V input voltage and 300 mA output current. The radiated power is concentrated on the odd harmonics of the switching frequency. The first peak is at 90 kHz, but it is not the highest peak, as expected. The highest peaks are the third, fifth, and seventh harmonics, which amplitude still be lower than -70 dBm. The different operating conditions of the converter do not significantly influence the radiated EMI. The implemented techniques, lowering the radiated emission levels under -70 dBm, make the proposed DC/DC converter suitable for electromagnetic sensitive applications. For example, the combination of the TID and emission performances, showed in this Chapter and in Chapter 4 respectively, enabling the DC/DC converter to operate in GOCE, EXOMARS, Rosetta, BepiColombo and Solar Orbiter missions [83–86]. The payload of these missions, aiming to measure electromagnetic fields and particle population in space plasma, is extremely sensitive to low frequency electric and magnetic fields and requires stringent electromagnetic cleanliness. This necessity for cleanliness occurs due to the sensitivity of the measuring instruments placed on the spacecraft boom [87]. For this reason, in Fig. 5.21 is displayed also the ECSS-E-ST-20-07C standard limit, typically used for aerospace applications [88] and the stringent limits imposed by the GOCE mission aircraft. As a result of the comparison displayed in Fig. 5.21, the radiated emissions of the proposed DC/DC inductorless converter are well below the GOCE EMC limits without the use of metallic shields, lowering the spacecraft weight as well as the launch cost.

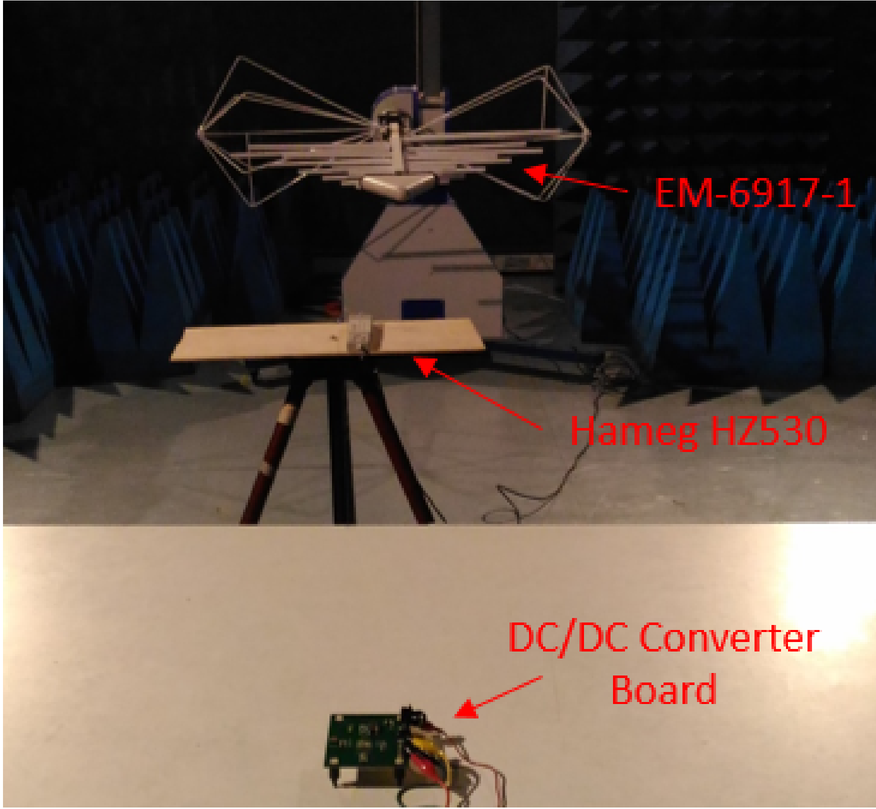

Figure 5.20: *System set-up for radiated EMI test in anechoic room.*

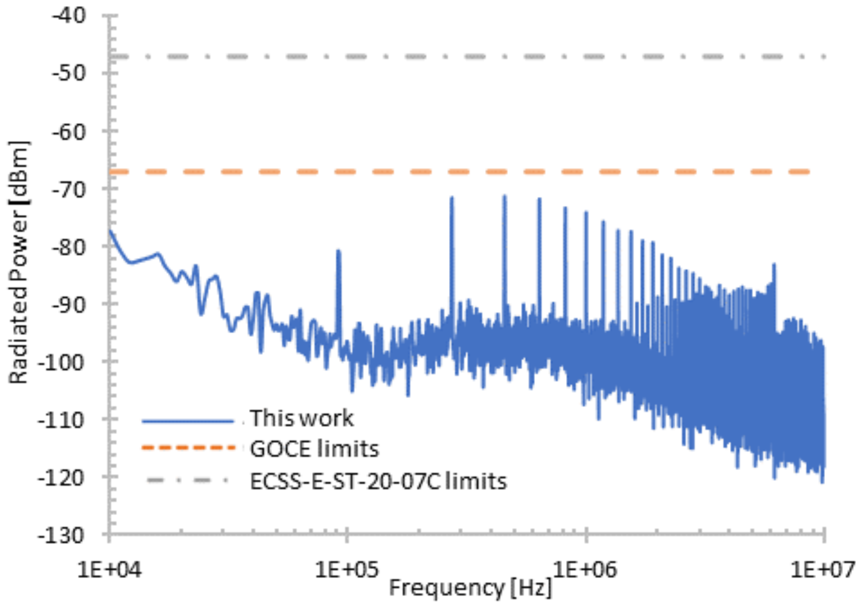

Figure 5.21: *Electric field measured at a distance of 1 m from the testing board in anechoic room.*

5.5.1 EMC Standard Test

A test of standard electromagnetic compatibility (EMC) was performed to verify that the designed DC/DC converter is compliant with domestic environment legal limits (CISPR 22). The test was performed in an anechoic room at 3 m from the converter with the biconical antenna EM-6917-1. This test compares the emissions from 30 MHz to 1 GHz with standard limits (red line in Fig. 5.22). The test does not show EMC problems and the converter emissions are hidden in the background.

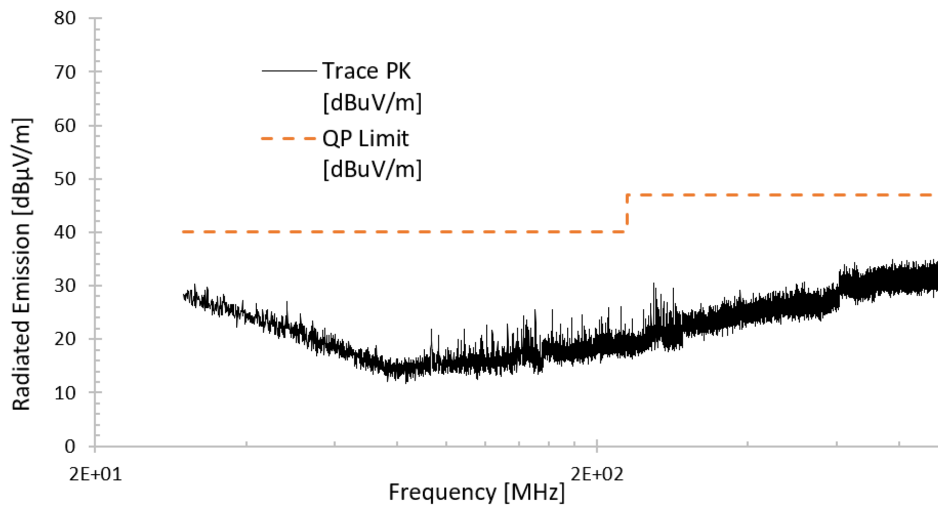

Figure 5.22: *Test of EMC results, CISPR 22 law limit.*

5.6 Soft-Start Techniques to Reduce Peak Currents

The typical approach to the design of a DC/DC switching converter is conducted as a separate view of the converter design from the EMI problems. If the converter would be designed to take into account the EMC problems already in the embryo project phase, it would be possible implementing some additional techniques, such as the soft-start [89–92]. One of the most critical operating phases of the switching converters, and in particular of the SC type selected here as a case study, is the wake-up phase. Indeed, during wake up, the capacitors are discharged and this, combined with the low resistances of switches, leads to high current peaks (see Fig. 5.24), which create high disturbance values. These currents are even one order of magnitude higher than steady-state currents, e.g., 5.6 A in the considered case study versus steady-state currents below 0.5 A. These current peaks in the converter awakening phase generate high levels of disturbance on the power line. All the devices connected at the same power source will suffer from this effect. In addition, these high spikes can damage the converter reducing its reliability (see Fig. 5.23). Fig. 5.23 shows the effect of an uncontrolled wake-up phase. The input pad of the chip, the board pad, and the bonding wire were fused by these high current peaks. Therefore, a soft-start technique is required to reduce the current peaks. While the EMI filter designed in Section 5.2 is outside the DC/DC converter integrated circuit, the soft-start solution must be integrated within the DC/DC

circuitry. In the converter design phase, it is possible to use different solutions to make a soft-start. In this work, an increment, at soft-start, of the resistance of the switching elements is adopted.

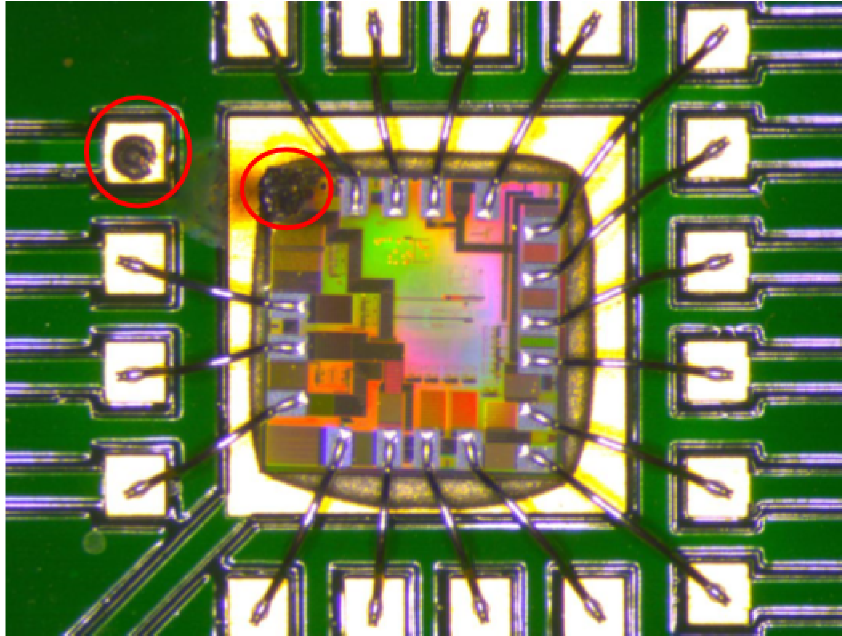

Figure 5.23: *Die glued on board damaged by wake-up current peaks.*

The idea is realizing the power switches of the converters as multiple MOSFETs working in parallel. By controlling the number of transistors that are operating, it is possible to control the resistance value of each switching element. The resistance value is increased at the starting phase to reduce high current peaks and is decreased at the steady-state to improve the converter efficiency. In the wake-up condition, the voltage drop across the converter switches is high and the overdrive is fixed by the driver, so the current is limited from natural MOSFETs characteristics. The lower is the number of parallel transistors, the lower is the current in this phase. Therefore, the gates of the MOSFETs are driven separately and only some of them are enabled at the converter wake up. Furthermore, the first stage of the SPSM requires more input charge when working as step-up, as discussed in Section 5.1, hence this conversion mode was disabled during the soft-start. Comparing the input current shown in Fig. 5.24 with Fig. 5.25, the three times current peak reduction obtained thanks to the use of the soft-start can be observed in the second setup. Since the soft-start increases the resistance at the starting phase, it has a negative impact on power efficiency during the starting transient. However, this technique is applied only during the awakening transient whose time duration is limited at 0.2 ms (e.g., from 0.1 ms to 0.3 ms in Fig. 5.25). Hence, its overall impact on the average power efficiency is negligible.

5.7 Electromagnetic Interface Comparison to State-of-the-art

The filters for the reduction of the EMI produced from SMPS are typically realized with passive elements, capacitors, inductors, and resistors. The big values of used in-

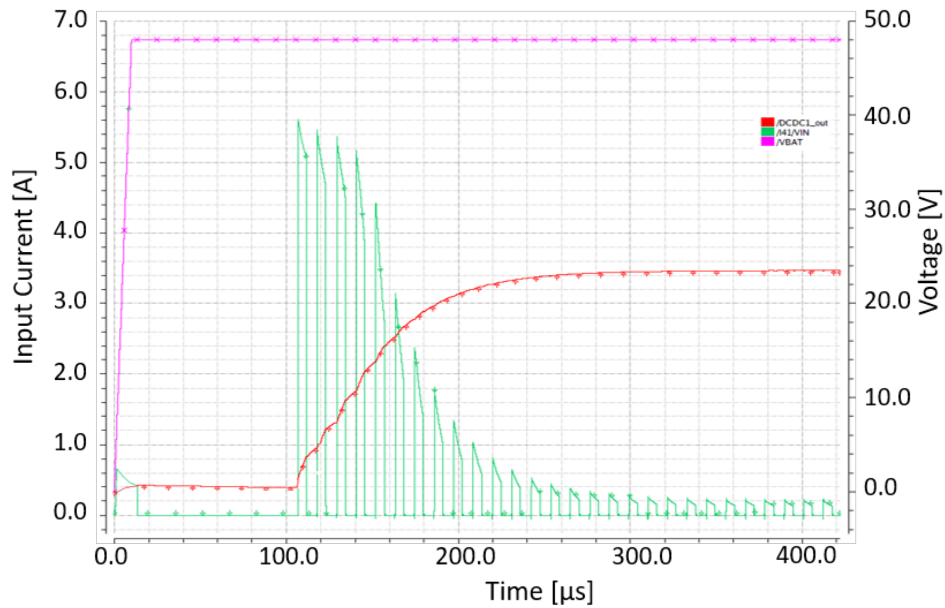

Figure 5.24: *Input current without soft-start modality (the green signal is the input current request from the converter).*

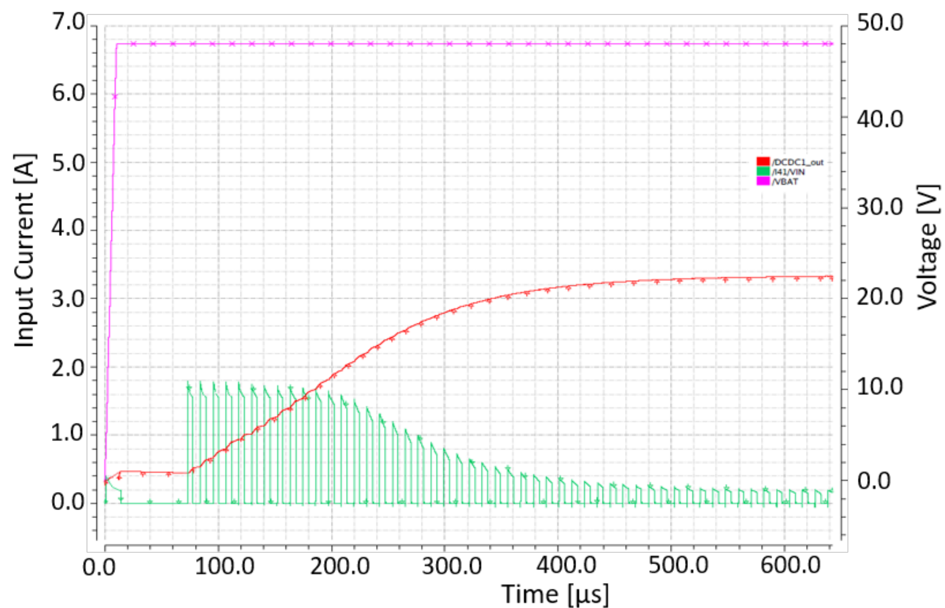

Figure 5.25: *Input current with soft-start modality (the current peaks, represented by green signal, are reduced by three times versus Fig. 5.24).*

ductors limit the integration of these filters. For applications in the automotive and aerospace (see Chapter 2), system integration is becoming a fundamental requirement,

hence low inductor values have to be used. For high-voltage applications, such as the new emerging 48 V battery standard application in the automotive industry, the cable parasitic elements and high slope signals can generate overvoltage. Hence, countermeasures that mitigate such situations should be taken.
Table 5.7 displays a qualitative comparison between the techniques discussed in this work, focusing on the reduction effects of conducted and radiated EMI, the possibility of integration on-chip, the design effort required, and the cost of additional components and occupied area. For design effort and cost, the negative values should be intended as a higher effort and cost.

Table 5.7: *Comparison of the three proposed EMI reduction techniques*

	Conducted EMI reduction	Radiated EMI reduction	Could be integrated	Low design effort	Low cost
EMI filter	+++	-	- -	- -	- -
SKIP control	++	++	+++	+	++
Soft-start technique	+	+	+++	-	+

It is worth noting that the three techniques allow for a reduction of EMI conducted and radiated emissions without any negative impact on the stability and power efficiency of the converter, as discussed in Sections 5.2 and 5.4. Considering a comparison with the state-of-the-art, the following conclusions are drawn:

- The proposed EMI filter reduces with 45 dB the conducted interferences using low inductor value, which is smaller than that used in the state-of-the-art by a factor 3 versus [93] and by one order of magnitude versus [19] and [20]. A lower inductor value leads to lower cost and size for the filter.
- The SKIP algorithm allows reducing the EMI emissions with a design effort lower than that required by the current state-of-the-art techniques [94] and [95]. The power of this control method is its easy implementation that also allows for reducing the cost of additional components.
- The soft-start technique implemented here allows for a reduction of about three times the current spikes in the converter starting phase, without adding dedicated large power components to manage this phase.

CHAPTER 6

TID and SEU Mitigation Techniques

As electronic systems are pervading harsh environments, new challenges have to be faced in order to increase the electronics reliability of systems under extreme temperature, electromagnetic fields, and radiation conditions. The electronic devices, operating in aerospace and HEP environments, described in Chapter 2, have to withstand performance decreasing effects due to radiation phenomena. Generally, three main approaches have been considered to develop radiation hard electronic components: process enhancement (Radiation Hardening By Process, RHBP [96]), design enhancement (Radiation Hardening By Design, RHBD [97]), and finally shielded packages (Radiation Hardening By Shield, RHBS [98]). RHBP requires a very expensive dedicated process or specific variation of a standard process, which does not have the same maturity as a standard one. In general, RHBP presents an effort that can be supported only by large silicon foundries but the rad-hard market is only a niche. RHBS, usually, needs expensive and cumbersome shields that can not be adopted for applications where weight and volume are essential. For example, NASA's Europa Clipper spacecraft uses 12.7 mm aluminum walls to shield the internal devices from external radiation (see Chapter 2), which impacts on the launch cost. Therefore, RHBD techniques are preferable whenever is possible. Radiation effects affect semiconductor devices in two predominant ways:

- Dose effects are characterized by slowly parameters shifts that accumulate over time due to radiation exposure. They lead the semiconductor devices to drift out of tolerance constraints and fail.
- Single-event effects are random, instantaneous disturbs generated by the passage of a single particle or photon. Each SEE can lead to failures in more than one device.

6.1 Total Ionizing Dose Effects

In response to radiation exposure, TID sensitivity can limit product reliability and functionality. TID is defined as the energy absorbed by a unit mass of material when exposed to ionizing radiation. The overall exposure is quantified in units of radiation-absorbed dose, or rad, which is defined as the dose that causes the absorption of 100 ergs by one gram of matter. The International System of Units uses grays (Gy), with 1 Gy = 100 krad = 1 J/kg. Since most commercial and research sectors continue to use the rad in this thesis all TID levels are reported in rad(SiO_2).
The key mechanism driving TID, in electronic devices, is the generation, transport, and trapping of holes in insulation materials. Each type of radiation (photons, ions, neutrons, electrons) loses energy in different ways while traversing matter. This energy released in insulating materials creates electron-hole pairs, which, in the presence of electrical fields, are split. The electrons, having higher mobility than holes, are fast swept out from the insulator. Instead, the holes slowly migrate by drift and diffusion toward the SiO_2-Si interface. In addition, this process breaks chemical bonds, releasing trapped protons (H+). These protons are free to diffuse or drift in the same direction as the holes, see Fig. 6.1. For N-MOSFETs, the positive oxide trapped charge leads to a reduction in threshold voltage (V_{th}), instead, for P-MOSFETs, these charges produce an increment of the V_{th}. The holes that migrate toward the SiO_2-Si interface get captured by mid-band-gap traps near the interface or are captured at the interface itself, where they create interface states, leading to an increase of the subthreshold swing of both the MOSFET types. Therefore, the combination of these two effects (positive charge trapped in gate oxide and interface traps) makes N-MOSFETs less damaged by radiation phenomena [99]. The amount of charge collected by MOSFET oxide is strictly correlated with its thickness, indeed the higher is the oxide thickness and the stronger is the effect that charge has on MOSFETs [100], in particular, a ${t_{ox}}^2$ dependence of the flat band voltage shift is observed. The high-quality gate oxides in today's advanced CMOS technologies, much thinner than 10 nm, have minimized TID induced threshold voltage shifts in individual transistors for most applications. However, even in these technologies, the field insulation for adjacent transistors remains relatively thick and will exhibit sensitivity to TID-induced charge. This effect was already described in the TID test of the DC/DC converter, Section 4.3.3, which demonstrated to be able to operate up to 43 krad.
For the design of electrical circuits sustaining the higher cumulative doses required by the HEP experiments (see Chapter 2), advanced technology with respect to the 0.35 µm technology used for the DC/DC converter is adopted. The technology chosen for the high-speed rad-hard driver design, detailed reported in Chapter 7 is the commercial-grade TSMC 65 nm technology. It is, currently, the state-of-the-art technology for rad-hard applications, thanks to its only 2 nm thin gate oxide [41, 101–105], which makes its MOSFETs very rad-hard devices. Nevertheless, the ehps generated in the spacer oxide and at its interface with the LDD (Lightly Doped Drain) region can modify the effective doping of LDD and affect the overall channel resistance, in a greater way for P-MOSFETs and lower for N-MOSFETs [102], see Fig. 6.2. In addition, the radiation effects on the Shallow Trench Isolation (STI) between different devices, has a dramatic consequence on P-MOSFET devices, where the charge trapped in the interface traps

and in the bulk oxide is positive, adding up their contributions and tending to turn off the transistor. In N-MOSFET devices, the two defects typologies trap opposite charges: the positive charge accumulated in the STI is responsible for the creation of parasitic transistors along the main channel, and the negative charge buildup in the interface tends to turn on them [102]. In Fig. 6.3 are shown the consequences that the previous radiation effects have on the current of minimum size MOSFETs when exposed to high radiation levels.

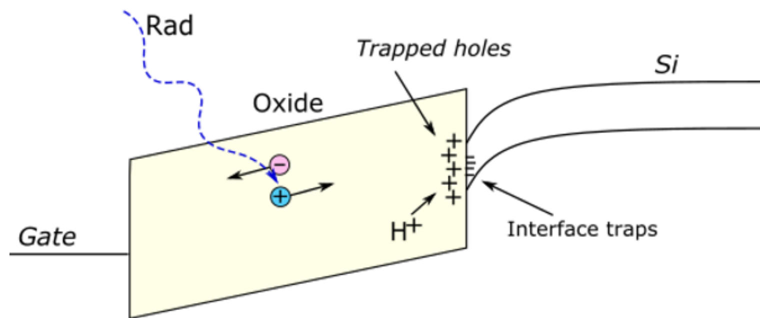

Figure 6.1: *Energy bands of MOSFET structure and radiation effects*

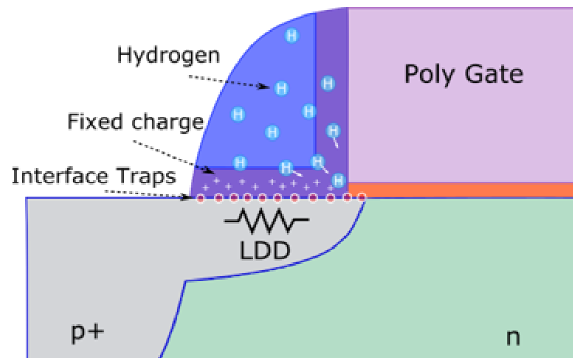

Figure 6.2: *LDD spacers cross section and collected charge trapped when the MOSFET is exposed to radiation.*

Although the SOI technology is widely used for rad-hard space systems, for the application targeted in this work the bulk-silicon technology was preferred. Even though the sensitive volume for charge collection of SOI substrate is much smaller than for bulk-silicon devices, making SOI devices much harder to SEE, the radiation creates charge buildup in the buried oxide of SOI transistors, making this technology more sensitive to TID, as trapped charge can drive the transistors from their back gates [106].

6.2 IC techniques to face TID effects

The effects reported in the previous Section 6.1 are particularly dramatic for high-dose levels, as shown in Fig. 6.3. Therefore, techniques to mitigate their consequences have to be adopted.

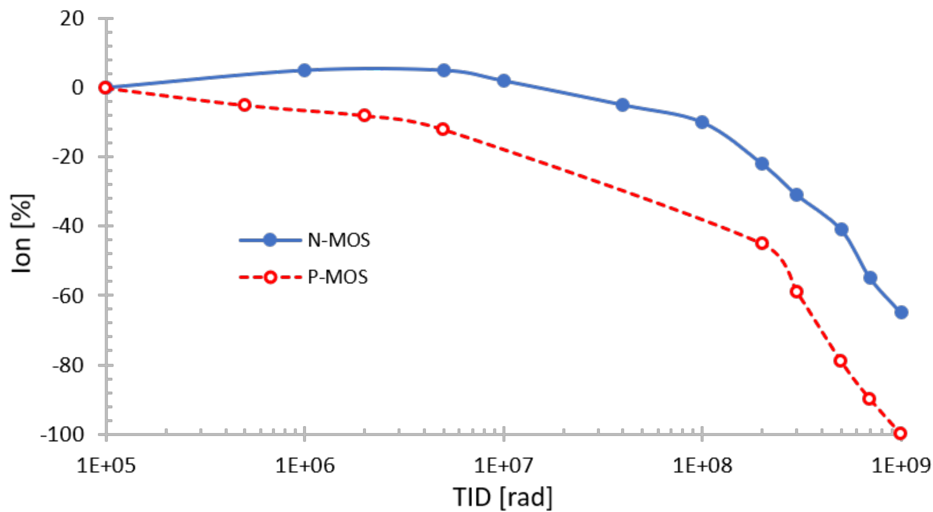

Figure 6.3: *Percent current loss of minimum size N-MOSFETs and P-MOSFETs connected as a diode for different TID levels in the target 65 nm technology [103].*

6.2.1 Enclosed Layout Transistors

One of the main effects that makes such huge performance degradation is due to STI. When the STI dielectric is struck by ions or radiation, e-h pairs are generated and the same effects discuss in Section 6.1 for the gate-oxide are obtained. The positive charge trapped near the channel creates parasitic MOSFETs that are mainly responsible for leakage current in N-MOSFETs. Furthermore, the creation of interface defects, trapping charge, creates an electrical field that leads to narrow channel effects [103]. A solution to fix this problem is avoiding the edge between the gate and the STI, designing circular gate shape MOSFETs, as in Fig. 6.4, called Enclosed Layout Transistor or Edge Less Transistor (ELT) [107]. The MOSFET drain has usually higher resistance than the source, making it a hot node for SEE. The inner well of the ELT MOSFET shape, having a lower area than the external one, is the best candidate to be used as the drain terminal, reducing the sensitive area. A comparison between Figs. 6.3 and 6.5 shows the improvement performance using ELT layout for N and P-MOSFETs, in particular the robustness again the radiation increases of 15% for N-MOSFETs and 10% for P-MOSFETs [104]. On the other hand, the use of ELT leads to use more area for the layout (nearly 2% more for each MOSFET) and imposes a minimum MOSFET width of 1.3 µm to meet the fabrication rules. In addition, these MOSFETs layout needs ad-hoc models and tools for electrical simulations and for recognition of the circular shapes in the LVS (Layout vs. Schematic) check.

6.2.2 Minimum Length

Fig. 6.5 shows a performance increase with an increase in transistors length. This is related to LDD spacer oxide effects. LDDs are next to gate oxide and have a higher thickness, so the radiation effects on these structures influence whole MOSFET performance. Two main effects are due to LDDs spacers, the first is the increment of the MOSFET in series resistance due to charge trapped in the spacer oxide or at its

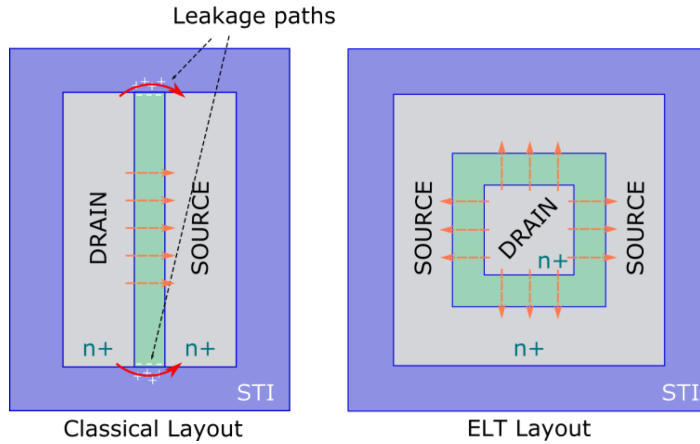

Figure 6.4: *Classical (left) and ELT (right) MOSFET layout structure. In the classical layout the leakage paths, due to radiation charge in STI, are highlighted.*

interface. The second is due to H+, which can move near the channel provoking V_{th} shift [104]. The use of long transistors allows reducing the contribution of these effects on the MOSFETs performance, having a low channel percentage near the LDDs. Obviously, the use of long MOSFETs means reducing their transconductance or increasing MOSFET capacitances if the W/L ratio is kept constant. Therefore, the use of long MOSFETs can be a solution only for low-speed applications.

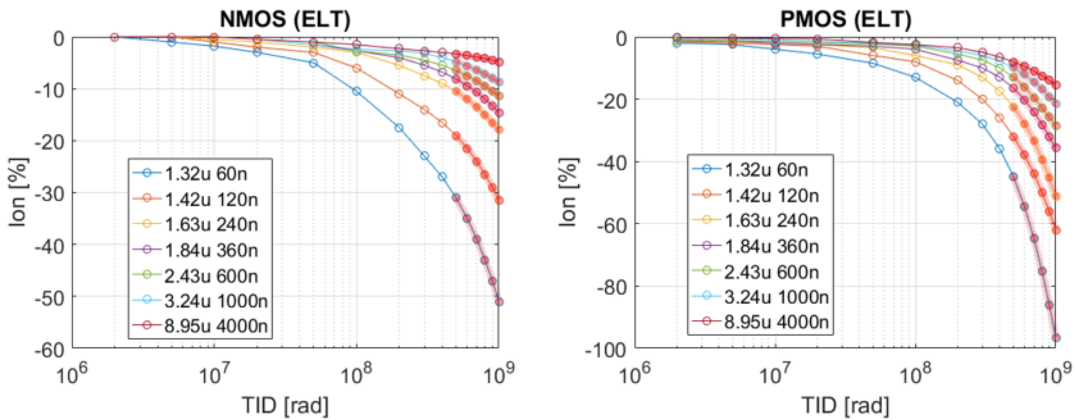

Figure 6.5: *Percent current loss of N-MOSFETs (left) and P-MOSFETs (right) connected as a diode for different TID levels in the target 65 nm technology. The data up to 400 Mrad are extracted from [103], the other are extracted with an interpolation algorithm.*

6.2.3 CMOS vs. CML approach

The dramatic effects that radiations cause on the P-MOSFETs transconductance, mobility and threshold voltage than N-MOSFETs ones on equal conditions, makes the CMOS approach not the winner choice for high-speed high-dose applications. One of the alternatives to the classic CMOS implementation is the CML (Current Mode Logic) logic, which using only resistors and N-MOSFETs, shows better performances when the electronic system is exposed to high-radiation environments. Hereafter, the com-

parisons between two basic D flip-flops (DFFs) designed in 65 nm CMOS and CML technology are shown when they operate in typical conditions and when they are exposed to radiation. The simulation models used for the exposition to 1 Grad is reported in Section 6.2.4.

CMOS D Flip-flop

The CMOS-DFF chosen for the system evaluation is the classical 16 transistors static DFF shown in Fig. 6.6. The MOSFETs are sized to face high-speed switching (10 Gbps) and high TID, adopting the previously described RHBD techniques. In order to reduce the radiation effects, the chosen MOSFETs length is 120 nm and the width of the N-MOSFETs and P-MOSFETs are 4 μm and 12 μm, respectively.

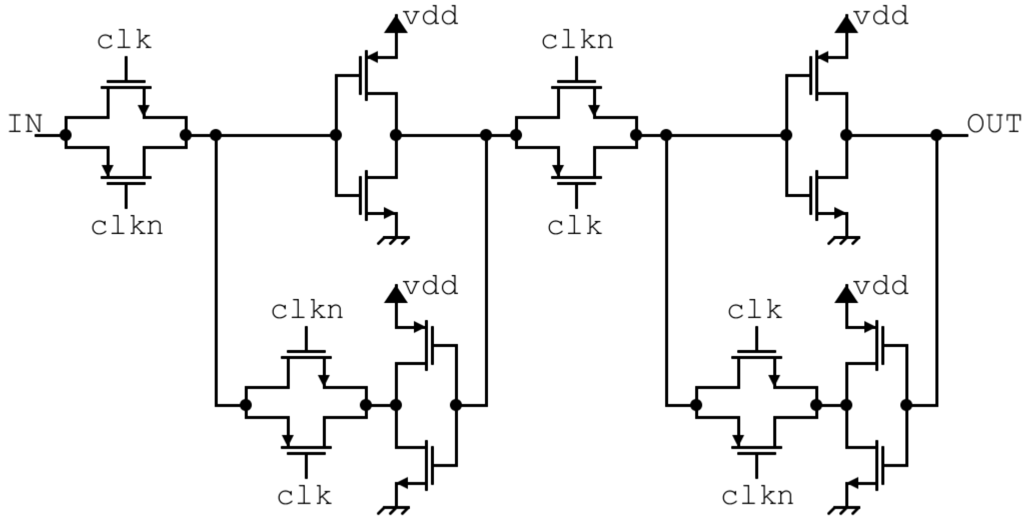

Figure 6.6: *Schematic of the CMOS 16 transistors D flip-flop*

In Fig. 6.7 is shown the 10 Gbps eye diagram of the CMOS-DFF operating in typical condition. When the CMOS-DFF is exposed to 500 Mrad TID, it shows a significant reduction of the maximum switching frequency, which decreases to 3.5 Gbps. This is mainly due to P-MOSFETs degradation, which not allows the fast commutation of not-gates. As shown in Fig. 6.8, although the adoption of the previously described RHBD techniques, used to face the high TID levels, the P-MOSFETs degradation effects are extremely strong for 1 Grad TID exposition, reducing the maximum switching frequency at only 2.5 Gbps.

CML D Flip-flop

In Fig. 6.9 is shown the schematic of a CML-DFF, which implements two latches with the classic two differential couples, one to impose the signal and the other for level regeneration. This technology uses differential signals to reject common-mode disturbs and a voltage swing of 400 mV for higher switching frequency. It is sized with 4 μm signal MOSFETs (the transistors having IN1 and IN2 signals on their gate), 8 μm clock MOSFETs (the transistors having clk and clkn on their gate), 24 μm for the current tails MOSFETs. The switching transistors have 120 nm length, instead, the tail current

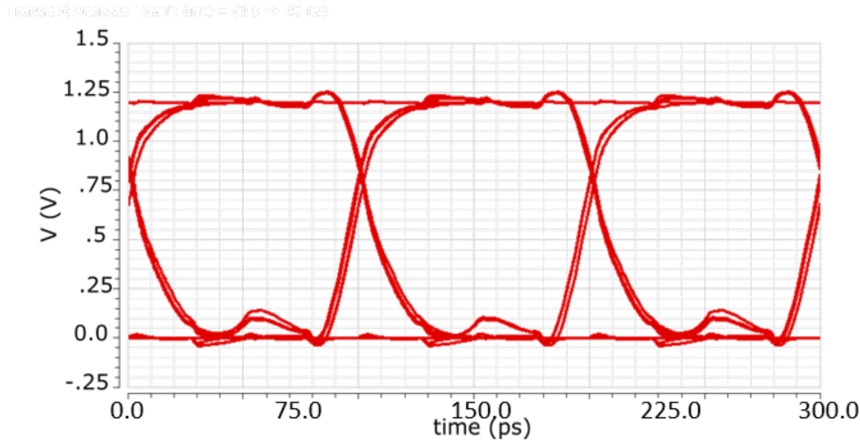

Figure 6.7: *10 Gbps eye diagram of the CMOS D flip-flop operating in typical condition.*

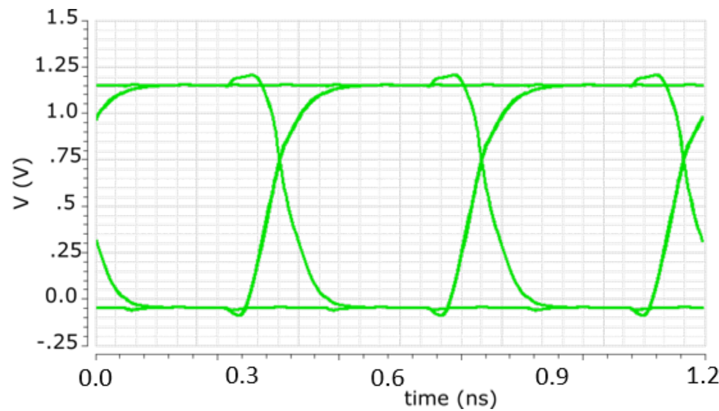

Figure 6.8: *2.5 Gbps eye diagram of the CMOS D flip-flop when exposed to 1 Grad TID.*

MOSFETs have 240 nm length.
Under high TID the CML-DFF presents only slightly performance degradation in comparison with the CMOS cell. The simulations with the irradiated models, presented in Section 6.2.4, highlight that the CML-DFF works at 10 Gbps also when exposed to 1 Grad TID only with a decrement on the eye-opening of 50 mV, as shown in Fig. 6.10. Where the green trace is the output response of the CML-DFF in typical condition, the yellow and the red traces are the results for 500 Mrad and 1 Grad exposition, respectively.

6.2.4 1 Grad (SiO_2) MOSFET models development

Today, in literature, only a few 65 nm technology irradiation data of minimum size MOSFETs exposed up to 1 Grad (SiO_2) are present [102–105]. It is worth highlighting that even recent rad-hard chips in literature or in the market are not able to work at dose levels close to 1 Grad (SiO_2). For example, the 1.2 Gbps readout circuit in [41] is able to operate up to 600 Mrad (SiO_2). Therefore, in order to design a system and predict its behavior at high TID levels, a model for N-MOSFETs and P-MOSFETs, exposed to a high dose level, is developed starting from literature data extracted from the same commercial-grade technology [102–105, 108]. The MOSFETs properties like

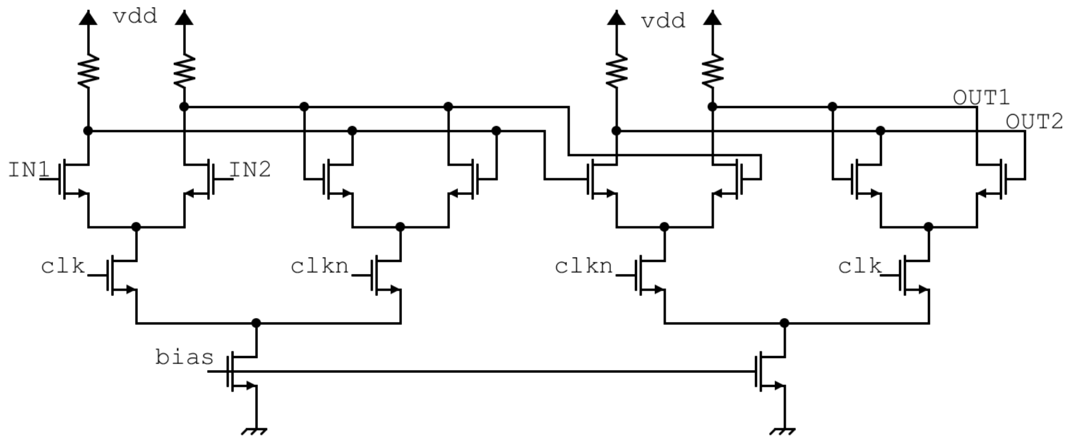

Figure 6.9: *Schematic of the CML D flip-flop*

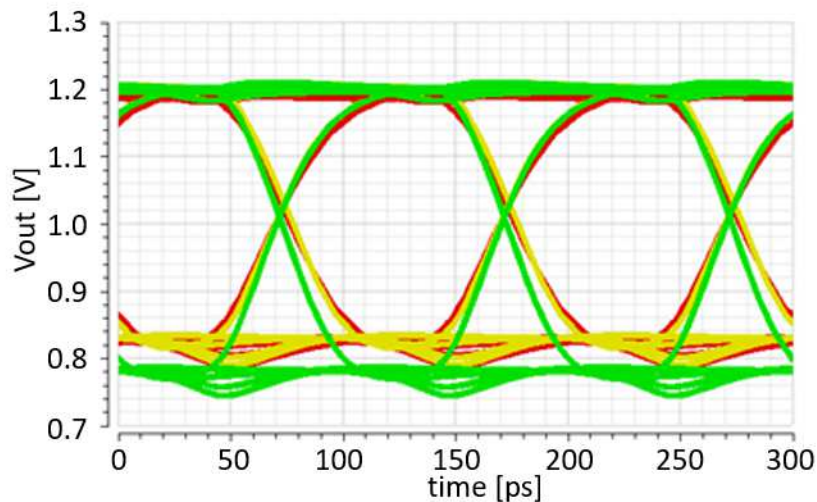

Figure 6.10: *Eye diagram of the CML DFF output signals at 10 Gbps for typical (green trace), 500 Mrad (yellow trace) and 1 Grad TID (red trace)*

threshold voltage, offset voltage, electrical mobility and subthreshold swing are set in a BSIM (Berkeley Short-channel IGFET Model) model, for different widths and lengths, in order to simulate the DC behavior of different MOSFET shapes. In particular, the data of the variation of the N-MOSFET threshold voltage and subthreshold swing up to 1 Grad (SiO_2), for different transistors lengths, are extracted from [102], while those for P-MOSFETs are extracted from data in [105]. The variation of threshold voltage for both MOSFET types, for different widths, up to 1 Grad (SiO_2) is extracted from data in [104]. The variation of the offset voltage, for both MOSFETs types, for different lengths, is extracted from [102]. The reduction in electrical mobility for both MOSFET types is extrapolated from the effects on ON-current of MOSFETs exposed up to 1 Grad (SiO_2), for different transistor widths and lengths that are available in [102]. Afterward, the models were verified using the ON-current vs. V_{gs} characteristic, for different transistors size reported in [102]. The purpose of these DC models is to provide some

first instruments, at simulation levels, to develop RHBD techniques for the system that must work in an irradiated environment.

6.3 Single Event Effects

A SEE occurs when a particle with enough energy traverses an electronic device, leaving a high density of ionized electron-hole pairs (ehps) in its wake. This phenomenon can generate destructive and nondestructive effects. Nondestructive SEEs destroy data states but do not affect devices permanently, whereas destructive SEEs destroy the data state and permanently damage or destroy devices. The SEE effects on a specific technology depend on the ion LET, trajectory, energy, local layout, biasing, layers, and a myriad of other device and circuit details. However, the main effects due to particles hitting appear in the region with strong electrical fields, able to physically separate the ehps particles. The reverse-biased junction is the most charge-sensitive part of microelectronics. Indeed, silicon radiation detectors are large area diodes that are reverse-biased for high electrical field creation, which is particularly effective at separating electrons and holes before they can recombine. The silicon technologies, both BJT or CMOS technologies, are filled with reverse-biased junctions sensitive to particle strike. In Fig. 6.11 is shown a basic N-MOSFET structure and the process that generates the SEE.

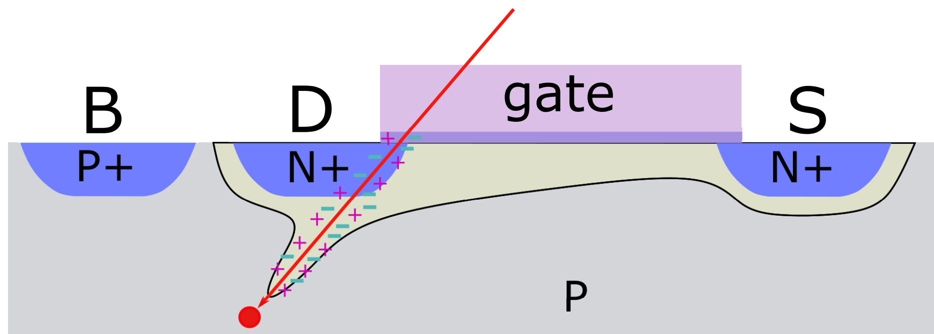

Figure 6.11: *e-h pair generation due to ionizing particle strike in semiconductor device.*

The SEE events can generate different effects depending on the system that affect. If the event occurs in a sequential logic or memory components, the SEE transforms into persistent errors and generates Single Event Upset (SEU), corrupting the data. This effect can be generated also in combinatorial logic if the SEE can propagate to the input of sequential logic, and then latched in at the next clock. The probability that a SEE will be captured as an SEU in sequential components increases linearly with frequency because the number of clock edges increases with increasing clock frequency. In analog components like amplifiers and comparators, SEE will cause a short-lived transient disturbance on the output of the device. The duration, shape, and magnitude of SEE highly depend on which part of the amplifier the ion hits. One additional area where SEEs cause system-reliability issues is in power devices, as shown in Section 4.3.2. Although most SEEs are nondestructive, they impact on system availability. For example, in Section 4.3.2 is detailed shown as, even though the loading devices are not damaged by high-voltage fault, the SEEs that occur in the IC DC/DC converter can create same power discontinuity. While small glitches can be tolerated, large-magnitude

undershoots can lead to data corruption and/or resets in downstream systems. To be noticed that overshoots on the output of power devices, in Section 4.3.2 avoided by the inductorless insulator stage, are much more problematic than power discontinuity because they can cause permanent damages.

6.4 IC techniques to face SEE effects

As space applications are more affects by SEE than TID the study of solutions to deal with the impact of energetic heavy ions or protons is more widespread in literature [109]. Therefore, techniques as triple redundancy and error correction code are pervasive in a radiated environment [110]. Being space, the main market of rad-hard devices and having TID lower than 1 Mrad [6], the effort to develop systems to reduce the TID effects is significantly lower than that to face SEE. Hence, for this reason, in this thesis work, techniques as spatial and time redundancy [111] and SEU-hardened digital cells [112] are not discussed, leaving space to some consideration on the comparison between the SEE-tolerant properties of the classical CMOS technology and the CML technology used for the drivers in Chapter 7.
The main differences between the two architectures for a SEE point of view are:

- *Voltage swing*: the probability of SEU occurring in a digital system is straightly related to the voltage gap between high and low levels. Obviously, this depends on the power supply level but also on the digital circuit architecture. Although, as shown in Figs. 6.8 and 6.10, the CML technology is more TID-tolerant than CMOS one, it has lower voltage swing. This on a side allows achieving higher bit-rate performances but on the other makes the system more sensitive to SEU. Indeed, a lower voltage shift on the hit node is needed to flip the information stored. In CML logic the voltage swing has to be able to fully unbalancing the differential couple and it depends on the technology node. For example, the swing required for the 65 nm technology is about 400 mV, which, considering a power supply of 1.2 V, makes the CML logic three times more sensitive to SEE than CMOS logic (only for the digital level swing point of view).

- *Capacitance nodes*: the previous comparison on the logic level swing is not the only affecting the SEE-hardness. The lower voltage swing of the CML logic allows achieving higher data speed, considering the same device size. However, making a comparison at the same speed rate is possible to use larger CML devices than CMOS ones, reducing the SEEs effects. Indeed, wide devices increase the equivalent capacitance of the circuit nodes, allowing a lower voltage swing of the hit node.

- *Charge sharing*: the differential nature of the CML logic has the advantage to reject the common-mode disturbs. The effects generated by TID radiation can be clearly associated with common-mode disturbs and partially compensated by differential structures. This property of differential structures can be used also for SEE mitigation. Indeed, thanks to the technology scaling, the size of the funnel generated by particle strike interests more adjacent devices, leading to charge redistribution on these devices. If the fingers of the two devices of the differential

couple are interdigitated, the effect of charge sharing becomes a common mode disturbs which is mitigated by the differential structure, see Fig. 6.12.

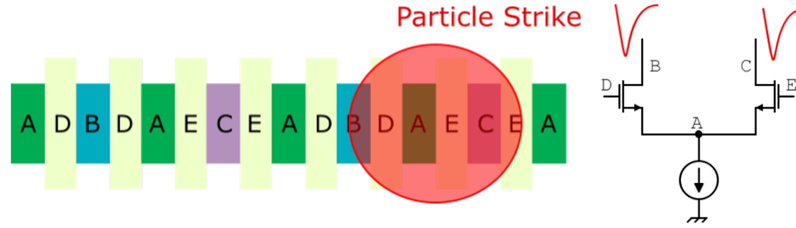

Figure 6.12: *The particle strike affects more adjacent devices. If the devices interested are the MOSFETs of a differential couple, the SEE effects can be mitigated.*

- *N-well free*: as detailed described in Section 6.1, one the solution adopted to work at very high-level doses is the not use of P-MOSFETs. This solution has positive effects also on the SEE-hardness. In particular, not using P-MOSFETs the IC is N-well-free. This prevents the occurrence of latch-ups generate by particles strike, thanks to the absence of parasitic npn nor pnp BJTs in the substrate.

In response to the previous consideration is not possible saying if the CML logic is more or less SEE hard than CMOS one because it depends on the single-cell sizing and on its layout. What can be truly considered is that, when voltage scaling occurs with advanced digital circuits, it takes less injected charge to create digital levels flips. Thus, more advanced higher-speed technologies are potentially more sensitive to SEUs induced by SEE, because both their occurrence probability and their ability to propagate over multiple stages has increased with each new subsequent technology node. Hereafter, the comparison between the SEE performances of the CMOS-DFF and CML-DFF cells, described in Section 6.1, are showed.

6.4.1 CMOS-DFF and CML-DFF SEE Comparison

The simulations to predict the SEE effects on a system can be performed modeling the electrical behavior that ions strike generate on the circuit nodes. The ehps, generated in a reversed-bias junction affected by ion strike, are separated and following the electrical paths create an impulsive current in the circuit node connected with the junction. This phenomenon could be electrical simulated adding, at the nodes of the electrical circuit, some current generators with a double exponential waveform like Eq. 6.1, represented in Fig. 6.13.

$$I(t) = \frac{Q}{\tau_a \cdot \tau_b}(e^{-\frac{t-t_d}{\tau_a}} - e^{-\frac{t-t_d}{\tau_b}}) \tag{6.1}$$

Where Q is the charge generated with the particle strike, t_d is the injection instant, τ_a and τ_b are the constant time of particle generation and recombination. All the constants depend on the particle LET and technology used [113, 114].

The effects that this current pulse has on the circuit depends on the impedance of the node where it is applied. The higher is the node impedance and the greater is the voltage pulse that could generate SEU. Hence, in order to evaluate the worst-case

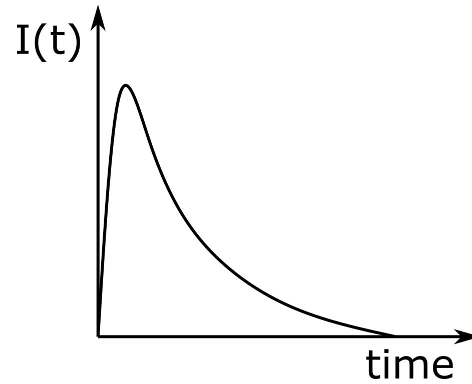

Figure 6.13: *Electrical modeling of a particle strike effects. A first fast phase of ehps generation in followed by a slower recombination phase.*

effects generated by SEE on the previous CMOS-DFF and CML-DFF, high impedance nodes are selected as target nodes.

SEE on CMOS-DFF

The high-impedance selected node for SEE is highlighted in Fig. 6.14. The SEE simulation was performed by implementing the Eq. 6.1 in the equivalent current generator by veriloga programming language. In Table 6.1 are listed the values of the equation parameters used in the equivalent current generator. Four particles with different energy are used to SEE simulations.

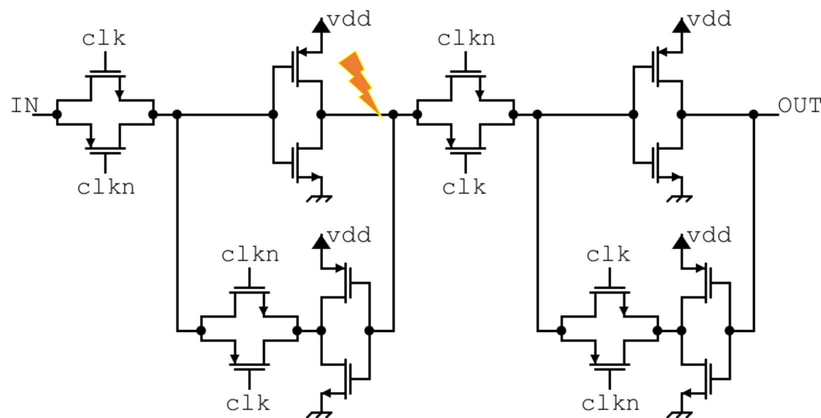

Figure 6.14: *Schematic of the CMOS 16 transistors DFF and the hit node.*

Table 6.1: *Parameter of Eq. 6.1 used for SEE CMOS-DFF simulation.*

τ_a (ps)	τ_b (ps)	Q (fF)			
200	50	1	5	10	15

Fig. 6.15 shows the simulation results of four particles impacting on the target node of the CMOS-DFF at 2 ns, 4 ns, 6 ns and 8 ns (blue line). In response to the current

pulse, a voltage shift on the hit node is generated. This voltage, thanks to the feedback of the latch cell is stored creating an SEU, which is then transmitted at the output. Therefore, the high-impedance of the selected node and the strong feedback of the latch cell makes the CMOS-DFF sensitive also to low energy particles with few femto Farads charge released. This type of effect is typically addressed reducing the feedback gain of the latch, which on the other side means reducing the data rate of the CMOS cell [115].

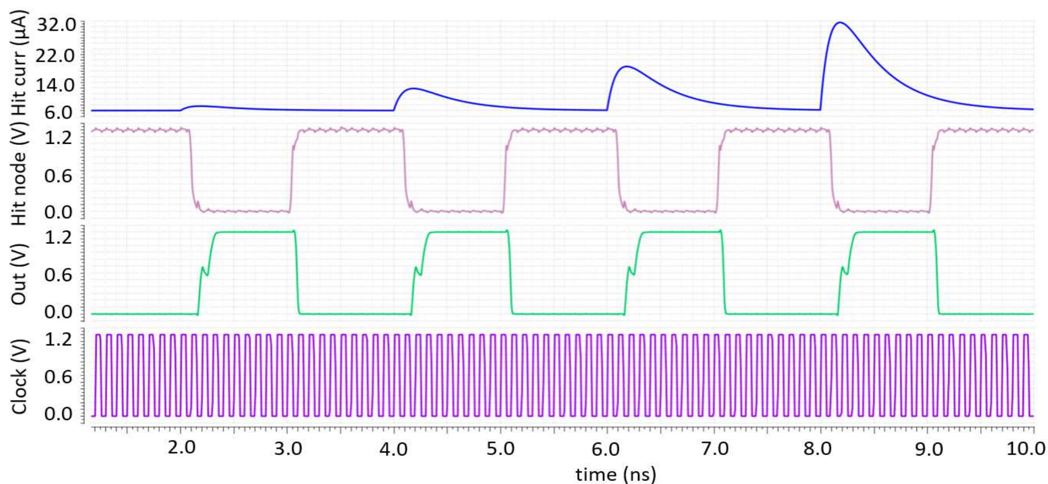

Figure 6.15: *Simulation of the SEE on CMOS-DFF. The blue line represents the current due to a particle strike. The pink line is the voltage on the node hit by particle. The green line is the output of the DFF in response to low-level input plus the effect of particles strike (without the SEE a low-level continuous line should appear). The purple line is the clock of the DFF.*

SEE on CML-DFF

The high-impedance target node of the CML-DFF is the drain of the differential couple, as shown in Fig. 6.16. It is hit with particles having higher energy than the previous CMOS-DFF cell because simulations have highlighted the stronger radiation hardness of this CML cell with respect to the CMOS cell. In Table 6.2 are listed the parameter used in the equivalent SEE generator.

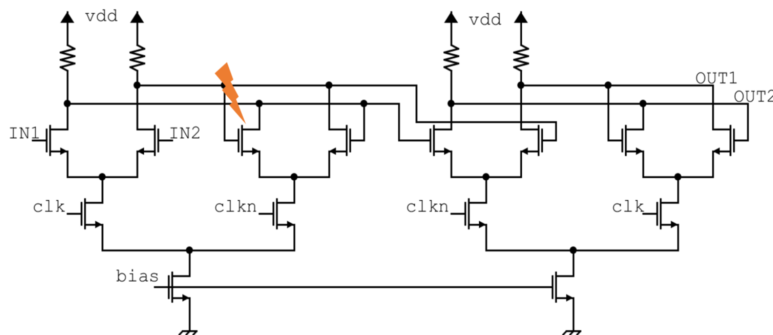

Figure 6.16: *Schematic of the CML-DFF and the hit node.*

Table 6.2: *Parameter of Eq. 6.1 used for SEE CML-DFF simulations.*

τ_a (ps)	τ_b (ps)	Q (fF)			
200	50	10	50	100	150
400	100	100	300	600	900

In Fig. 6.17 is showed the simulation results of four SEE events with the value listed in the first row of Table 6.2. The brown line represents the current value injected to simulate the SEE. The orange line is the voltage generated by the SEE on the hit node and the red line is the voltage level on the other differential node. As shown, the SEE affects both differential signals, in a greater way the signal of the target node (orange) and in a lower way its counterpart signal. This effect is due to the CML latch used to restore the logic levels (second differential couple starting from left in Fig. 6.17). The purple and green lines in Fig. 6.17 are the output signals of the CML-DFF. The simulation result highlights that the designed CML-DFF is able to withstand charge up to 100 fF without generating SEU. After 100 fF, a flip bit appears at the output of the CML-DFF.

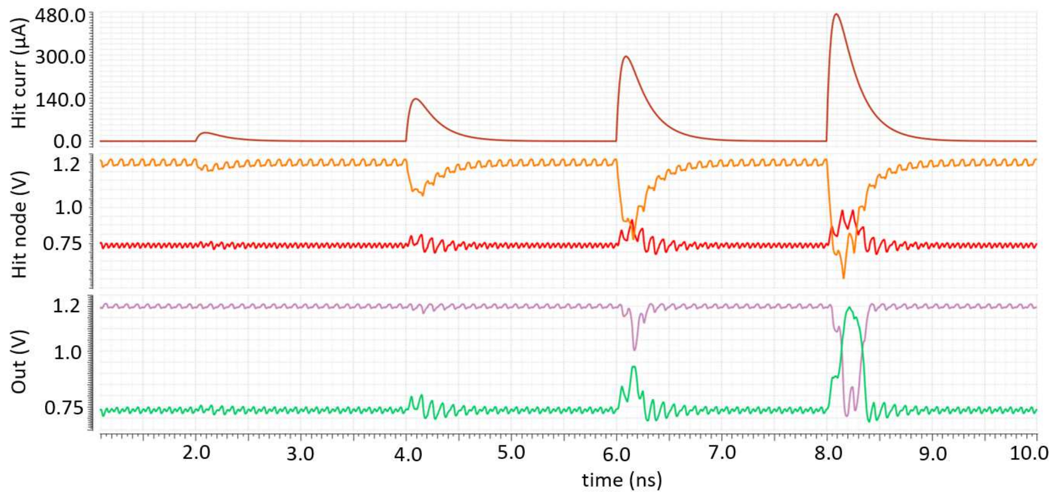

Figure 6.17: *Simulation of ion strike on the node highlighted in Fig. 6.16 with the parameter in the first row of Table 6.2.*

Fig. 6.18 shows the same SEE simulation results but with higher charge values released in a greater time. As shown, the first SEE of Fig. 6.18 releases the same charge of the third SEE of Fig. 6.17 but the dilution of the charge in greater time reduces the SEE effect. This dilution time depends on the particle nature and on its energy.

The simulations of the SEE on CMOS and CML DFFs show the best SEE tolerant performances of the single CML cell with respect to the CMOS one. However, thanks to the triple redundancy techniques, typically used in CMOS approach, the SEE hardness of the CMOS systems are sensibly improved. The use of triple redundancy techniques could improve also the SEE tolerant level of the CML, but, since the much higher power and area consumption of this technology with respect to CMOS, the effort paid for its

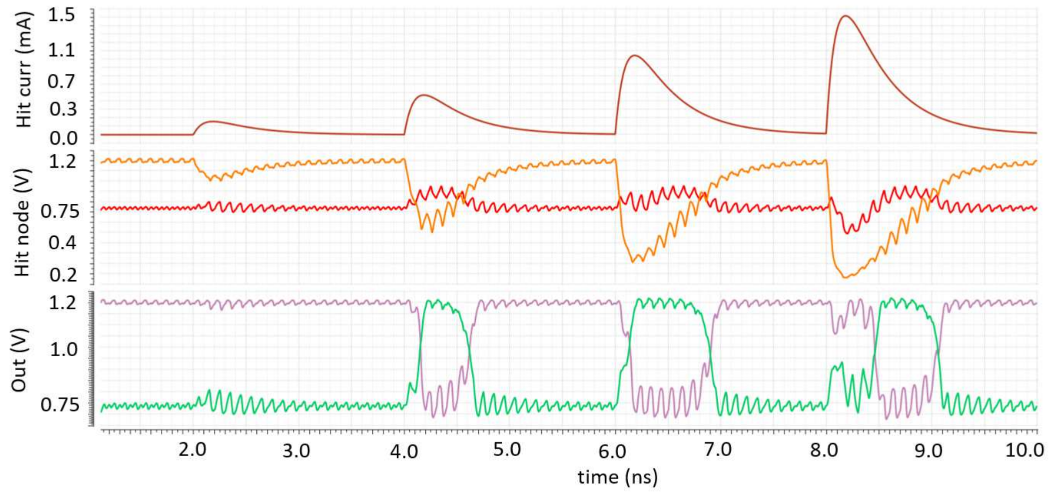

Figure 6.18: *Simulation of ion strike on the node highlighted in Fig. 6.16 with the parameter in the second row of Table 6.2.*

implementation could not be suitable for the application.

CHAPTER 7

High-speed Electro-Optical Modulator Drivers Design

In this Chapter, the techniques for TID and SEE mitigation, presented in Chapter 6, are applied for the design of high-speed radiation-tolerant drivers for electro-optical modulators, targeting the LHC harsh environment, see Chapter 2.

The silicon detectors use reversed biased silicon p-n junction in 2D or 3D structures to reveal the charge left by particle interaction. This charge is collected by the front-end and amplified. The signal generated is shaped and converted into digital data [116]. Then the information is extracted from the front-end using optical links, for their high bandwidth-distance product, their low mass and their resilience against electromagnetic interferences [117]. Today, these links are based on Vertical Cavity Surface Emitting Lasers (VCSELs), which have been qualified for the current LHC experiments [118, 119]. However, considering the next upgrade with a forecasted luminosity increase for 5 – 7 times, a sensible degradation of the VCSELs performance is expected [120], see Chapter 2. One of the most promising technologies currently investigated to face higher radiation levels is based on Silicon Photonics optical modulators. In particular two devices are the target optical modulators for the next upgrade:

- Mach Zehnder Modulator (MZM)
- Ring Resonator (RR)

7.1 MZM and RR

The MZM is an interferometry modulator that splits light equally into two separate optical arms and then recombines the two optical waves. If the two waves are recombined in phase, they will create a constructive interference, otherwise, if there is a phase shift of

π between the two optical signals, they will create a destructive interference [121–123], see Fig. 7.1. This modulation result is driven by electrical signals, which, driving the p-n junction of the optical waveguides, increase or decrease the number of electrical carriers. As a consequence, the refraction index of the paths in the optical waveguides is affected, shifting the phase of the two optical signals [124]. The voltage swing required to drive the MZM is strictly related to its length. The longer the two arms are the lower is the V_π (driving signals voltage value to reach the π phase shift between the two arms). However, the longer the arms are and the higher the optical losses inside the material are. Hence, a short MZM with high V_π is the best choice for an optical power budget analysis, allowing reaching longer distances with lower laser power. From an electrical point of view, the high V_π requirement fights with the high-speed target and the high-radiation level requirements. Therefore, a trade-off between electrical and optical world has to be found. The target MZM chosen for the application is 1.5 mm long and requires an amplitude for the differential signals of about 2 Vpp to reach the desired modulation performance.

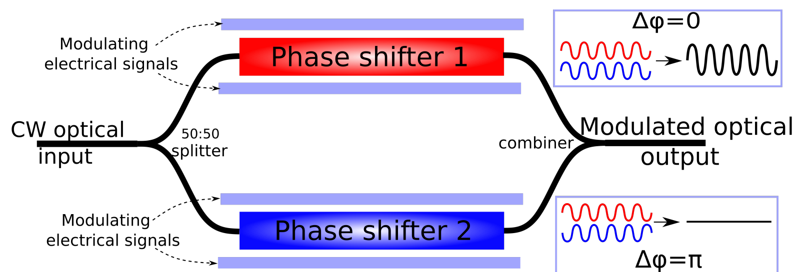

Figure 7.1: *Architecture and functionality of the MZM.*

The ring resonator consists of an optical waveguide which is looped back on itself, such that resonance occurs when the optical path length of the resonator is exactly a whole number of wavelengths. By changing the refraction index of the ring, it is possible to shift the resonance peak, see Fig. 7.2. This, as in the MZM case, is made driving a p-n junction to create a depletion region with a variable number of electrical carriers [125, 126]. The RR has slightly lighter constraints, requiring only driving signals with a differential amplitude of 1.5 Vpp.

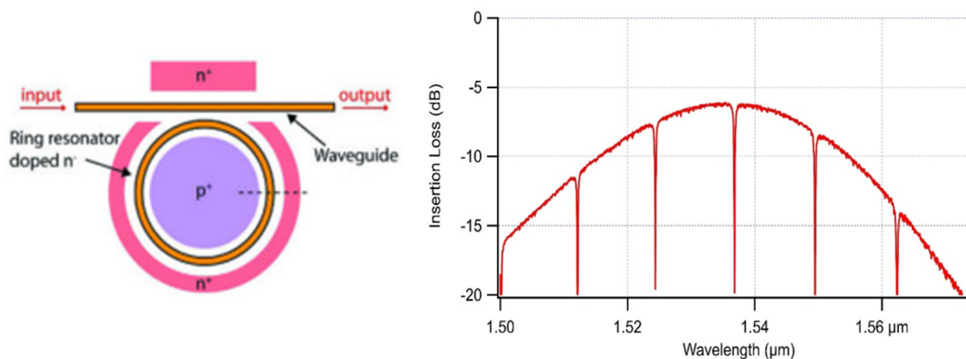

Figure 7.2: *Architecture and functionality of the RR.*

7.2 Drivers Design

Two drivers are designed for the two optical modulators, using the radiation hard technique detailed displayed in Chapter 6. The combination of high-speed links and the P-MOSFETs damaging in the high-dose environment makes these P-MOSFET devices not useful for this application. Therefore, the drivers are designed using CML technology, which, using only N-MOSFETs and passive devices, is more suitable for this harsh environment, see Chapter 6. Nevertheless, its Achille's heel is the static power consumption that is higher than CMOS technology, making its use not suitable for low-speed low-power applications. The minimum MOSFETs length used for this application is 120 nm, which is chosen to partially compensate for the TID damage on N-MOSFETs exposed to radiation. Indeed, the degradation of 120 nm transistor performance is 20% smaller than in the case where the minimum size allowed by the technology (60 nm) is used, see Fig. 6.5. The suitability of 120 nm minimal length choice in terms of TID robustness is verified by experimental measurements up to 800 Mrad (SiO_2) in Section 7.4.3. This choice improves the irradiated N-MOSFETs performances but on the other hand halves the maximum cut-off frequency available in the target technology. In terms of signal speed, the use of double-length MOSFETs for these drivers is partially compensated by the lower CML signals swing than the CMOS one. Fig. 7.3 shows the architecture of the chip designed to integrate both drivers. The two drivers share the same first receiver stage and then the signals are split to feed the remaining blocks. This solution is adopted only for test purposes, due to the limited number of pads available for the input signals. All other pads are used for different circuits designed in the same chip, but whose analysis is out of the scope of this thesis.

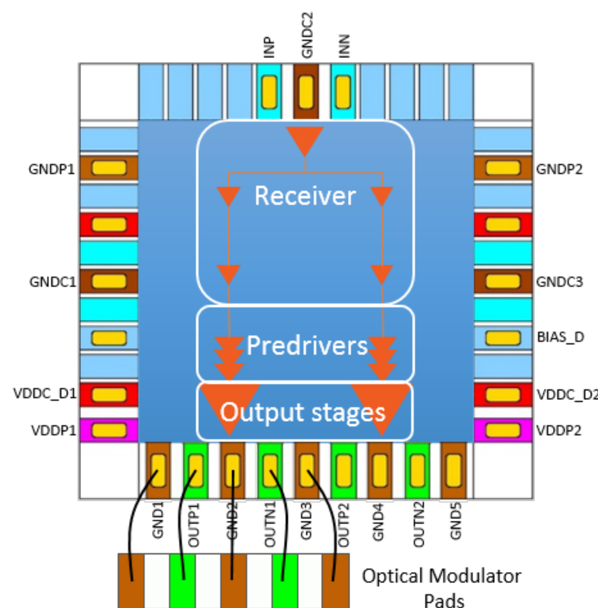

Figure 7.3: *Chip architecture where only receiver, pre-drivers and output stages are highlighted. A schematic of the direct bonding between the drivers chip and the GSGSG pads of one of the optical modulators are also displayed.*

7.2.1 Output stages design

The 2 Vpp required by the MZM makes challenging the design of the driver in the target 65 nm. Indeed, the use of 2.5 V MOSFETs, available in this technology, is avoided even though they are typically used for I/O interfaces. This choice is driven by their thicker gate oxide than core MOSFETs one, which reduces the radiation hardness of the 2.5 V MOSFETs. The core MOSFETs used in the whole chip are able to sustain only 1.2 V, therefore the generation of the required driving voltage is handled by using a cascode architecture and 2.4 V supply voltage in the last stage, as shown in Fig. 7.4. The cascode architecture allows sharing the high-voltage on the two stacked MOSFETs, preventing them from being damaged. The two drivers, one for RR and one for MZM, have the same configuration but a different output stage. The RRs, having a really small size, do not use termination, therefore a 50 Ω internal termination connected to the power supply is used. In addition, an inductor of 800 pH is connected in series to the termination for bandwidth extension, which is mainly limited by 600 fF equivalent capacitance of pads and ESD circuit protections, specially designed for high dose levels. The inductor used is a differential inductor for a lower layout size than two separate inductors. The MZMs have typically a 50 Ω termination connected to ground, but a termination connected to the power supply is preferable. In this way an open-drain driver could be used without creating a high AC impedance inside the chip, preventing signal partitioning and so amplitude losses. To achieve the required output signal amplitude, also in high TID condition, the output stage MOSFETs are sized with wide widths. The MOSFETs of the cascode stage have 620 µm width and the differential couple is sized with 410 µm MOSFET width. As a consequence of this sizing the previous stages are loaded with 305.7 fF equivalent capacitance, thus making necessary the use of pre-driver stages for both drivers.

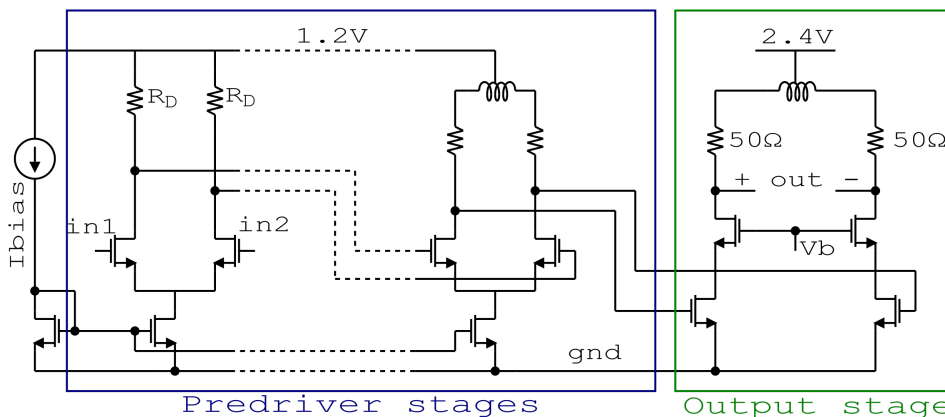

Figure 7.4: *Schematic of the CML pre-driver stages and output stage. The RR-driver uses the internal 50 Ω termination plus a series inductor. The MZM-driver has an open drain configuration. For the sake of clarity, only 2 pre-driver stages are shown. The number of actual stages, preceding the output stage of each driver, is five. The bias current for the tail current mirrors is provided from an external source using the BIAS_D pad in Fig. 7.3.*

7.2.2 Pre-driver stages design

The pre-driver is a cascade of 'N' CML buffers with increasing size, designed considering the spectral power density of a random signal at clock frequency f_{clk}, which is made by nulls at multiples of the clock rate and a -20 dB/dec slope from f_{clk} up to the knee frequency (f_{knee}). Beyond the f_{knee} the spectrum roils off much faster than -20 dB/dec [127]. The f_{knee}, which could be considered as the maximum significant frequency of the random signal, does not depend on the f_{clk} but only on the rise time of the signal. The relation between the f_{knee} and the rise time is expressed in Eq. 7.1, where t_r is the rise time of the signal. For this application, considering t_r equal to 20% of the period and 5 Gbps data rate, the f_{knee} is 6.25 GHz and the constant time is equal to 25.46 ps.

$$f_{knee} = \frac{1}{2 \cdot t_r} \tag{7.1}$$

The total time constant of a buffer chain with tapered factor k is expressed in Eq. 7.2, using the open-circuit-time-constant technique.

$$\tau = N \cdot R_D \cdot \{C_{gd} + C_{db} + k[C_{gs} + (1 + A)C_{gd}]\} \tag{7.2}$$

In Eq. 7.2, R_D is the pull-up resistance of the CML stages, C_{xy} are the x – y capacitances and A is the small signal voltage gain of a single buffer. The expression (1+A) C_{gd} represents the Miller effect on the C_{gd} capacitance of the following stage. The tapered factor k and the number of stages are chosen to minimize the delay time of the buffer chain and to reduce the loading effects on the receiver stage, therefore values of 2.7 and 5 are adopted, respectively, as already well known from the relationship reported in [128] for a generic CMOS buffer chain. For the sizing of the single buffer stage, the Eq. 7.2 can be rewritten as Eq. 7.3, where C'_{xy} are the x – y capacitances for width unit, f_t is the cut-off frequency, V_{te} is half of the MOSFET overdrive (V_{te} = (V_{gs}-V_{th})/2) and ΔV is the logic swing of the CML stages.

$$\tau = N \frac{\Delta V}{C'_{gs} \cdot f_t \cdot V_{te}} [C'_{db} + C'_{gs} + k(1 + (1 + A)k)C'_{gd}] \tag{7.3}$$

In order to minimize τ, f_t should be maximized choosing a current density value of the couple MOSFETs around 0.2 mA/µm, which is known to be technology independent [129]. However, to keep the tail MOSFET in saturation with a low voltage power supply, also for high radiation levels, a current density of 0.1 mA/µm is adopted. The logic swing ΔV, which is fixed by the tail current and the pull-up resistance (ΔV = $R_D \cdot I_T$, where I_T is the tail current), should be minimized to improve the delay. However, this voltage is determined by the minimum voltage required to fully switch the tail current in the differential pair. Thanks to the $I_{ds}(V_{gs})$ MOSFETs characteristic for the selected current density, and accounting the margin required to work in such a harsh environment, a logic swing value of 400 mV is fixed for the buffer stages of the pre-driver. Although the small-signal voltage gain, A in Eqs. 7.2 and 7.3, has to be minimized to reduce the Miller effect on the capacitance of the following stage, it must still be greater than unity to maintain the regenerative properties of the CML logic family. For this reason, a minimum gain of 1.5 is chosen to address the radiation

effects. The first stage of the pre-driver is sized for a tail current of 0.5 mA and using a differential couple width of 4 µm and length of 120 nm. This sizing guarantees the performance required from the stage also at high radiation levels. The sizing of the other pre-driver stages is omitted in this thesis because from the sizing of this first stage it is possible to reconstruct that of the other stages. In order to drive the output stage, the lower signal level of the last pre-driver has to be a value lower than 400 mV, thus the signals should have a voltage swing of at least 800 mV. To compensate for the effect of signal speed reduction, an inductor is used together with the pull-up resistor to create an inductive peaking technique [130, 131], which enhances the bandwidth of the last pre-driver stage. The inductors of the peaking technique are typically sized considering the Eq. 7.4, where R_D is the pull-up resistance, C_D is the load capacitance and α is a proportional coefficient typically set to 0.4 to get the maximally flat gain response [131]. For this application, a parameter α of 1.3 is adopted for the generation of 3.5 dB pre-emphasis peak to compensate for the high-frequency attenuation of the previous stages. A differential inductor is used to minimize the layout area. In addition, it is worth noting that the inductor is connected in series to the pull-up resistors. This simplifies the inductor choice since a high Q factor is not required.

$$L = \alpha \cdot R_D^2 \cdot C_D \tag{7.4}$$

7.2.3 Receiver

For application constraints, the input pads of the drivers are placed on the opposite side of the output pads. Therefore, a distributed receiver is used to bring the high-speed signals at the input of the two drivers. The receiver is made by three CML stages, as shown in Fig. 7.3. The first stage is a CML stage with a broadband matching impedance. After the first stage, the signal path is split into two paths, each one made by two identical CML stages. The first stage, driving two CML buffers, has double size than the others to allow not to lose the bandwidth of the input signals. The other two CML buffers with identical size are just used to connect the input signals with the driver, placed in the other chip side, compensating for the parasitic capacitance of the paths.

7.2.4 Power Consumption and Power Supply Rejection Ratio

Table 7.1 shows the power consumption, obtained with post-layout simulations, of the MZM driver stages for typical condition and after being exposed to 1 Grad (SiO_2) dose. The values of the receiver and pre-driver stages, before and after being exposed to radiation, are comparable because the bias current has been increased for partial compensation of TID effects. The output stage, having no bias current control shows a higher reduction of the power consumption, explained by the reduction of MOSFET current shown in Section 6.1. The power consumption of the RR driver is not displayed in this thesis for its similarity to that of the MZM driver. The measurements of power consumption cannot be directly performed because the power supply is shared with other devices placed in the same chip. Whole chip-level measurements have shown that power consumption data extracted from post-layout simulations are aligned with real fabricated chip measurements. Table 7.2 shows the PSRR of the two drivers for the

two power supplies. As expected, the PSRR increases with frequency but still be below -21.18 dB for the MZM driver and -25 dB for the RR driver. The two drivers are more sensitive to disturbs on 1.2 V supply than the other because these disturbs are amplified by the pre-driver multi-stages. PSRR measurements on the fabricated chip are aligned with the post-layout simulation data in Table 7.2.

Table 7.1: *Power consumption of the MZM driver stages*

	Receiver (mW)	Pre-driver (mW)	Output stage (mW)
Typical condition	20.4	42.65	35.01
1 Grad (SiO_2)	19.5	40.72	21.65

Table 7.2: *PSRR data of the MZM and RR drivers*

PSRR	VDD (1.2 V)		VDDP (2.4 V)	
Frequency (GHz)	MZM Driver (dB)	RR Driver (dB)	MZM Driver (dB)	RR Driver (dB)
0.1	-50.31	-49.63	-76.60	-76.83
1	-36.98	-36.63	-53.22	-53.90
5	-21.18	-25.00	-30.44	-35.16

7.2.5 SEE Simulations

In addition to the high TID level robustness, the two drivers should address the SEE of high-energy particles generated by the collision of the two proton beam inside the LHC. The nature and energy of these particles depend on the experiment type. Hence, electrical simulations to predict the critical charge, which could generate data corruption, are performed. The same double exponential equivalent model, shown in Section 6.4.1, was used to simulate the effects of charge injection on the drivers circuits nodes. As for the CML-DFF showed in Section 6.4.1, the most sensitive nodes are the drains of the differential couple. The main difference between the CML stages of the designed drivers and the CML-DFF, shown in Section 6.4.1, is the absence of the feedback cell for signal storage and regeneration. This cell reduces the SEE hardness because the SEE effects generated on a signal are mirrored also on the differential counterpart, as shown in Figs. 6.17 and 6.18 (orange and red signals). Therefore the CML cells of the drivers are more radiation hard with respect to the CML-DFF. In order to predict the SEE robustness of the drivers the critical charge of each driver stage is extracted with simulation and listed in Table 7.3. The SEE simulations are performed considering the Eq. 6.1 with $\tau_a = 400$ ps and $\tau_b = 100$ ps. The values listed in Table 7.3 show an increasing trend of the critical charge with the increasing of the stage size (Stage 1 is the first stage of the predriver and Stage 5 is the last stage of the predriver). Indeed, as expected the greater is the MOSFETs size, the higher is the node parasitic capacitance and the lower is the SEE effect. On the other side, the greater is the MOSFET size and the higher is the probability that a high-energy particle hits the sensitive node. This probability can not be considered in the electrical simulation only. Therefore, a merit-factor can be defined as the ratio between the critical charge and the MOSFET area, where the SEE is applied, as listen in the second line of Table 7.3. The first four stages show

nearly the same merit-factor, instead, the last two stages highlight a lower merit-factor, indicating higher sensitivity to SEE. This effect is due to the inductors used to implement the inductive peaking techniques, see Section 7.2.2. These inductors increase the impedance of the nodes where the equivalent SEE generators are applied, increasing the SEE voltage disturbs.
These SEE simulations intend to give a first SEE behavior prediction, the probability that a high-energy particle hits a sensitive area or the effects due to interdigitated layout and charge sharing, discussed in Chapter 6, are not considered in the electrical simulations. Therefore, experimental tests should be performed for better SEE analysis, as shown in Section 7.4.3.

Table 7.3: *Critical charge (Qc) of the MZM driver stages and the merit-factor obtained as the ratio between the Qc and its MOSFET size (W).*

	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Out Stage
Qc [pF]	0.4	1	2.5	7	10	25
Qc/W [pF/μm]	0.1	0.09	0.086	0.089	0.047	0.06

7.2.6 Chip Layout

The full-custom layout of the chip is based on the techniques for radiation effect mitigation displayed in Chapter 6. Indeed, the n-well-free characteristic of this driver architecture excludes the generation of the latch-up problem generated by heavy ions. The layout of all MOSFETs is an interdigitated structure for matching purposes, but also to reduce the common-mode effects of TID described in Chapter 6. All the free layout space is filled with a grid of substrate contacts to ensure a ground potential at the substrate, draining out parasitic charge. Fig. 7.5 shows the layout of the RR driver, whose area is dominated by the two differential inductors. The whole area is 347 μm * 180 μm where 270 μm * 170 μm is the area of the two inductors.

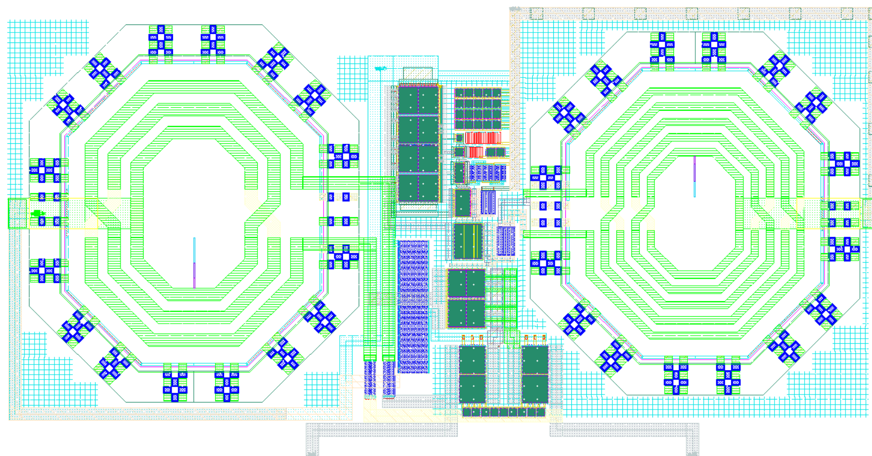

Figure 7.5: *Image of the RR driver layout.*

The layout image of the MZM driver is omitted in this work because it has the same structure as the RR driver but without the left inductor. Therefore, its area is 200 μm

* 180 µm where 140 µm * 170 µm is the area of the inductor. Fig. 7.6 shows the chip layout and the SEM (Scanning Electron Microscope) image of the 1 mm * 1 mm chip fabricated in the 65 nm TSMC technology. Particularly, the layout in Fig. 7.6.a highlights the placement of MZM driver, RR driver and the distributed receiver. To be noted that the differential signals in the distributed receiver layout are as close as possible to each other to reject common-mode disturbs. The ground and the power paths run along the signal paths to reduce the cross talk generated by the other high-speed systems placed on the chip and not discussed in this thesis. The SEM image in Fig. 7.6.b shows the inductors size and the pads placements, while the other structures are covered by metal layers.

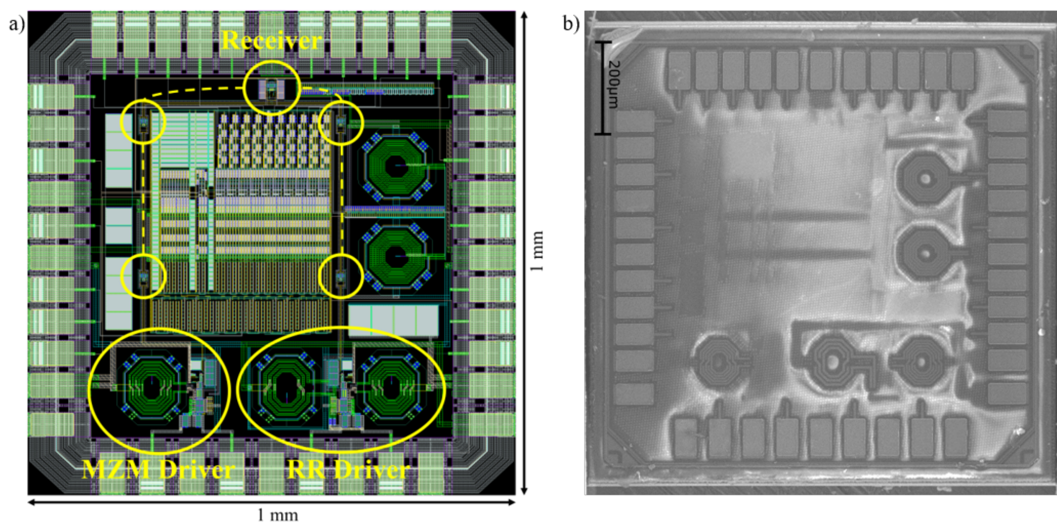

Figure 7.6: *Images of (a) chip layout, where the two drivers and the receiver are highlighted; (b) chip fabricated in 65 nm technology, taken using a SEM.*

7.3 Chip-Board Co-Simulations

The drivers simulation results are strictly related to the load used for the simulations. Therefore, an appropriate load model is essential for sizing the drivers and for obtaining results close to experimental measurements. Obviously, using a complex model to better simulate the real effects means creating simulations that could take a long time. Therefore, for the sizing of the drivers, a first simplified load model is used, and then a more accurate model was generated and used for refining. The model used for the first sizing of the drivers is shown in Fig. 7.7. It is composed of the 600 fF equivalent capacitance of the output chip pad and its ESD protection, the equivalent model of the bonding wire, obtained from the 1 nH/mm rule of thumb and previous experiences, the equivalent capacitance of the board and the 50 Ω termination resistor. Implementing this simplified model in the simulator, the 5 Gbps eye diagram of the MZM driver output signals is obtained and showed in Fig. 7.8.

A more accurate model of the carrier board used for the device test was extracted using an electromagnetic simulator. The CAD of the board was imported into an electromagnetic simulator and simplified to reduce simulation time. Fig. 7.9 shows the

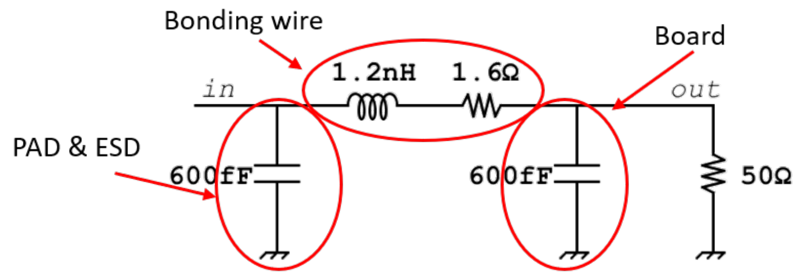

Figure 7.7: *Simplified drivers load model. It is composed by the pad equivalent capacitance, the wire bonding model, the board model and the termination.*

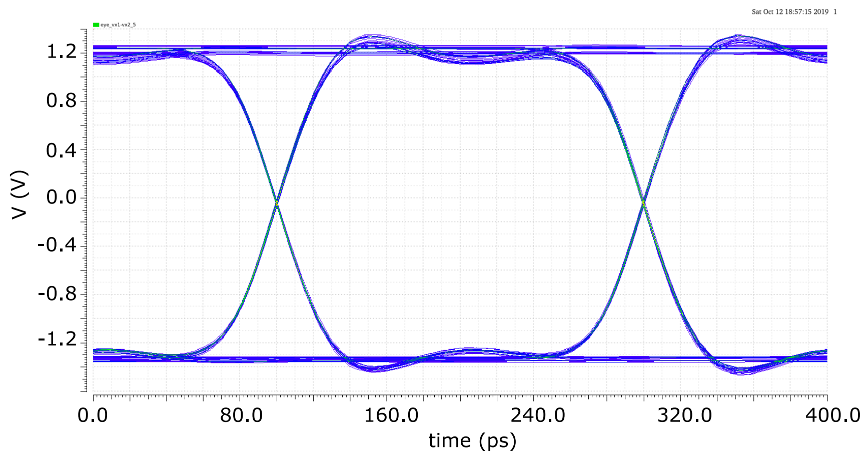

Figure 7.8: *Eye diagram of the MZM driver output signals at 5 Gbps using the simplified model in Fig. 7.7*

CAD of the board, where the input-output drivers paths are highlighted in red. The bonding wire connections between the drivers chip and the board are directly simulated together with the board. This allows providing the simulator the right wires bonding shapes, which affect the wires parasitic elements.

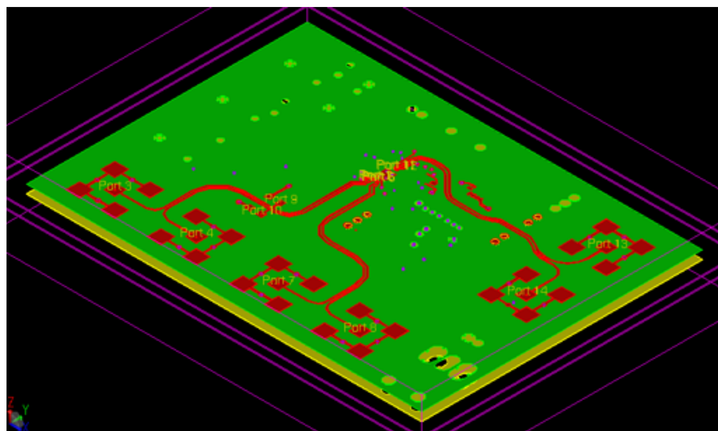

Figure 7.9: *Electromagnetic board level simulation using ADS-EMPRO Keysight tool. In the board center is placed the drivers chip and the wire bonding interconnections.*

The S-parameter matrix obtained from the electromagnetic simulation is then imported in Cadence's environment for the drivers characterization. The result of this co-simulation between the integrated electrical devices, inside the silicon chip, and the board model is shown in Fig. 7.10. The comparison between Figs. 7.8 and 7.10 highlights the heavy effects that the parasitic elements of the carried board have on the driver performances.

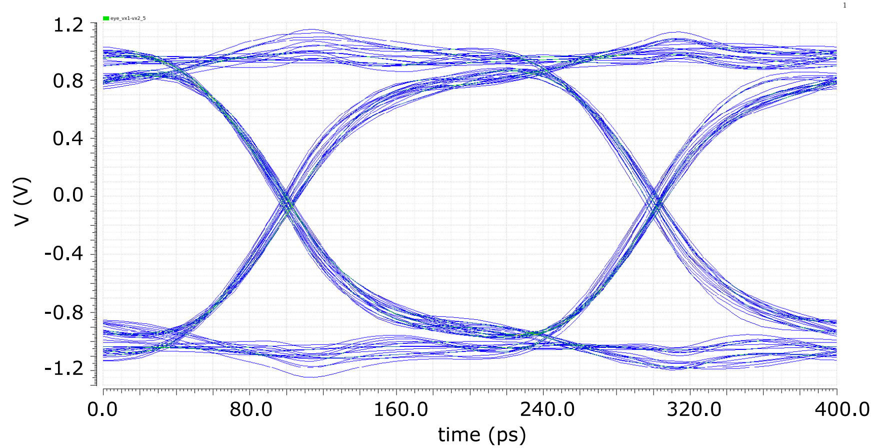

Figure 7.10: *Eye diagram of the MZM driver output signals at 5 Gbps using the bord model extracted with electromagnetic simulations.*

7.4 Drivers Measurements

The characterization of the two drivers is performed by connecting the chip directly to the testing board in Fig. 7.11 through 38 μm aluminum bonding wires. To limit the X-rays and heavy ions effects on onboard COTS (Commercial Off-The-Shelf) components, a metallic shield-mask is used during the radiation. Therefore, a distance of 2 cm is kept between the DUT (Device Under Test) chip and the other COTS components. The next sub-sections show the frequency domain and time domain measurements and the test results for the chip exposed to radiation.

7.4.1 Frequency Domain Measurements

The output signals of the driver are measured using a 40 GHz Anritsu VNA (Vector Network Analyzer), which provided also the 400 mVpp plus 1 V DC value signal to excite the two drivers. In Figs. 7.12 and 7.13 the S parameters S11 and S21 of the two drivers are displayed. Both S21 shows a broad-band bandwidth of up to 3 GHz. However, low power matching was found between 2 GHz and 3 GHz (S11 higher than -10 dB). The drivers were excited with -3 dBm input signals and considering a 5 dB of S21, the output signals have a power of 2 dBm, which on 50 Ω load means a single-ended amplitude of about 750 mVpp that meets the application constraint. Since the VNA measurements, alone, are not able to provide information about the power shared on the harmonics above the first, due to non-linear effects, then VNA measurements are followed by eye diagram measurements.

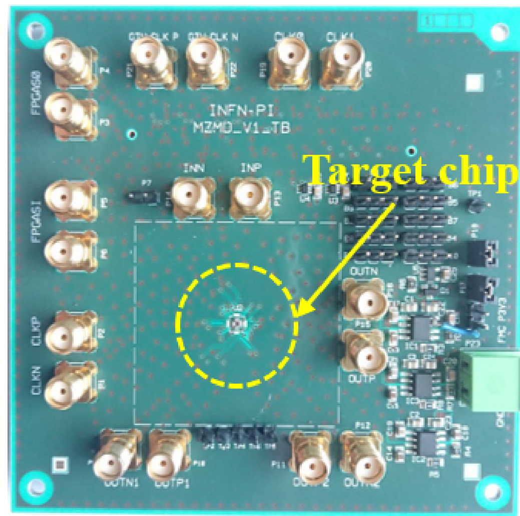

Figure 7.11: *Testing board with the chip directly bonded on the board, avoiding the package effects on high speed signals and radiation.*

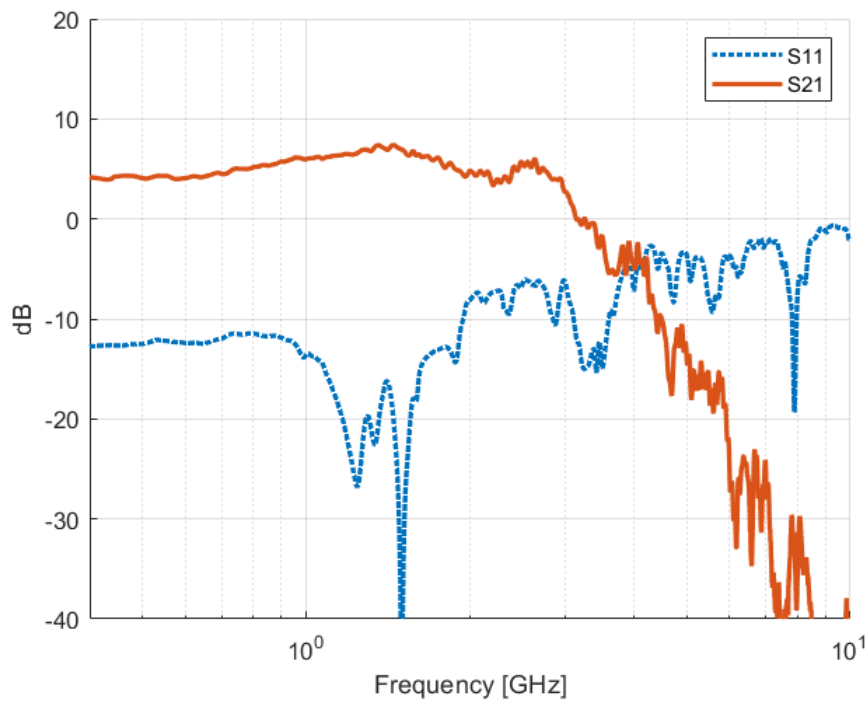

Figure 7.12: *S parameters, S11 and S21, of the MZM-driver, measured with -3 dBm input power and 1 V DC voltage.*

7.4.2 Time Domain measurements

The time-domain measurements were performed by exciting the DUT chip with PRBS23 (Pseudo Random Binary Sequence) signals generated by a Kintex Ultrascale FPGA MGT output and using a 23 GHz 100 GS/s Tektronix oscilloscope to get the eye-diagrams and the BER bathtub graphics. The oscilloscope loads the driver with a 50

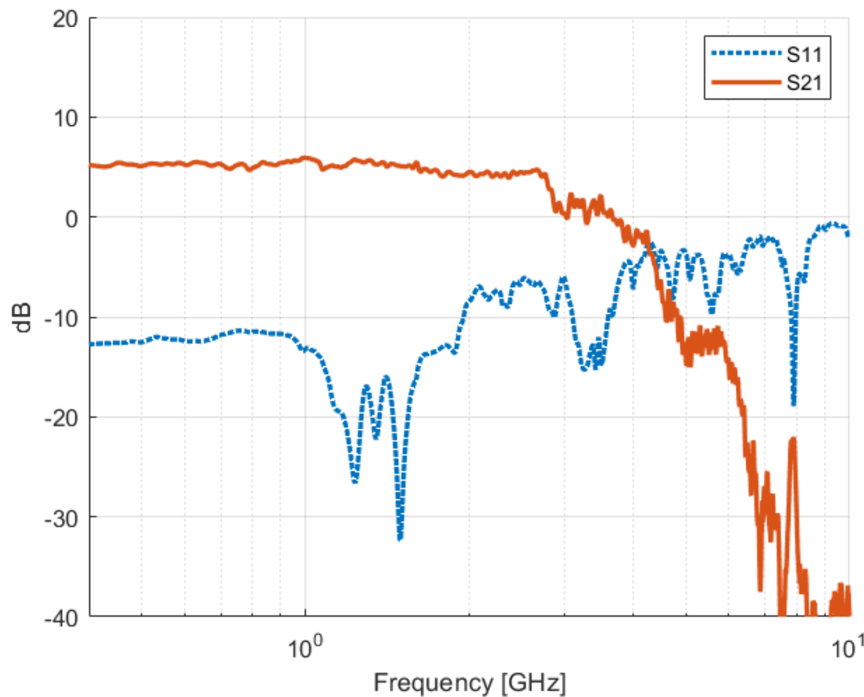

Figure 7.13: *S parameters, S11 and S21, of the RR-driver, measured with -3 dBm input power and 1 V DC voltage.*

Ω impedance halving the signal amplitude of the eye diagrams. Therefore, a factor of 2 should be considered to get the real signal amplitude from the eye-diagrams in Figs. 7.14 to 7.16. Fig. 7.14 shows the eye diagram of the RR-driver output at 1 Gbps with an eye amplitude of 1.24 V and so a real amplitude of 2.48 V. The eye diagram of the MZM-driver at low data rate is not reported in this thesis because it is comparable to that of Fig. 7.14. In Fig. 7.15 the eye diagram of the MZM-driver outputs at 5 Gbps is shown with its bathtub graphic. As we can see, the eye-amplitude (defined as the difference between the mean one level and the mean zero level) is 1.37 V, which means a real amplitude of 2.75 V.

Fig. 7.16 shows the eye diagram of the RR-driver outputs at 5 Gbps. In this case, the eye amplitude is only 1.04 V, which means a real amplitude of 2.08 V. However, the higher jitter effect, which shifts the zero-crossing points, makes a lower eye-height (defined as the vertical inner space distance of the eye diagram) of 510 mV and so 1.02 V without the oscilloscope loading effects. Therefore, a higher BER (Bit Error Rate) is expected for this driver. After the first electrical characterization with measuring instruments (VNA and Oscilloscope) the whole system test was performed connecting the drivers with the relative MZM and RR developed by CERN, through bonding wires, see Fig. 7.17. The lightwave was generated using a laser in C-band and read with a photodetector (New Focus Model 1434). The electrical signals, encoded with 8b/10b code, were generated with a Kintex Ultrascale FPGA and the photodetector output was read with a high-speed oscilloscope. In particular, Figs. 7.18 and 7.19 show example results of the optical power eye diagrams at 1 Gbps and 5 Gbps, respectively, using the MZM modulator. The two different lines of the eye diagram in Fig. 7.18 are due to the

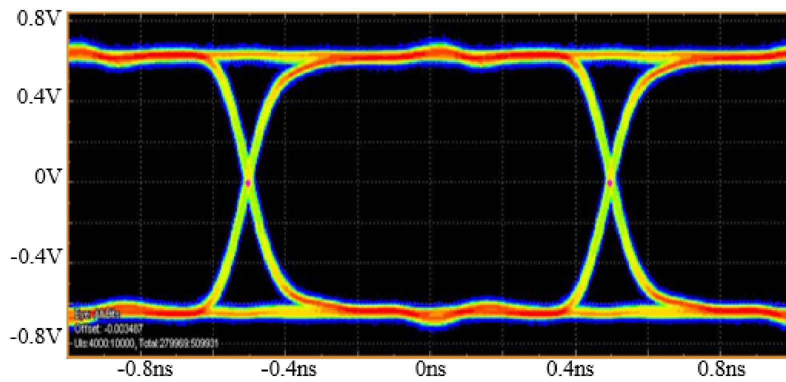

Figure 7.14: *Eye diagram of MZM-driver differential output at 1 Gbps. The signals are affected by 50 Ω instrument loading effect.*

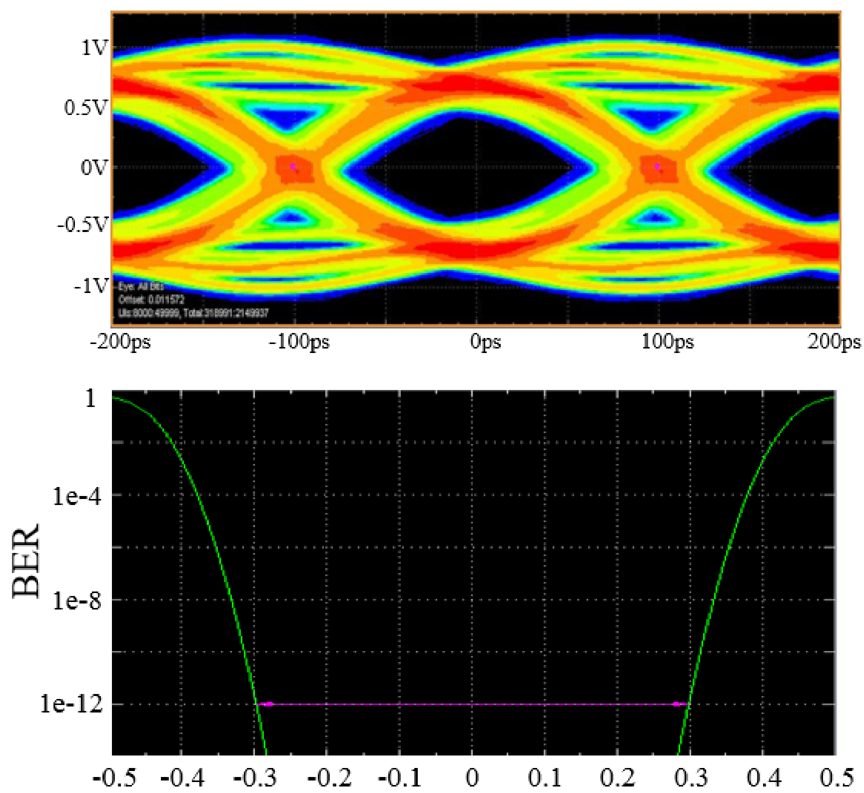

Figure 7.15: *Eye diagram of MZM-driver differential output at 5 Gbps (top) and bathtub graphic for the BER estimation with unit interval normalized axis (bottom).*

Inter-Symbolic Interference (ISI), which in this case is the dominant contributor to the deterministic jitter.

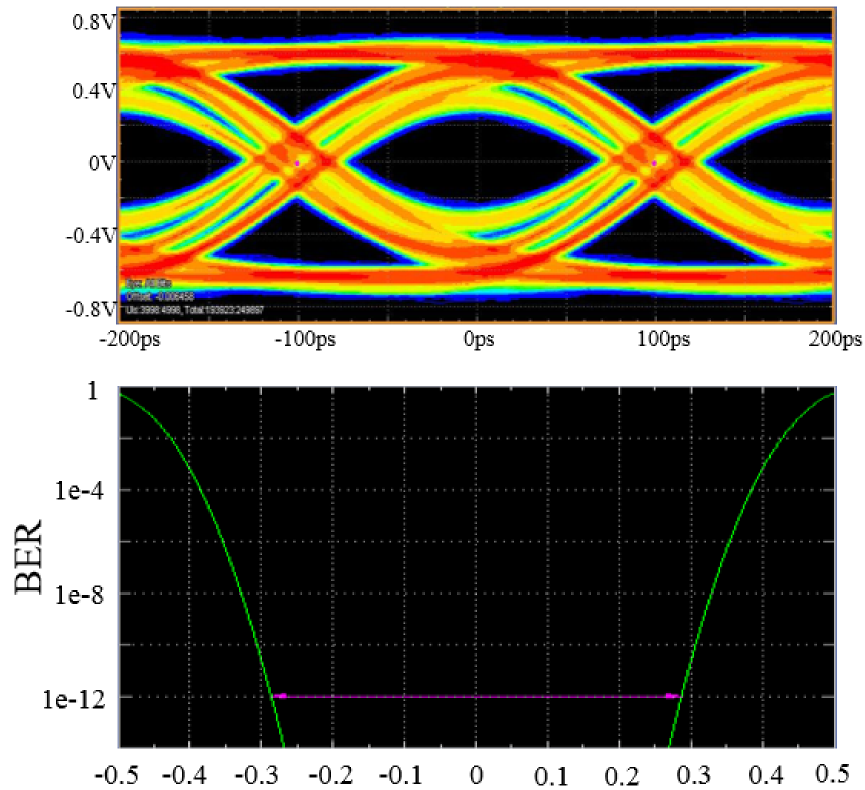

Figure 7.16: *Eye diagram of RR-driver differential output at 5 Gbps (top) and bathtub graphic for the BER estimation with unit interval normalized axis (bottom).*

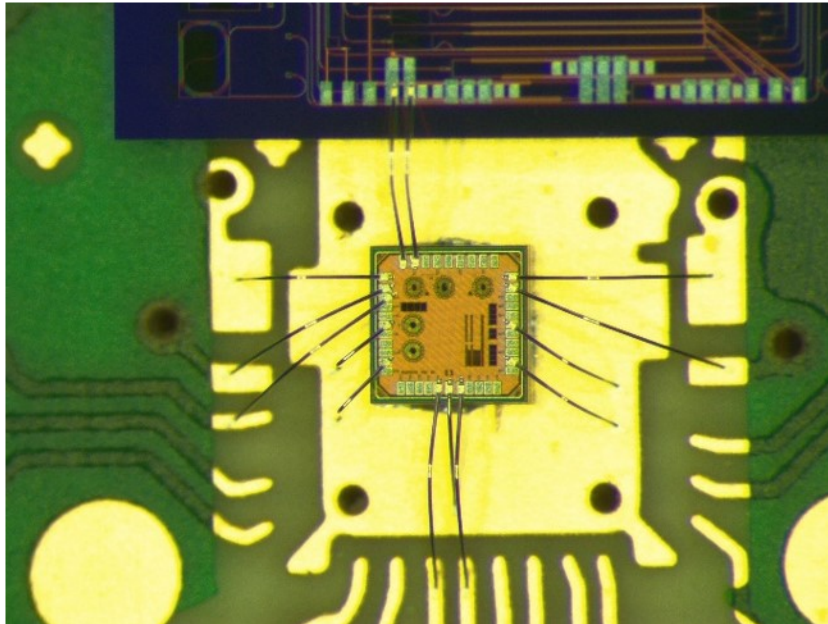

Figure 7.17: *Silicon drivers chip directly bonded with the Silicon Photonics chip. In particular, the image shows the bonding of the RR with its driver.*

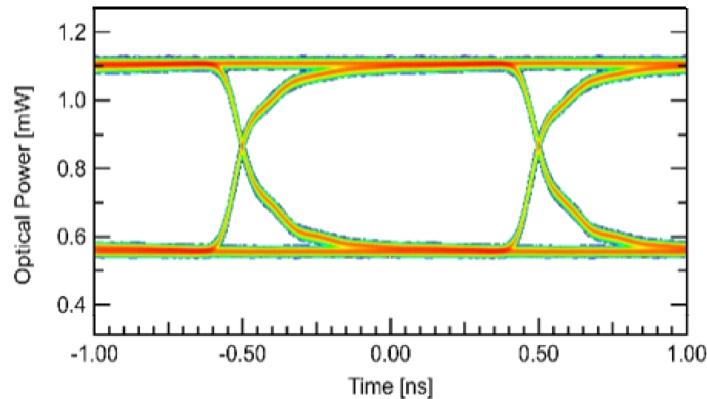

Figure 7.18: *Eye diagram of the MZM output optical power for 1 Gbps.*

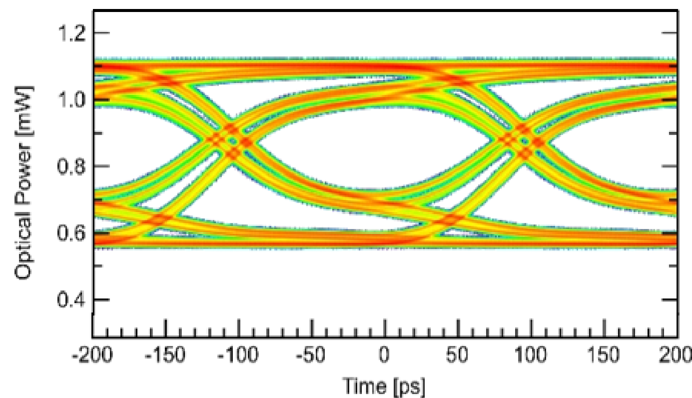

Figure 7.19: *Eye diagram of the MZM output optical power for 5 Gbps.*

7.4.3 TID and SEE Measurements

TID experimental verification

The TID measurements were performed using the X-ray Seifert RP 149 machine with a density of 4.3 Mrad/h at the X-ray facility of INFN Padova, see Fig. 7.20. The dose rate used for the test was chosen only to achieve the desired TID levels in a relatively short time. The estimated real dose rate inside the HL-LHC is some orders lower than that used for test purposes, allowing to reach 800 Mrad in ten years. Therefore, the TID test performed in this work is a worsening of the real condition, since the charge buildup in the oxide does not have time to recombine through annealing effects. During irradiation, the chip was powered on and received a 400 mVpp 1 Gbps differential signal to recreate the operating environment. Fig. 7.21 shows the amplitude variation of the two drivers outputs for increasing TID levels. For high radiation levels, the signal amplitude decreases due to worse MOSFET performances, as expected from Chapter 6. The amplitude decrement at 800 Mrad (SiO_2) is 30% for MZM-driver and 25% for RR-driver, which is in line with the extrapolation results reported in Fig. 6.3, showing a 27% loss in current value at 800 Mrad (SiO_2) level for N-MOSFETs with a length of 120 nm. These results verify also the model developed for MOSFETs operating in a high radiation level environment.

Table 7.4 sums up the variation of the main signal parameters of the two drivers

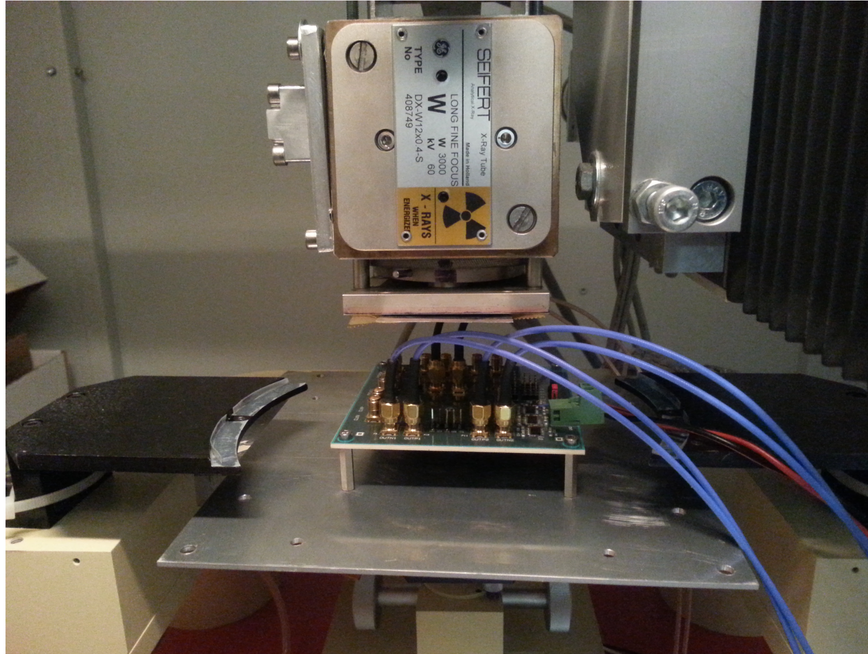

Figure 7.20: *Photo of the carrier board placed in the Seifert RP 140 machine for the TID test at INFN Padova.*

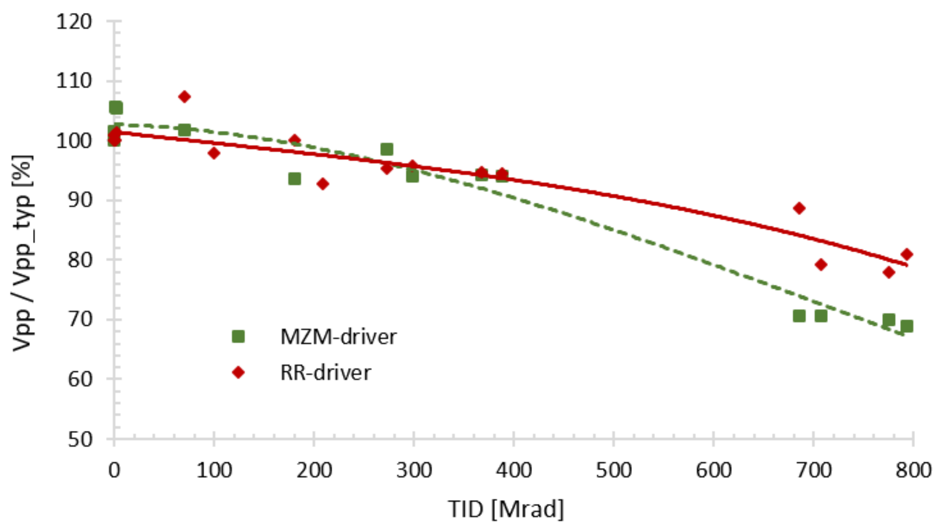

Figure 7.21: *Measured amplitude reduction as a function of the total dose.*

measured at 800 Mrad (SiO_2). Different fall and rise time (defined as the interval time taken from 10% to 90% of the signal amplitude) effects are observed. A higher fall time increment could be explained with a stronger TID effect on active components than passive ones. A significant different rise time between the two drivers is obtained as a result of the measurements. This can be explained considering the different driver topologies: the RR driver has an internal “pull-up” for the output stage, instead, the MZM driver is an open-drain driver, which for the electrical test purposes uses external

50 Ω pull-up resistors. These external resistors are placed on the bottom side of the testing board used for the TID test, shielding them from radiation damage. Being the "pull-up" of the MZM driver not affected by radiation, the rise times of this driver in typical condition and when exposed to 800 Mrad are nearly the same. In the test of the whole system, electrical and optical components will be exposed to radiation, hence a more balanced losing between rising and fall time is expected as in the RR driver test. Considering the results obtained by time-domain measurements and the -30% loss due to TID effects, the real eye amplitude at 800 Mrad (SiO_2) for the MZM-driver is 1.93 V, which is slightly less than the 2 V target. In the RR-driver case, considering a -25% loss at 800 Mrad (SiO_2), a real eye amplitude of 1.56 V is obtained, meeting the constraint for the RR-driver.

Table 7.4: *Relative variation from 0 Mrad to 800 Mrad (SiO_2) at 1 Gbps for the main signals parameters*

	Single Ended Vpp	Fall Time	Rise Time
MZM Driver	-30%	+20%	-0.2%
RR Driver	-25%	+65%	+40%

SEE experimental verification

Tests with heavy ions were made with the Tandem accelerator of the National Laboratories of INFN Legnaro (IT), see Fig. 7.22. Seven heavy ions, with different LET, were used to test the two drivers on the chip. The drivers were excited with 1 Gbps signal encoded with NRZ 8b/10b, generated by a Kintex Ultrascale FPGA, and their outputs were sent to the FPGA for the comparison between the sent and the received bits patters. This in order to find bits errors generated by the interaction between heavy ions and silicon devices. The measurements were performed using a data rate of 1 Gbps for the speed reduction due to BNC connectors and long cables used in the measurement setup. Fig. 7.23 shows the Weibull's curve of the cross-section as a function of the ions LET. The cross-section is calculated as the ratio between the number of errors found during the experiment and the total fluence (Mions/cm^2) used for the test of the selected ion. As shown in Fig. 7.23, a cross-section lower than 1e-8 was found for the O^{16} ion, with a LET value of 3.16 MeV·cm^2/mg, since no error was registered for a fluence over 100 Mions/cm^2.

Table 7.5 lists an estimation of the BER generated in the forecasted CMS experiment of the HL-LHC using the MZM driver. The BER is calculated using eq. 7.5, where σ is the cross-section shown in Fig. 7.23, the flux is the particles flux reported in [132] and the bit rate is equal to the target bit rate of this work (5 Gbps).

$$BER = \frac{\sigma \cdot flux}{bitrate} \tag{7.5}$$

In Table 7.5 are listed the BER for two different LET points, 3.16 MeV·cm^2/mg and 42 MeV·cm^2/mg corresponding to a cross-section of 1e-9 cm^2 and 3.3e-6 cm^2, respectively, and for three distance points from the beamline, 5 cm, 10 cm and 15 cm.

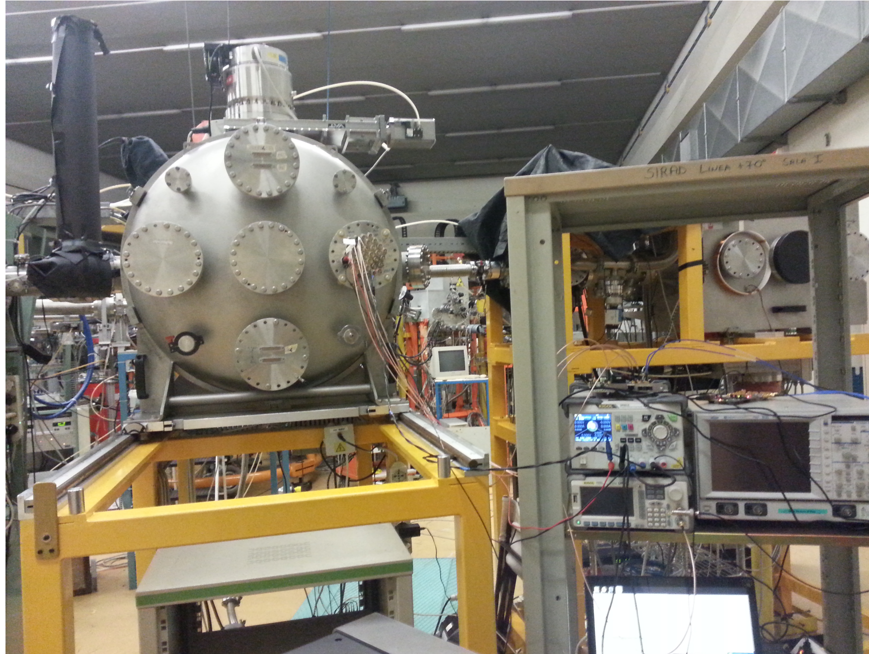

Figure 7.22: *Photo of the vacuum chamber used for the heavy ions test and instrumentation setup.*

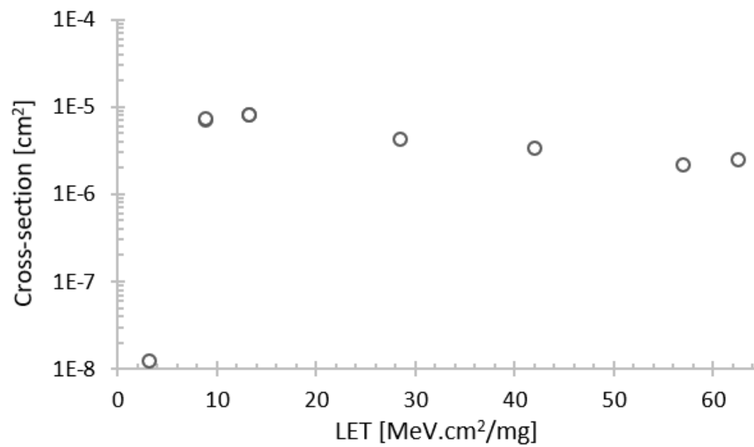

Figure 7.23: *Cross-section as a function of the ions LET for the MZM driver.*

Table 7.5: *BER data for different distances from the beam line*

		LET = 3.16 MeV·cm^2/mg	LET = 42 MeV·cm^2/mg
Distance (cm)	Flux ($\cdot 10^6 cm^{-2} s$)	BER	BER
5	32.5	<6.50e-11	2.73e-8
10	16.3	<3.25e-11	1.37e-8
15	3.2	<6.50e-12	2.73e-9

7.5 State-of-the-art Comparison

Thanks to the radiation-tolerant techniques proposed in Chapter 6, the designed drivers are able to operate up to 5 Gbps when exposed to 800 Mrad TID. Considering the heavy radiation effects on the 65 nm CMOS technology, a CML approach is adopted, avoiding the use of P-MOSFET transistors, whose performance are extremely affected by charge trapped in silicon oxides. In addition, to mitigate the radiation effects on LDD spacers, double MOSFET length is used for the drivers design. Table 7.6 compares the drivers exploited in this thesis with state-of-the-art drivers for HEP experiments. The work in [119] has the same data-rate of this work but a TID radiation hardness limited to 100 Mrad. The work in [133] has a double data rate but only 100 Mrad hardness and output power limited to 2.04 dBm, which is not suitable for MZM driving. Considering the measurement results of the two proposed drivers, the RHBD techniques used to face radiation problems seem to bring the driver to work at a level of radiation where, today, no other chip is able to work.

Table 7.6: *State-of-the-art comparison table*

	[119]	[134]	This work
Technology	130 nm	130 nm	65 nm
Bit Rate	5 Gbps	10 Gbps	5 Gbps
Output Power	3.98 dBm	2.04 dBm	12.77 dBm MZM 10.34 dBm RR
TID tolerant	100 Mrad	100 Mrad	800 Mrad

CHAPTER 8

Conclusions

The ICs operating in harsh environments have to adopt techniques to mitigate the effects generated by rugged conditions. The development of these techniques, to enabling the electronic devices to properly work under stressing conditions, still be one of the most challenges in the ICs electronic design. As shown in Chapter 1, silicon devices could be extremely affected by high-energy disturbance, such as strong chemical attacks, mechanical stresses, heavy electromagnetic disturbs, wide temperature changes and high-energy radiation. Harsh environments can collect more than one of the previous rugged conditions making even more challenging the ICs design.
The automotive, aerospace and HEP worlds, being characterized by high-voltages domains, high-temperature and strong electromagnetic disturbs, make demanding the development of specific techniques for enabling the ICs to operate in critical systems. In this framework, some high-voltage and fault-tolerant ICs techniques are developed in this thesis and discussed in Chapter 3. In particular, techniques, as multi-domains management, equivalent resistor based design, HV diode switches and back-to-back HV diode switches, SKIP, and SC inductorless insulator, are used to design an integrated inductorless DC/DC converter, whose system and transistor levels design is presented in Chapter 3. It is composed by a multi-stage cascade architecture, consisting of three SC converters with step-up/down capabilities plus linear converters working in parallel at the end of the cascade. Multiple regulated output voltages and input-output isolation are provided without the use of cumbersome inductors or transformers. In addition, the design includes an on-chip control unit and a serial interface towards the external host. The comparison between the proposed DC/DC converter and commercial/research solutions, reported in Table 4.3, highlights the benefits of the techniques developed in this thesis. At the best of the author's knowledge, this is the first inductorless DC/DC converter able to ensures regulation performance in a wide range from 6 V to 60 V.

The features of the fabricated IC were evaluated through experimental measurements in a classical 2D configuration, with external components placed side-by-side with the chip, and using an innovative 3D solution, with external passive components stacked on top of the DC/DC converter die, for area reduction. The comparison between the measurement results of the 2D and 3D structures, performed in Chapter 4, highlights that the 3D technology is a feasible way for converter applications where low-power loads have to be supplied by high-voltage inputs, up to 60 V. The use of an all integrated DC/DC converter in a 3D technology can reduce the occupied area versus state-of-the-art solutions, keeping good performance. This area reduction was evaluated in at least a factor 5 versus similar 2D designs [62], paving the ways for future investigations on the 3D technologies.
The overvoltage and SEE tests highlight the fault-tolerant features of the innovative converter INSUL stage, adopted in the proposed DC/DC converter and realized avoiding the use of off-chip transformers. The TID test of the whole DC/DC converter proves the 43 krad radiation-hardness of the device, making it suitable for space applications as Earth-Moon travels [63].
Since the ever-more relevant EMI issue in converter electronics, Chapter 5 is wholly dedicated to techniques to reduce conducted and radiated EMI. The proposed DC/DC converter, implementing techniques, as input filter, low switching frequency, SKIP, and soft-start, reduces the conducted and radiated EMI emission below -51.61 dBm and -70 dBm respectively, values widely lower than CISPR 22 law limits. In addition, the combination of the TID and emission performances, showed in Chapter 4 and in Chapter 5 respectively, enabling the DC/DC converter to operate in space missions requiring stringent electromagnetic cleanliness, without the use of metallic shields, as GOCE, EXOMARS, Rosetta, BepiColombo and Solar Orbiter missions [83–86]. The use of the commercial-grade 0.35 µm HV-MOSFET technology makes the designed DC/DC converter a low-cost solution for low power conversion. However, in the case, the proposed DC/DC converter architecture would be used for higher power conversion an efficiency improvement could be required. This efficiency increment can be realized in two main ways: the first based on the converter architecture revision and the second on the technology used. Better efficiency levels can be achieved increasing the number of VCRs in order to reduce the voltage across the pass element of the output linear converters. Ideally, if all the SC stages had no losses and an infinite number of VCRs would be used, the only losses will be due by the minimum voltage across the pass element of the linear converter, with a sensitive efficiency increment. In case of losses on the SC stages, a trade-off between the number of SC stages and the losses due to liner converter should be done. A way to reduce the losses of the SC stages is the use of higher performance technology with lower ON-resistance devices. The Silicon-Carbide (SiC) technology is an emergent solution that exhibits ten-times higher critical electric field strength, two-times higher saturated electron drift velocity, and three-times higher thermal conductivity than Si, making it an attractive option for power devices [135]. The use of SiC devices, having lower ON-resistance and higher critical field strength than the LDMOS devices used in the proposed DC/DC converter, will reduce the R_{FSL} of the Eq. 3.6 and Eq. 3.7, improving the SC stages efficiency, as shown in Eq. 3.8. Also, the R_{SSL} could be improved choosing the SiC solution. Indeed, the SiC devices, having lower ON-resistance, allow using smaller devices, which can be driven with a

higher frequency. Then, being the R_{SSL} strictly related to the switching frequency, as shown in Eq. 3.6, a reduction of R_{SSL} could be achieved.
On the radiation side, the effects on integrated silicon devices, due to radiation exposure in aerospace and HEP applications, are detailed described in Chapter 6, together with the RHBD techniques used in this thesis to address extreme TID levels and SEE effects, like long MOSFETs, ELT transistors and CML as a replacement for CMOS architecture. These RHBD techniques, in addition to buffer chain and inductive peaking solutions, are then used in Chapter 7 for the design of two high-speed rad-hard drivers for electro-optical modulators. The drivers are fabricated in the 65 nm commercial-grade TSMC technology and experimentally tested with electrical and electro-optical setups, exhibiting 800 Mrad 5 Gbps capabilities. The 5 Gbps results show a differential signal amplitude of about 2.75 Vpp for the MZM-driver and 2.08 Vpp for the RR-driver, which allow the MZM and RR to operate adequately. The TID measurements, performed using X-ray, highlight an amplitude reduction of 30% for MZM-driver and 25% for RR-driver at 800 Mrad, which are in line with the data extrapolated from state-of-the-art measurements. The heavy-ion tests have highlighted an immunity LET threshold between 3.16 Mev $\cdot$ cm^2/mg and 8.79 MeV $\cdot$ cm^2/mg and a plateau lower than 1e-5 cm^2. Thanks to these values an estimation of the BER levels, for the next LHC upgrade, is performed, highlighting a maximum BER of 2.73e-8, when the device is placed in the inner layer of the detector, at only 5 cm from the beamline. At the best of the author's knowledge, thanks to the radiation hard techniques adopted and described in Chapter 6, this chip is the first high-speed electronic device, in literature and market, able to operate at such high radiation levels.
An even more increment of the radiation tolerant property can be achieved using an advanced technology node, indeed in Chapter 6 is highlighted the relation between MOSFETs radiation hardness and their gate oxide thickness. The lower is the gate oxide thickness and the lower is the charge accumulated in it. Indeed, recent measurements on single devices implemented in the 28 nm TSMC technology exposed to high levels of radiation have proved a radiation hardness improvement of about 45% for N-MOSFETs and 50% for P-MOSFETs [136, 137], allowing achieving 1 Grad level with a lower design effort or higher radiation levels with the same techniques proposed in Chapter 6. On the high-speed side, the 28 nm technology could be able to increase the drivers bit rate for its higher cutoff frequency. However, the main limitation on the drivers bandwidth is due to the interface with the external world. Indeed, pads, ESD protections, bonding wires and electro-optical loads are mechanically constrained independently of the technology scaling. Some preliminary simulations have already shown that halving the ESD protections capacitances, reducing the bonding wire inductances, and improving the load modeling, a bit rate of 10 Gbps can be achieved with the same technology used in this thesis. Therefore, to achieve better speed performances a major effort should be paid on the packaging side. Currently, the best packaging solutions to achieve the best high-speed performance is the 3D stacking of the electronic chip on the photonic die (the first is typically smaller than the second), using ball bonds or TSV for the electrical connections. This solution, on a side, allows eliminating the bonding wires, reducing also the pads size, but, on the other side, requires a layout co-design of the electronic and photonic chips that is not always possible.

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