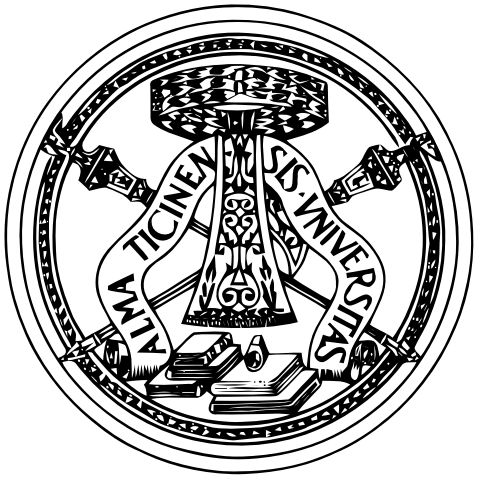

Università di Pavia

Frequency Doublers and Phase Shifters for D-band Phased Arrays in SiGe BiCMOS Technology

Department of Electrical, Computer and Biomedical Engineering

Ph.D. Degree in Microelectronics

Supervisor:
Ch.mo Prof. Andrea Mazzanti

Ph.D. Candidate:
Lorenzo Piotto

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Abstract

The continuous growth in the demand for seamless and high-data-rate mobile connectivity is setting severe requirements to the network infrastructure for 5G and beyond. The development of technologies capable of working above 100 GHz opens with confidence to mm-Wave and sub-THz bands, promising to achieve data rates above 100 Gbps with wireless links, giving the advantage of reduced deployment costs and higher flexibility compared to fiber solutions. On the other hand, with the increasing path loss and limited output power achievable by single amplifiers, phased-array systems become the only solution to increase EIRP, providing both high antenna gain and power combining. At the same time, the system gains the flexibility of beam steering, relaxing the challenges of TX-RX antenna alignment, and opening to a reconfigurable network interconnection.
The need for high performance transceivers has to cope with the challenge of operating at frequencies in the range of one half or one third of the f_{max} of currently available silicon technologies, negatively affecting the key performance metrics, as output power, low noise, wide bandwidth and efficiency.

The three years research activity focused on the development of key building blocks in SiGe BiCMOS technology, targeting D-band phased array transceivers for backhaul communications.
The first part concentrates on the need for wideband and high efficient frequency multipliers, proposing a novel mixer based frequency doubler architecture. The conversion gain is improved by applying a DC offset to the switching-quad transistors, such that the duty-cycle is reduced and the output current assumes an almost square-wave shape at twice the input frequency. The DC offset is self-adjusted by a low-frequency feedback loop to maintain optimal performance against input power and PVT variations.
A proof of concept design in K-band demonstrates a remarkable 85% fractional bandwidth along with a P_{sat} = 5.7 dBm, 17% collector efficiency and better than 40 dB rejection of the fundamental component. The concept is validated also in D-band, with experimental results showing a peak output power of 6.5 dBm at 148 GHz with 7.4 % power conversion efficiency and 8 dB of conversion gain. The -3dB bandwidth is from 125 GHz to 170 GHz and output power remains greater than 0 dBm over the full D-band, from 110 GHz to

170 GHz.
The second part of the thesis focuses on phase shifters. First, the vector interpolation principle is investigated, with particular care on the AM-AM and AM-PM distortion mechanisms introduced by the need for high dynamic range variable gain amplifiers (VGAs). A testchip proves [130 - 175] GHz bandwidth along with the highest reported $OP_{1dB} = 1.8$ dBm and collector efficiency, $\eta = 2.4\%$, against vector interpolation phase shifters operating in the same frequency range, and low RMS amplitude and phase errors of 0.8 dB and 5°, respectively.
To further increase the limited efficiency of the vector interpolation scheme, and both the bandwidth and high-insertion-loss limitations of fully-passive solutions, a novel phase shifter architecture is proposed. The input signal is split into I/Q vectors which are shifted with passive fine step phase shifters, passed through 0°/180° passive phase inversion blocks, and finally combined by a pair of amplifiers operated at constant gain for optimal linearity. The relative phase shift between the I and Q vectors is exploited for gain and phase errors corrections, avoiding the need of VGAs. Measurement results on a SiGe BiCMOS test-chip working in D-band compare favorably against previous works, demonstrating [130 - 170] GHz bandwidth, a superior OP_{1dB} above 2 dBm and with the highest power efficiency of 5%.

This work has been carried out at the Analog Integrated Circuits (AIC) Laboratory of University of Pavia, and received funding from the Commission of the European Union within the H2020 DRAGON project (Grant Agreement No. 955699) and KDT SHIFT project (Grant Agreement No. 1010962). The definition of system requirements was carried out in collaboration with the group of Huawei Milan, Italy.

Contents

1 Introduction

This dissertation summarizes the three years activity carried out while pursuing the Ph.D. at the Analog Integrated Circuit Laboratory, supervised and mentored by Prof. Andrea Mazzanti and with a fruitful cooperation with various colleagues and friends.
Most of the research work focused on developing key building blocks targeting D-Band phased array transceivers for backhaul communication, operating in the frequency range [130 - 175] GHz. In particular, the first part of the activity concentrated on frequency doublers, while the latter on phase shifters.
The dissertation is organized as follows:
Chapter one gives a brief introduction on the backhaul network, investigating why in D-band we will probably need phased arrays and what benefits/challenges they bring along.
Chapter two focuses on frequency doublers, introducing an architecture which is inherently broadband. A proof of concept is tested at low frequency to demonstrate the performance, while a second test chip extends the results in D-band.
Chapter three concentrates on phase shifters, with two implementation in D-band. The first is based on the vector interpolation principle, with a study of the distortion mechanisms that impair linearity. The second overcomes the linearity bottleneck in the vector interpolation approach, i.e. the VGAs, by leveraging a combination of passive phase shifting networks and active circuits, organized in order to minimize losses and avoid the need of gain control within the amplifying stages.
Chapter four eventually draws the overall conclusion.

1.1 The backhaul network

Ever since, the challenges of new generation communication standards are pushing for higher data-rates, supporting massive number of connected devices, lowering latency and improving quality of service.
Among other important changes, one structural key aspect to accomplish this is to increase the number of radio nodes (base stations) distributed across the

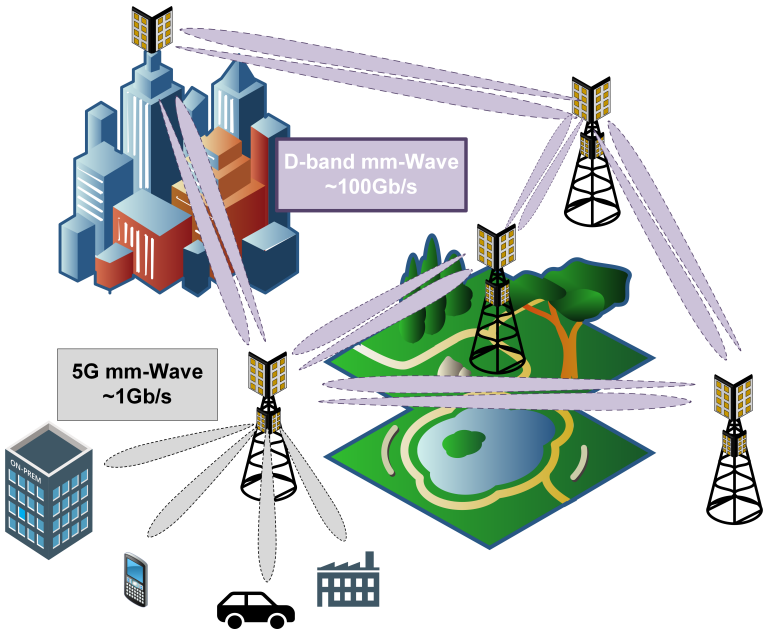


Figure 1.1: Network infrastructure: in gray the base station serving users and, in purple, the backhaul interconnection links

network, requiring a complex interconnecting mesh, aka *backhaul network*, as visible in Fig. 1.1. High research effort is involved on this topic in order to move backhaul communications from optical fiber (highly performing but expansive to lay) to wireless. [1] estimates more than a factor of 20 in cost between a point to point connection based on fiber optics with respect to a wireless link, not mentioning the deployment time and permission constraints.
The concept is not new and already in place for many years with commercial links up to the range of [10 - 25] Gbps at E-band frequencies ([71 - 86] GHz), exploiting channel bandwidths up to 2 GHz or, at lower bandwidth, higher spectrally efficient modulation schemes up to 1024-QAM. Being this a well established solution, research is pushing toward the next generation of backhaul links that is planned to be in D-band ([130 - 175] GHz), supporting frequency division duplexed (FDD) links with up to 5 GHz bandwidth, or time division duplexing (TDD) up to 10 GHz and throughput >100 Gbps.
This change brings few challenges. First of all, the so called free space path loss increases due to the scaling of the antenna size with frequency. Along with the wider channel bandwidth and a degraded receiver noise figure, this forces the need for higher EIRP for a given link distance. This may be mitigated by increasing the antenna directivity (i.e. scaling less the antenna size), at the expense of a narrower beam aperture which, considering an antenna gain of [30 - 40] dB, is already in the order of few degrees, increasing the challenges of antenna alignment. The increased EIRP requirement sets a second issue, given by the limited output power achievable by a single power amplifier (PA) at these frequencies, even exploiting the more performing III-V technology nodes,

as done in the current E-band links.
These two limitations can be overcome by introducing the concept of phased arrays, already well explored in radars and satellite communications, where the single-front-end-single-antenna architecture is split into multiple front-ends (FE) and multiple radiating elements. The overall antenna directivity scales with the number of elements ($G_{ANT} = 10\log N + G_E$, N being the number of elements and G_E the antenna gain of the single element) and the same advantages of increased EIRP at the TX side and increased SNR at the RX side are maintained with respect to a single high directivity antenna. At the same time, given we now have multiple (M) transmitters, the EIRP increases by another factor ($10\log M$) due to the over-the-air power combining, meaning we are not anymore limited by the output power of a single device. Moreover, by controlling the relative delays between the various radiating elements, the radiation pattern can be electronically steered, easing the issue of TX-RX antenna alignment and compensating for mechanical vibration of the antenna mounting point [2].
This architecture, along with the larger production scale, enables the use of silicon based technologies, with most focus, for now, on the SiGe BiCMOS that offers high speed/medium power heterojunction bipolar transistors (HBTs) with low power CMOS nodes, fundamental for the backbone of the transceiver (digital, biasing, monitoring etc.). If the volumes allows for it, fully CMOS solutions will probably follow. However, also hybrid architectures based on chiplets may have a future, leveraging the high performance of compound semiconductor technologies (e.g. InP) in the critical blocks, as the PA or the low noise amplifier (LNA), along with a scaled CMOS core which may become dense of functionalities.

1.2 Phased Array Systems

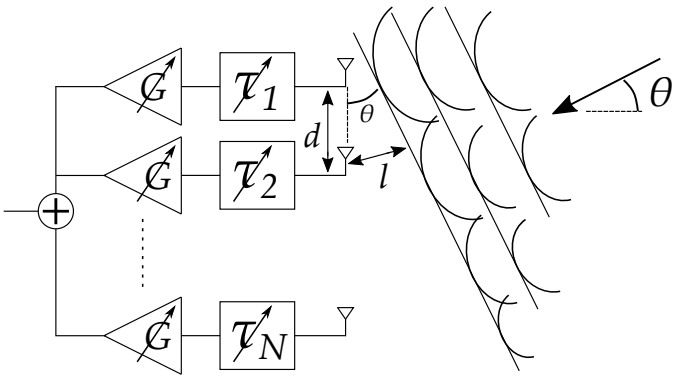


Figure 1.2: Phased Array structure

Figure 1.2 depicts a one dimensional structure of a phased array, where multiple antenna elements, usually spaced by a distance of $d = \lambda/2$, are fed by

multiple transceivers, also called beamformers, which may control the relative delay τ and, as second order requirement, the relative gain G of the signal feeding each element. Figure 1.2 represents an RX scenario where the incoming wave arrives with an angle θ with respect to the normal plane of the array. From purely geometrical considerations, between one element and the successive, the wave has to travel a further distance $l = d \cdot \sin\theta$, introducing a delay $\tau'=c/l$, with c being the speed of light as we assume we are in air. It is therefore clear that, to achieve constructive summation at the "+" node, the relative delay between adjacent channels needs to be $\tau_m - \tau_{m-1}=\tau'$. To point the antenna along one direction, i.e. perform the beam steering, it is therefore sufficient to change the value of the relative delay. The more the antenna elements, the higher the selectivity of the constructive/destructive interference, which leads to narrower beam aperture and higher the antenna directivity. The concept is extended in the two dimensions applying the same approach on both azimuth and elevation.
As said, a second desired feature is relative gain control among the channel. This is used to improve the radiation pattern of the antenna by reducing the undesired side lobes [3] that arise, especially when the beam steering angle is increased.

We have seen that, by its nature, a phased array requires a progressive delay among the different channels, which is proportional to the number of elements and the desired beam steering range, also called scan angle of the array. This may be in the order of many periods of the RF frequency and it is normally unpractical to achieve in the analog domain, requiring digital or hybrid beamforming architectures. On the other hand, these solutions are more complex, power hungry and difficult to be realized at mm-Wave bands, as the required delay resolution scales with frequency.
We all know that, at a single frequency, the delay can be substituted by a phase shift. This has the major benefit of being periodic, thus it does not scale with the array size, and easily implementable in RFICs. However, this simplification can be employed only when the fractional bandwidth of operation is narrow, as typically the case in communication systems (e.g. in D-band the instantaneous channel BW is 5 GHz over a 150 GHz carrier), since, in general, it introduces undesired impairments as beam squinting, a modulation/broadening of the pointing angle of the antenna θ [4], and signal distortion, similar to the inter-symbol interference introduced when not fulfilling the Heaviside condition [5].

Figure 1.3 shows a simplified block diagram of a wireless communication system. This is not a general picture, as many variants on the architecture are possible. Blocks are divided into the TX and RX chains, which, in the case of an FDD system, may be connected to separate antennas. The RX chain starts

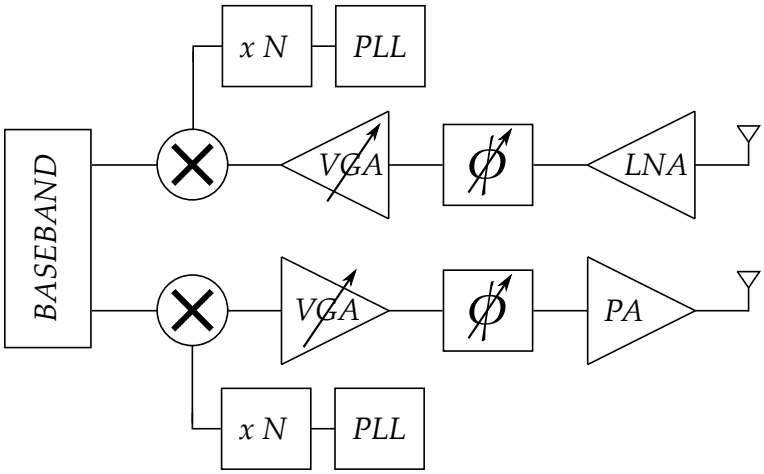


Figure 1.3: Wireless communication system block diagram

with the low noise amplifier (LNA) required to minimize the noise figure of the receiver, maximizing the sensitivity. Then, phase shifter and the variable gain amplifier (VGA) are used to support beamforming. Later, the RF signal is downconverted at lower, or, as in this case, baseband frequencies, where it is processed by the baseband unit, also in charge of controlling all the blocks.
The same concept, but in reverse, is used in the TX side, which ends with the power amplifier (PA), in charge of maximizing the power to the antenna, and, in general, it is the block dominating the overall power efficiency of the TX chain.
On top and bottom are the frequency synthesizer, formed by a phase locked loop (PLL), normally working in sub mm-Wave frequencies, and a frequency multiplier to generate the high frequency LO.

2 Frequency Doublers

Frequency synthesis is a key function in RF and mm-Wave wireless communication and sensing. In this framework, the development of wideband components and systems is presently driving intense research activity for applications such as dual band 5G transceivers [6], [7] and high resolution imaging in industrial [8], [9], medical [10], [11] and scientific fields. Typically, RF frequency synthesis is based on a Phase-Locked Loop (PLL) with a Voltage-Controlled Oscillator (VCO) operating at the target output frequency. However, the design of PLL components is made challenging when the operating frequency is increased towards the mm-Wave band, and this approach limits the overall synthesizer performance. As an example, mm-Wave frequency dividers are narrow-band or power hungry, while integrated VCOs display the best performance (efficiency, phase noise and tuning range) in a frequency range that is typically below 15 GHz [12].
Moving towards mm-Wave, a more efficient synthesis solution consists of employing frequency multipliers, cascaded to a lower frequency PLL, to reach the target band.
Frequency doublers (and in general even-order multipliers realized by cascading doublers) are commonly preferred over odd-order multipliers because of their intrinsic performance advantage. Multiple topologies are available, but they can mostly be classified into push-push rectifiers and multiplier-based frequency doublers.

Push-push topologies, whose concept is depicted in Fig. 2.1a, are based on a pair of class-B biased transistors, driven by anti-phase signals, which behave as full-wave rectifiers. Albeit very simple, this solution has several shortcomings. First, the conversion efficiency is limited; moreover, it needs a differential input while delivering a single-ended output, and it suffers from poor rejection of the fundamental frequency component. In fact, the input common mode arising from amplitude and phase unbalances on the (ideally balanced) driving signals is directly transferred to the output current. Different approaches have been investigated to mitigate the drawbacks of this structure. Push-push circuits combined with injection-locked oscillators have been proposed to boost the conversion gain and efficiency at the expense of bandwidth [13], [14], [15].

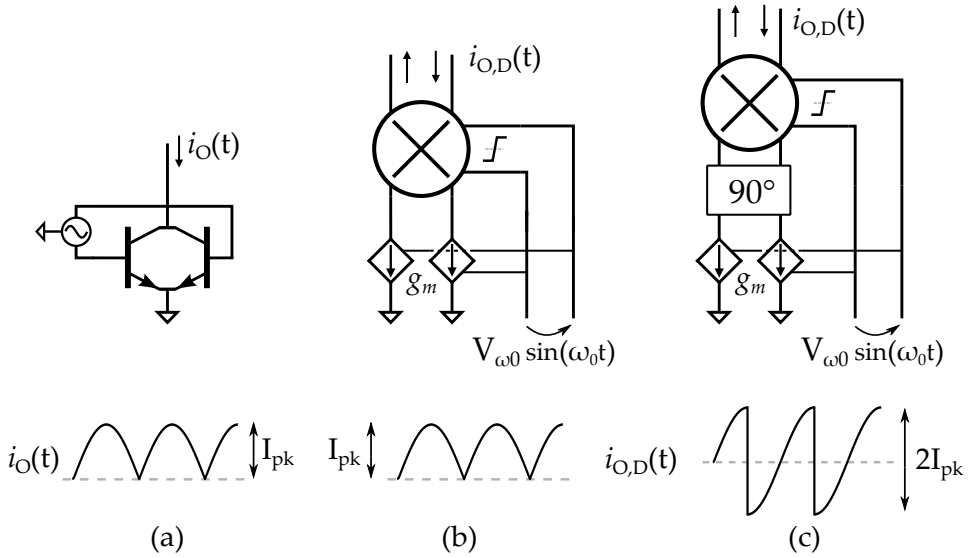


Figure 2.1: Frequency doubler architectures. Push-push pair (a) and Gilbert-cell mixer driven by in-phase (b) and in-quadrature (c) signals.

Solutions to attenuate the fundamental frequency at the output through harmonic traps, by cancelling the input common-mode, or by driving push-push structures with quadrature signals require tuned circuits [16], complex baluns [17] or hybrid couplers [18], thus again limiting the operation bandwidth or with a penalty in output power and efficiency [19]. Waveforms shaping [20] or the addition of a balancing branch to the push-push pair [21] display enhanced fundamental frequency rejection and broadband operation at the expense of reduced conversion gain or even high conversion loss [20].

Frequency doublers can also be realized with analog multipliers. When both the input ports are fed with signals at angular frequency ω_0, the fundamental component of the output signal contains a component at $2\omega_0$. Double-balanced Gilbert-cell mixers are the natural implementation of analog multipliers, where one ports is linear with the input signal while the other operates in saturation. As shown in Fig. 2.1b, when both the inputs are driven by the same signal, the mixer provides a full-wave rectified output current as in the case of the push-push doubler. But, contrary to the push-push rectifier, a double-balanced Gilbert cell operates with fully differential input and output signals, thus it is ideally insensitive to the input common-mode. This feature grants an advantage on the rejection of the input-frequency component and all odd harmonics in general. The architecture in Fig. 2.1b is intrinsically broadband, as confirmed by the design in [22] which targets ultra-wide operation bandwidth. The major limitation of an in-phase-driven Gilbert cell is the relatively low 2^{nd} harmonic conversion coefficient, a_2, defined as the fundamental Fourier component of

the output current (at $2\omega_0$) normalized to the peak input amplitude I_{pk}. As for the push-push rectifier, $a_2 = 0.42$. In addition, looking at the waveform in Fig. 2.1b, a strong DC component is present in the differential output current with a value, normalized to I_{pk}, equal to $a_0 = 0.63$. The non-zero mean current might be problematic when resistive loads are employed in ultra-wideband designs [22], [23].
These issues are solved driving the two ports of the mixer with quadrature signals, as shown in Fig. 2.1c. The previously considered rectified output current is here chopped at half the period, producing a symmetrical signal with zero DC component ($a_0 = 0$). Noticing that the two waveforms at the bottom of Fig. 2.1b and 2.1c have the same total energy, $a_0 = 0$ in Fig. 2.1c implies a higher harmonic content. In fact, by computing the Fourier components, $a_2 = 0.85$, i.e. the harmonic conversion gain of the quadrature-driven Gilbert-cell is doubled. On the other hand, the frequency doubler architecture of Fig. 2.1c needs a quadrature phase-shifting block, commonly implemented with a polyphase filter [24] or with a hybrid coupler [25], which sets an intrinsic bandwidth limitation along with the addition of losses and area occupation.

In [26], [27] we have proposed a novel approach to improve the overall performance of a Gilbert-cell based frequency doubler. If the saturated port of the mixer is driven at a deliberately reduced duty-cycle, the DC component on the output current is removed while simultaneously boosting the second harmonic conversion gain. The reduced duty-cycle is self-adjusted by a low-frequency feedback loop to maintain optimal operating conditions. The proposed approach still shows a good odd-harmonics suppression, typical of Gilbert-cell frequency doublers, combined with the high conversion efficiency of the solution in Fig. 2.1c. In addition, by avoiding quadrature generation, it allows for wideband operation.
The operation principle is first demonstrated at low frequency, with a doubler covering the full K-band [27], where transistor parasitics and interconnections do not introduce significant phase shifts. A direct comparison with a conventional mixer based frequency doubler driven by quadrature signals is carried out with the same technology and core structure. The results show a performance advantage in terms of bandwidth, gain and efficiency. The same concept is then implemented at sub-THz frequency with a doubler covering the D-band [28]. In this case, the RF core is modified to account for the relevant and unavoidable phase shifts introduced by parasitic components, ensuring an in-phase driving of the mixer input ports.

The chapter starts with explaining the operation principle of the proposed frequency doubler and its robustness against impairments. Then the design of the K-band frequency doublers is described, including thorough design

consideration for the feedback loop controlling the duty-cycle, followed by measurements and comparison table. Later, the D-band implementation of the same operating principle is reported along with the measurement results, eventually followed by the conclusion.

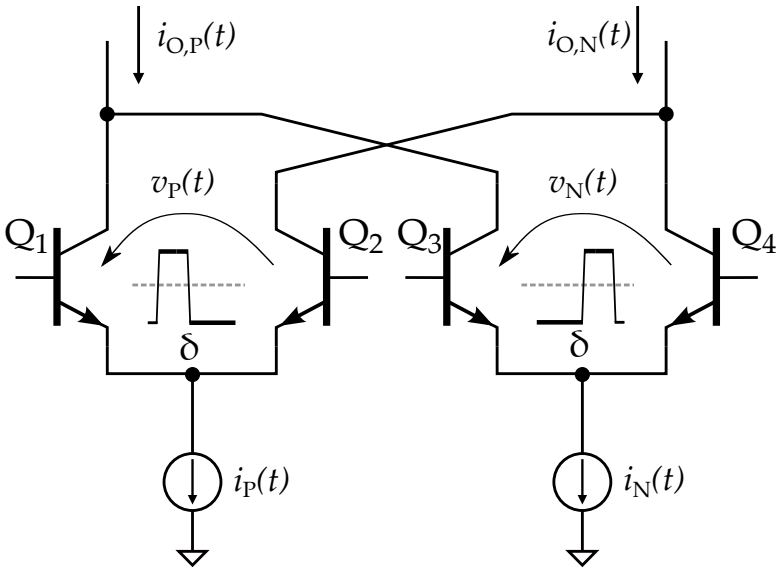


Figure 2.2: Frequency doubler based on a Gilbert-cell mixer.

2.1 Proposed Frequency Doubler

2.1.1 Operation Principle

The proposed frequency doubler is built around a conventional double-balanced Gilbert-cell mixer with the core schematic drawn in Fig. 2.2. The current sources $i_{P/N}(t)$ represent the tail transconductors, operating in class-A with a DC current I_{DC} and injecting sinusoidal differential currents with amplitude I_{pk} at angular frequency ω_0:

$$\begin{cases} i_P(t) = I_{DC} + I_{pk}\sin(\omega_0 t) \\ i_N(t) = I_{DC} - I_{pk}\sin(\omega_0 t) \end{cases} \tag{2.1}$$

The switching-quad transistors $Q_{1,2}$ - $Q_{3,4}$ are assumed to be driven with sufficiently large signals, $v_P(t)$, $v_N(t)$, to operate as ideal current switches or, equivalently, the differential driving signals $v_P(t)$ and $v_N(t)$ are considered as square waves with duty-cycle δ. With the assumption above, the differential output current is:

$$i_{O,D}(t) = \frac{1}{2}\left(i_{O,P}(t) - i_{O,N}(t)\right)$$

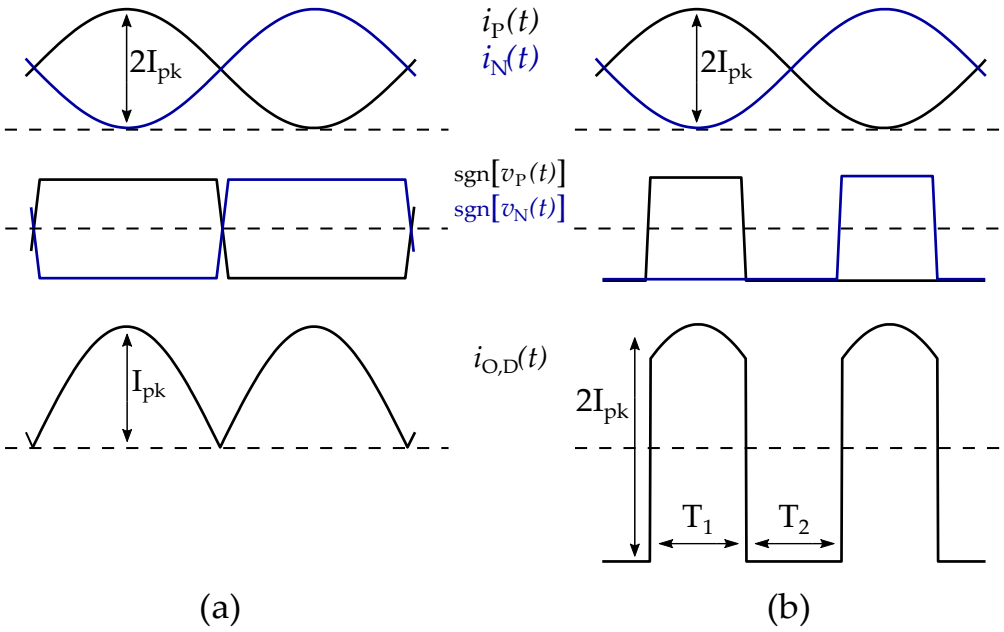


Figure 2.3: Waveforms with (a) $\delta = 50\%$, (b) $\delta = 25\%$.

$$\rightarrow i_{O,D}(t) = \frac{1}{2}\big(i_P(t)\cdot \mathrm{sgn}[v_P(t)] + i_N(t)\cdot \mathrm{sgn}[v_N(t)]\big) \tag{2.2}$$

where $\mathrm{sgn}[\cdot]$ denotes the well-known sign function.
The resulting characteristic waveforms with a switching-quad duty-cycle of $\delta = 50\%$ are plotted in Fig. 2.3a. In this situation, the Gilbert-cell mixer operates as a full-wave rectifier, with the output current given by:

$$i_{O,D}(t) = \frac{1}{2}\big|i_P(t) - i_N(t)\big| = \big|I_{pk}\sin(\omega_0 t)\big| \tag{2.3}$$

The fundamental component, $I_{O,2\omega 0}$, is at twice the input frequency and the second-harmonic current conversion gain, defined as the ratio between $I_{O,2\omega 0}$ and the amplitude of the input current, I_{pk}, is:

$$a_2 = \frac{I_{O,2\omega 0}}{I_{pk}} = \frac{4}{3\pi} \sim 0.42 \tag{2.4}$$

The circuit performance can be improved by reducing the switching-quad duty-cycle to $\delta = 25\%$, as shown by the waveforms in Fig. 2.3b. In this case, by using (2.2), the output current $i_{O,D}(t)$ can be written as:

$$i_{O,D}(t) = \begin{cases} \frac{1}{2}\big(i_P(t) - i_N(t)\big) = I_{pk}\sin(\omega_0 t) & t \in T_1 \\ \frac{1}{2}\big(-i_P(t) - i_N(t)\big) = -I_{DC} & t \in T_2 \end{cases} \tag{2.5}$$

The bottom plot in Fig. 2.3b shows $i_{O,D}(t)$ assuming the Gilbert-cell transconductors are operating at the edge of Class-A, i.e. with $I_{pk} = I_{DC}$. $i_{O,D}(t)$

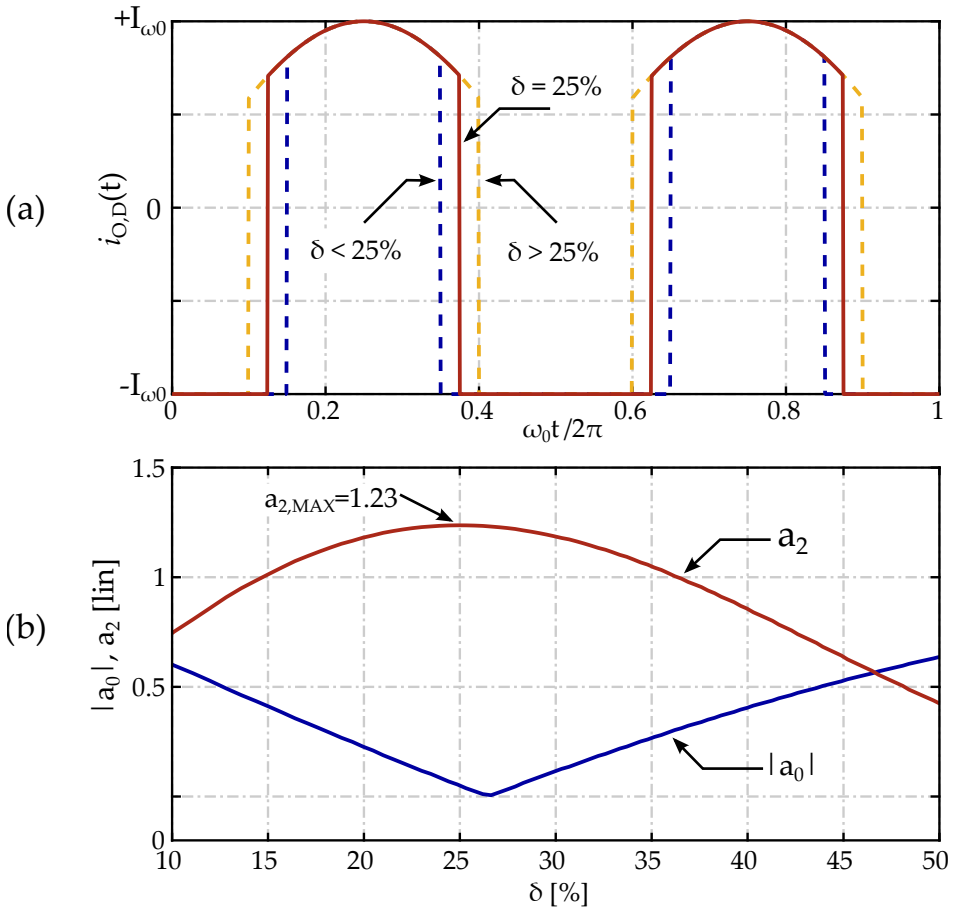


Figure 2.4: (a) Time domain waveforms vs duty-cycle δ, (b) DC (a_0) and second harmonic (a_2) coefficients against duty-cycle δ.

assumes an almost square-wave shape with a fundamental component at twice the input frequency. Approximating the waveform as a perfect square wave, the second-harmonic current conversion gain can be roughly estimated as $a_2 \sim \frac{4}{\pi} = 1.27$.

Still considering $I_{pk} = I_{DC}$, to gain more insight, Fig. 2.4a shows graphically how the switching-quad duty-cycle modifies the shape of $i_{O,D}(t)$ by modulating the duration of T_1 and T_2, thus impacting on the mean value of the waveform, $\overline{i_{O,D}(t)}$, and its fundamental component, $I_{O,2\omega 0}$ (at twice the input frequency). Fig. 2.4b plots the normalized DC component of $i_{O,D}(t)$ ($a_0 = \overline{i_{O,D}(t)}/I_{pk}$) and the second-harmonic current conversion gain (a_2), versus δ. $\delta = 25\%$ gives $a_{2,MAX} = 1.23$ which is an increase of 3 times (9.5 dB) compared the case of $\delta = 50\%$ duty-cycle previously considered (eq.(2.4)), and yet a remarkable 1.5x (3.5 dB) over the implementation shown in Fig. 2.1c where the input transconductors and the switching quad are driven by signals in quadrature phase. Still looking at Fig. 2.4b, at $\delta = 25\%$ the DC component of $i_{O,D}(t)$ is almost zero. a_0 is perfectly nulled at a slightly higher duty-cycle ($\delta \sim 26\%$) because the shape of $i_{O,D}(t)$ is not exactly a square wave.

In summary, a reduced duty-cycle (ideally $\delta = 25\%$) for the Gilbert-cell frequency doubler yields an output signal almost free of DC offset and a remarkable improvement of the harmonic conversion gain. It is also worth noticing that, regardless of the actual duty-cycle, the proposed approach preserves the fully balanced topology of the circuit, and thus an enhanced robustness to the leakage of the input signal and odd harmonics.

2.1.2 Duty-cycle Control Mechanism

Generating and distributing a square-wave signal to drive the switching quad at the desired duty-cycle is obviously not feasible at RF and mm-Wave, given the high harmonic content it involves.
A more practical solution consists in exploiting the large signal behavior of the switching quad. In fact, provided the driving signal amplitude is sufficiently large, the two differential pairs in Fig. 2.2 ($Q_{1,2}$ - $Q_{3,4}$) are sensitive to the sign of the differential signals $v_P(t)$, $v_N(t)$ and, ideally, not to the amplitude. Therefore, as shown in Fig. 2.5, the switching-quad duty-cycle can be reduced by applying a positive differential DC offset voltage, V_{OS}, to the base of the differential-pair transistors.
If $v_{IN}(t) = V_{\omega 0}\sin(\omega_0 t)$ is the voltage feeding the mixer, the signals at the base of $Q_{1,2}$ and $Q_{3,4}$ in Fig. 2.5 are:

$$\begin{cases} v_P(t) = V_{OS} + V_{\omega 0}\sin(\omega_0 t) \\ v_N(t) = V_{OS} - V_{\omega 0}\sin(\omega_0 t) \end{cases} \tag{2.6}$$

and the offset voltage which gives the desired switching duty-cycle (i.e. $\delta = 25\%$) can be immediately calculated:

$$V_{OS} = V_{\omega_0}\cos(\pi\delta) \Rightarrow V_{OS}\big|_{\delta=25\%} = \frac{V_{\omega_0}}{\sqrt{2}} \tag{2.7}$$

Notably, if $v_{IN}(t)$ is the same signal driving the transconductors of the Gilbert cell, the addition of V_{OS} allows a simple regulation of the switching-quad

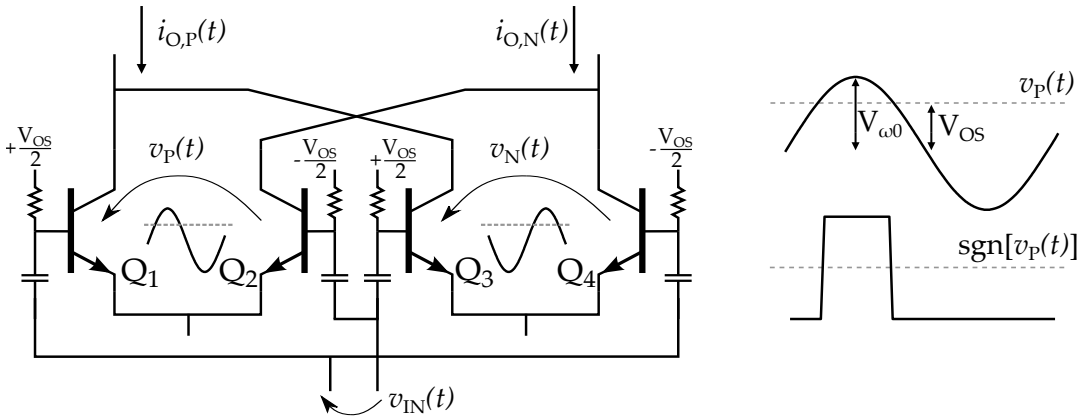


Figure 2.5: Offset-Duty cycle control mechanism.

duty-cycle while maintaining the correct timing shown in Fig. 2.3b, where the high-state of the equivalent square-wave switching signal is aligned to the peaks of the tail currents $i_{P,N}(t)$.
Eq.(2.7) shows that V_{OS} cannot be statically set, being dependent on the driving signal amplitude, V_{ω_0}, which is in general not precisely defined and subject to low-frequency drift. The use of an envelope detector to generate V_{OS} proportional to V_{ω_0} could be an option, with the drawback of high sensitivity to components spread and to the accuracy of the detector itself. Moreover, this open-loop approach is sub-optimal, not providing any correction to the non-ideal behavior of the switching quad, which becomes sensitive to the driving signal level when the amplitude is reduced.
A more robust and effective approach is suggested by noticing in Fig. 2.4 that, opposite to the case of $\delta = 50\%$, $\delta = 25\%$ leads to a quasi square-wave output current $i_{O,D}(t)$ with almost zero DC component. Being the mean value of the $i_{O,D}(t)$ relatively easy to measure, a low-frequency feedback loop can be closed to automatically adjust V_{OS} in order to null the DC component $\overline{i_{O,D}(t)}$. This technique yields a robust and nearly optimal performance, also compensating the real behavior of the switching quad at low driving amplitude V_{ω_0}.
To gain further insight, Fig. 2.6 plots the normalized DC component of $i_{O,D}(t)$ (a_0) and the second-harmonic current conversion gain (a_2) derived from simulations of the circuit in Fig. 2.5 at different V_{ω_0}. The equivalent duty-cycle on the horizontal axis is regulated by changing V_{OS} and calculated with (2.7). With large amplitude (grey curves) the switching-quad behavior is close to the ideal case and the maximum conversion gain is achieved close to $\delta = 25\%$. When V_{ω_0} is reduced (orange and red curves), $Q_{1,2}$ - $Q_{3,4}$ no longer behave

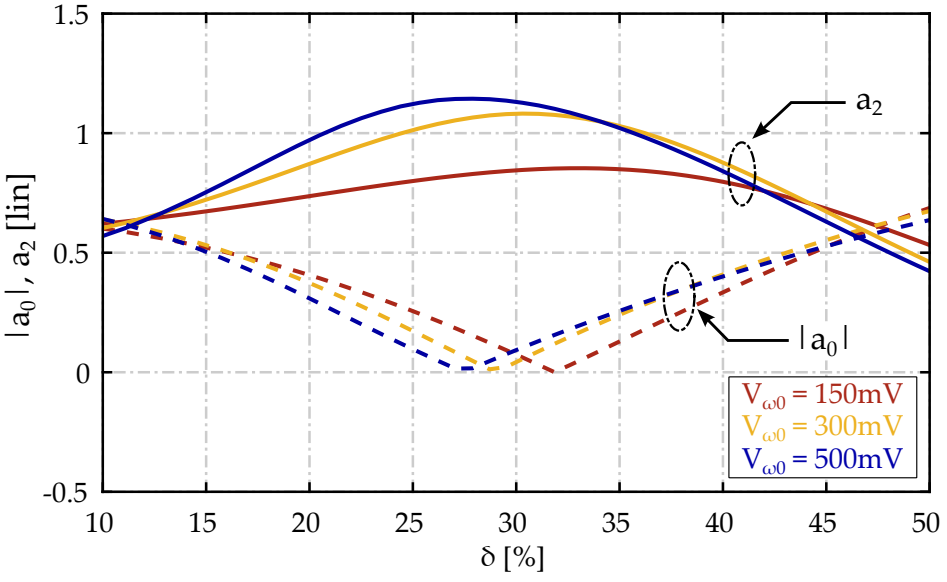


Figure 2.6: Simulated DC and second-harmonic coefficients, a_0, a_2, of the differential output current $i_{O,D}(t)$ versus δ for different V_{ω_0}.

as ideal switches and a_2 is maximized with a higher duty-cycle. Although a_2 is relatively flat around the points of maxima, the different curves in Fig. 2.6 show that the notches of a_0 track the peaks of a_2. Hence, by setting V_{OS} to null the DC component of the output differential current, the circuit is forced to operate at the points of maximum second-harmonic conversion gain, granting robustness and optimal performance against variation of V_{ω_0}.

Finally, it is worth mentioning that the proposed approach for the switching-quad duty-cycle control is not sensitive to phase variations of the input signal and, more importantly, it does not affect the phase of the output signal. In fact, recalling Fig. 2.4a, the variation of duty-cycle modulates the duration of the high and low levels of the switching waveform, T_1 and T_2, without impacting on the phase of the fundamental current component. This leads to the important observation, confirmed by simulations, that the loop parameters (such as gain, bandwidth and noise) do not impair the phase noise of the output signal.

2.1.3 Robustness to Input Amplitude Variation and Phase Skew

The output signal amplitude of Gilbert-cell frequency doublers is penalized by a reduction of the input driving level and by unwanted phase delay between the signals feeding the two input ports of the mixer. The robustness against these two impairments is evaluated in this section comparing the performance of a frequency doubler based on a Gilbert cell driven by quadrature signals (which features higher conversion gain, compared to in-phase driving) and the proposed architecture implementing a loop with self-adjusted switching-quad duty-cycle.
The detailed block diagrams of the two architectures are reported in Fig. 2.7. In both cases, a differential transconductor (g_m) driven by the input voltage $v_{IN}(t) = V_{\omega 0} \sin(\omega_0 t)$ generates the currents $i_P(t)$, $i_N(t)$ given by (2.1). In Fig. 2.7a the voltage $v_{IN}(t)$ feeds directly the hard-switching port of the mixer while the two currents $i_P(t)$, $i_N(t)$ are 90° shifted before the injection into the linear port. In Fig. 2.7b the linear and saturated ports of the mixer are ideally driven in phase. A DC voltage, V_{OS}, generated by a low-frequency feedback loop, is added to $v_{IN}(t)$ at the hard-switching port, to null the output DC component by reducing the switching-quad duty-cycle.
In both architectures an unwanted phase shift $\Delta\Phi$ is added to $v_{IN}(t)$ along the path toward the switching quad. This $\Delta\Phi$, unavoidable in practice, represents for example the delay added by routing parasitics in circuit layout. For the frequency doubler in Fig. 2.7a, $\Delta\Phi$ has obviously the same effect of a phase error of the 90° phase shifter on the input currents. The impact of the input amplitude, $V_{\omega 0}$, and $\Delta\Phi$ on the output signal amplitude is now evaluated.

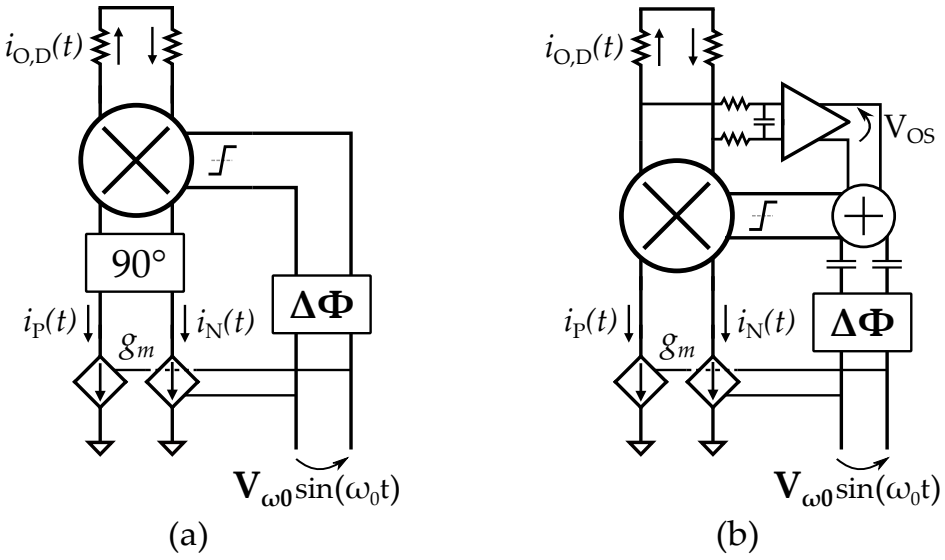


Figure 2.7: Block diagrams of the quadrature-driven Gilbert-cell based frequency doubler (a) and the presented reduced duty-cycle solution (b).

Assuming hard-switching operation of the mixer, the output differential current for the quadrature-driven Gilbert cell in Fig. 2.7a is given by:

$$i_{O,D}(t) = I_{pk}\cos(\omega_0 t)\cdot \mathrm{sgn}[\sin(\omega_0 t + \Delta\Phi)] \tag{2.8}$$

with $I_{pk} = g_m V_{\omega 0}$. The magnitude of the fundamental component of $i_{O,D}(t)$, $I_{O,2\omega 0}$, can be derived considering the 1st and 3rd order components of the Fourier expansion of the sign function. With some algebraic and trigonometric manipulations:

$$I_{O,2\omega 0} = I_{pk}\frac{4}{3\pi}\sqrt{4\cos^2(\Delta\Phi) + \sin^2(\Delta\Phi)} \tag{2.9}$$

From (2.9), the output amplitude of a quadrature-driven mixer is proportional to the input signal amplitude (being $I_{pk} = g_m V_{\omega 0}$) and the harmonic conversion gain is reduced from its maximum ($a_{2,MAX} = 8/3\pi \sim 0.85$) when $\Delta\Phi = 0$, reaching a minimum for $\Delta\Phi = \pm 90°$ (i.e. when the two ports of the multiplier are driven in phase). To gain insight, the impact on the output second harmonic component $I_{O,2\omega 0}$ of a 3 dB reduction in I_{pk} and $\pm 45°$ in $\Delta\Phi$ is graphically shown by the blue area on the plot in Fig. 2.8.

The same analysis in closed-form cannot be carried out for the proposed frequency doubler architecture in Fig. 2.7b, since $V_{\omega 0}$ and $\Delta\Phi$ influence both the fundamental and DC components of the output, thus affecting the steady-state V_{OS} and switching-quad duty-cycle set by the feedback loop. The impact

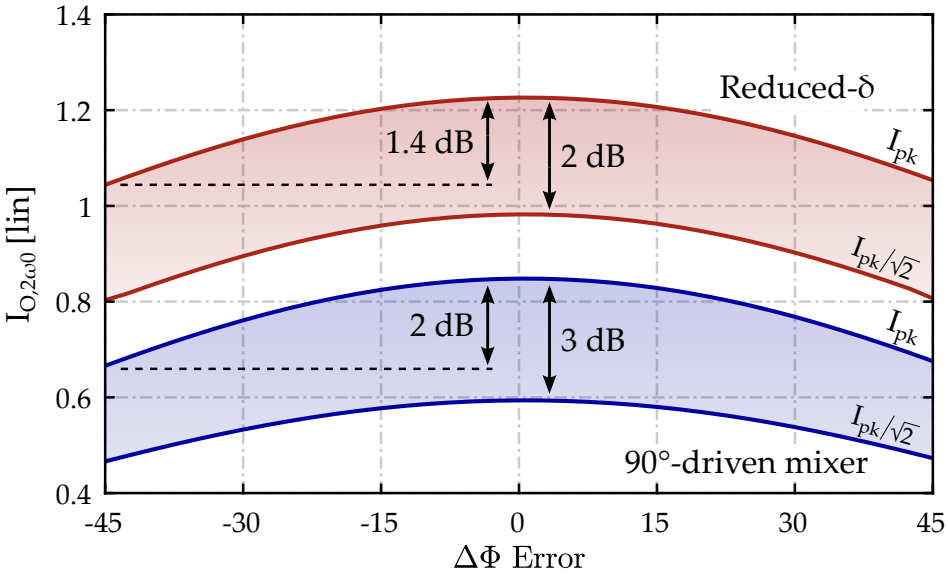


Figure 2.8: Simulated second-harmonic component $I_{O,2\omega 0}$ of the reduced duty-cycle and quadrature-driven mixer based frequency doublers against amplitude (3 dB) and phase ([-45, 45]°) variations from the ideal values.

of the two parameters is evaluated with numerical simulations and the results are plotted in the red area of Fig. 2.8. Comparing the blue and red curves, the proposed frequency doubler architecture displays a slightly lower sensitivity to both $\Delta\Phi$ and input amplitude reduction, with respect to the conventional solution of Fig. 2.7b. $\Delta\Phi = \pm 45°$ leads to a conversion gain penalty of 1.4 dB (instead of 2 dB) while a reduction of 3 dB of the input signal level causes 2 dB (instead of 3 dB) attenuation of the output amplitude. Intuitively, the enhanced robustness to the impairments can be explained looking back at the expression of the output differential current given by (2.5): $i_{O,D}(t)$ is sensitive (proportional) to the input signal only during T_1, while in the other part of the period (T_2) it is set by the DC bias current I_{DC} and not affected by $V_{\omega 0}$ and $\Delta\Phi$.

2.2 K-Band Frequency Doublers - Circuit Design

A conventional quadrature-driven Gilbert-cell frequency doubler and the proposed self-adjusted reduced duty-cycle architecture have been designed for experimental performance comparison. The circuits are implemented in a BiCMOS 0.13µm technology process and the design is presented in this section.

2.2.1 Quadrature-driven Gilbert-cell Frequency Doubler

Various quadrature-driven Gilbert-cell mixers are proposed in the literature, with the main difference in the position and implementation of the 90° phase

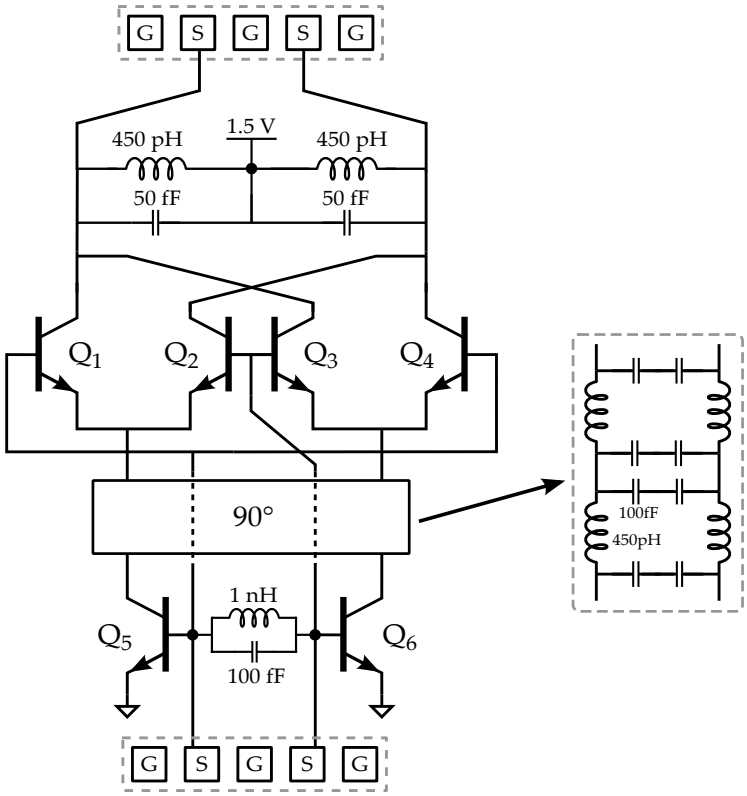


Figure 2.9: Schematic of the quadrature-driven Gilbert-cell frequency doubler.

shifter. As an example, in [25] a hybrid coupler generates the voltage signals in quadrature to drive the two input ports of the mixer. In [29], [30] the 90° phase shift is implemented in the current domain and placed between the common-emitter input devices and the switching-quad transistors of the Gilbert-cell. In this case, the impedance transformation performed by the phase shifter yields some current gain, improving the overall frequency doubler conversion gain. The schematic of the quadrature-driven mixer is shown in Fig. 2.9, where biasing circuits are omitted for simplicity and readability. The Gilbert-cell switching quad is formed by $Q_{1,2}$ - $Q_{3,4}$ while $Q_{5,6}$, in common-emitter configuration, implement the input transconductors. All the transistors have the same emitter area of 8 µm x 0.13 µm. A lumped-element delay line is inserted between the common emitter devices and the switching quad to introduce a 90° phase shift at the nominal center input frequency of 10 GHz. The line, with characteristic impedance $Z_{0,D} = 100\,\Omega$, is realized with two C-L-C sections where the capacitors also absorb the equivalent parasitic capacitances at the collectors of $Q_{5,6}$ and at the emitter nodes of the switching quad. The simulated insertion loss of the delay line is ~0.9 dB. Resonant networks are used for input matching and to provide the optimal load impedance at the output in order to maximize the saturated power, P_{sat}. The DC current of the input transistors, $Q_{5,6}$, is 2 x 7 mA and the supply voltage is $V_{CC} = 1.5$ V.

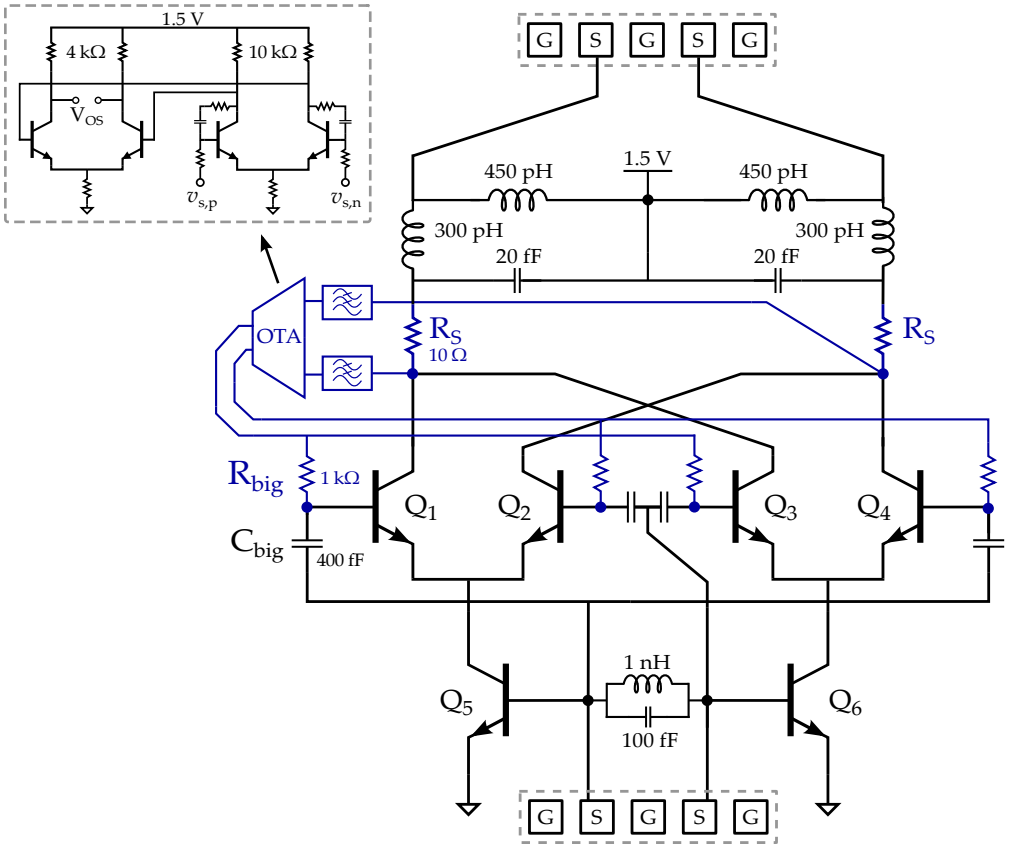


Figure 2.10: Schematic of the proposed reduced duty-cycle mixer based frequency doubler. Components in blue are part of the baseband feedback loop.

2.2.2 Gilbert-cell Frequency Doubler with Self-Adjusted Duty-cycle

The schematic of the proposed frequency doubler architecture is shown in Fig. 2.10. The size of the transistors in the Gilbert cell, the DC currents and the supply voltage are the same used in the quadrature-driven mixer doubler previously described. The output network is slightly modified to match the optimal load without penalizing the wider circuit bandwidth, no more limited by the use of a 90° phase shifter.
The low-frequency feedback loop controlling the switching-quad duty-cycle is implemented with a fully-differential OTA which senses the DC output current through a pair of resistors, R_S, and provides a differential V_{OS} DC component to the base of $Q_{1,2}$ and $Q_{3,4}$. The value of resistors $R_S = 10\,\Omega$ is chosen as a compromise between low DC voltage drop and robustness against the input offset voltage of the OTA. The OTA is designed with 1.25 V output common mode voltage such that the DC voltage at the base of $Q_{1,2}$ - $Q_{3,4}$ can range from 1 V to 1.5 V, corresponding to a maximum $V_{OS} = 500\,\text{mV}$. Choke resistors $R_{big} = 1\,\text{k}\Omega$ are used to feed the DC base voltage to the switching-quad transis-

tors while the input signal is coupled through capacitors $C_{big} = 400\,fF$.
The schematic of the OTA is shown as an inset in Fig. 2.10. It is composed of two cascaded differential stages with bipolar input transistors to benefit from the high transconductance and low offset voltage. The current consumption is 200 µA from 1.5 V supply. Miller capacitors with zero-nulling resistors are placed across the first stage with the dual purpose of limiting the loop bandwidth and, together with resistors in series to the input of the OTA, to suppress the RF signal at the sense nodes ($v_{S,P}$, $v_{S,N}$), avoiding the saturation of the OTA input pair due to the excessive RF voltage swing. The gain of the OTA and the size of Miller capacitors are carefully selected not to compromise the loop stability while maintaining sufficiently high loop gain, as discussed in the following sub-section.
The DC power consumption of the proposed frequency doubler is 21 mW from 1.5 V supply. The voltage drop across the sense resistors and the power consumption of the OTA are responsible for roughly 1 mW, i.e. only 5% of the total.

2.2.3 Loop Gain Analysis and Design Considerations

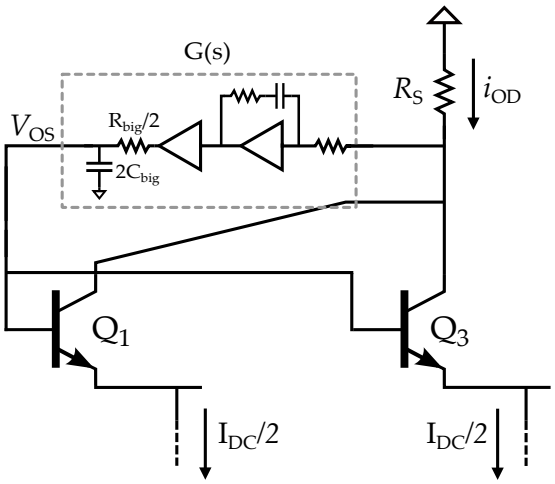


Figure 2.11: Differential-mode half-circuit schematic of the low frequency feedback loop.

At low frequency, within the bandwidth of interest for the loop-gain analysis, inductors and capacitors in the output matching network of the circuit in Fig. 2.10 can be considered short- and open-circuits, respectively. Therefore, the feedback loop can be analyzed considering the simplified schematic in Fig. 2.11, where the Gilbert-cell is replaced with a differential-mode equivalent

half-circuit. The loop gain $T(s)$ can be written as:

$$T(s) = R_S \cdot G(s) \cdot G_m \tag{2.10}$$

where $G(s)$ represents the OTA open-loop transfer function and G_m is the equivalent transconductance of the transistors Q_1 and Q_3. For simplicity, all the poles of $T(s)$ are concentrated within the OTA, including also the decoupling network R_{big}-C_{big}. The poles introduced by the switching-quad transistor parasitics appear at a much higher frequency and can be neglected.
At the quiescent point, i.e. without the input signal applied to the frequency doubler, the equivalent transconductance G_m simplifies to the small-signal transconductance of $Q_{1,3}$:

$$G_m = G_{m,SS} = 2g_{m1,3} \tag{2.11}$$

The small-signal loop gain $T(s)$ is shown in Fig. 2.12 with $T(0) = 48\,\text{dB}$ and a cut-off frequency (0 - dB gain) of $\sim 150\,\text{MHz}$. Miller capacitors are not sufficient to ensure a dominant pole compensation, therefore the nulling resistance is used to move its associated zero to the left half-plane and cancel the second pole, providing a safe stability margin of $\sim 70°$.

When the input signal is applied to the frequency doubler, the large-signal operation of the switching quad affects the loop gain. To take this effect into account, the equivalent transconductance G_m to be used in (2.10) must link the variation of the DC component in the output differential current, $\overline{i_{O,D}(t)}$, to a variation of the voltage V_{OS} applied by the OTA to the base of $Q_{1,2}$ - $Q_{3,4}$. Assuming hard-switching operation of the switching quad, the large-signal G_m can be evaluated by first linking the mean value of the output current to a variation of the switching-quad duty-cycle δ. $i_{O,D}(t)$ is given by (2.5) and the effect of δ on its shape is shown graphically in Fig. 2.4a. By integrating the waveform, the mean value is:

$$\overline{i_{O,D}(t)} = I_{pk}\left(2\delta - 1 + \frac{2}{\pi}\sin(\pi\delta)\right) \tag{2.12}$$

while the relation between δ and V_{OS} is derived from (2.7):

$$\delta = \frac{1}{\pi}\cos^{-1}\frac{V_{OS}}{V_{\omega 0}} \tag{2.13}$$

where $V_{\omega 0}$ is the amplitude of the RF signal driving the switching quad, which corresponds to the input amplitude of the frequency doubler. Combining (2.12) and (2.13), the equivalent large-signal transconductance can be expressed as:

$$G_m = G_{m,LS} = \frac{\partial\,\overline{i_{O,D}(t)}}{\partial\,V_{OS}} \tag{2.14}$$

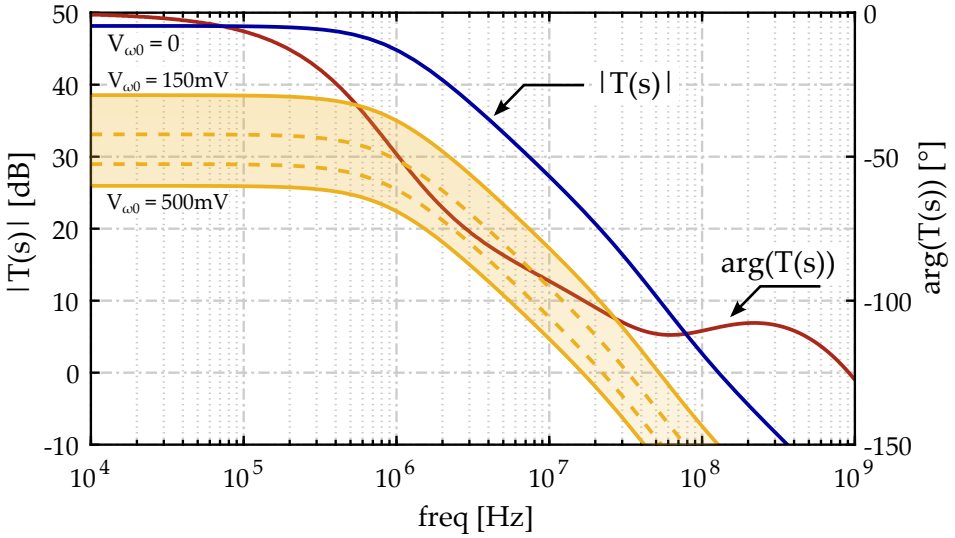


Figure 2.12: Bode plot of the Loop Gain $T(s)$. Red curve - small signal loop gain magnitude. Yellow area - Large signal loop gain magnitude with $V_{\omega 0} = [150 - 500]$ mV.

Linearizing around the nominal operating regime of $\delta = 25\%$ and replacing $V_{OS} = \frac{V_{\omega 0}}{\sqrt{2}}$ from (2.7),

$$G_{m,LS} \sim 1.5 \frac{I_{pk}}{V_{\omega 0}} \tag{2.15}$$

The equation above can be further elaborated to achieve a more insightful comparison of the loop gain in large and small signal regimes. At large signal the transconductors $Q_{5,6}$ in Fig. 2.10 inject into the switching quad a signal current (I_{pk}) nearly equal to the DC current I_{DC}. Substituting $I_{pk} = I_{DC}$ and noticing that the DC current in each transistor of the switching quad is $I_{DC}/2$, thus $g_{m3,5} = (I_{DC}/2)/v_t$ (being $v_t = 25$ mV the thermal voltage), (2.15) can be rewritten as:

$$G_{m,LS} \sim 1.5 \frac{I_{DC}}{V_{\omega 0}} = 1.5 \frac{2v_t}{V_{\omega 0}} g_{m1,3} = 1.5 \frac{v_t}{V_{\omega 0}} G_{m,SS} \tag{2.16}$$

Eq. (2.16) shows that when the frequency doubler is driven by a signal with amplitude larger than few tens of mV, the equivalent large-signal transconductance drops quickly below the small-signal level and the loop gain reduces with the inverse of $V_{\omega 0}$. Because all the poles/zeros in the loop gain belong to the OTA transfer function, the singularities of $T(s)$ are not affected and thus the closed loop bandwidth is reduced when $V_{\omega 0}$ increases. To gain further insight, the Bode plot of $T(s)$ is shown in Fig. 2.12 at the quiescent point ($V_{\omega 0} = 0$) and with $V_{\omega 0}$ from 150 mV to 500 mV. Increasing $V_{\omega 0}$, both the loop gain magnitude and the gain cross-over frequency (i.e. the closed loop bandwidth) decrease, while the poles/zeros positions and the phase response are not affected. Simulations also confirm quantitatively the result predicted by (2.16). With $V_{\omega 0} = 500$ mV, (2.16) predicts a decrease in loop gain of 22 dB and, assuming a single-pole 20 dB/dec slope, the closed-loop bandwidth is

reduced by roughly a factor of 10.

In summary, from a design perspective, the presented analysis reveals that, if a sufficient phase margin is achieved at the quiescent point, the stability is not compromised during operation. On the other hand, the target loop gain required to meet a desired performance (i.e. accuracy on the steady-state duty-cycle) has to be sized at the maximum expected input signal amplitude, where the loop gain is minimum. As an example, looking at the simulations in Fig. 2.6, a 10% relative error in the duty-cycle from the optimal value (i.e. $\delta \sim [23\text{-}29]\%$) leads to a negligible degradation in terms of harmonic conversion gain. At the same time, a 10% error in the duty-cycle corresponds to a roughly 10% error in the output DC component $\overline{i_{O,D}(t)}$. Being the steady-state error on $\overline{i_{O,D}(t)}$ equal to $1/|T(0)|$, the loop gain must remain greater than 20 dB, when the signal is present, to set $\overline{i_{O,D}(t)}$ with the accuracy of 10%.
The same consideration can be applied to evaluate the effect of the OTA equivalent input offset voltage, V_{os}. From Monte Carlo simulations, V_{os} at 3-σ is ± 1.5 mV, corresponding to a differential DC output current error of ± 150 µA. The previously considered 10% error on the duty-cycle results in a differential DC component of 450 µA, meaning that the OTA input offset voltage has a negligible impact on the overall doubler performance.
Moreover, as introduced in Sec. 2.1.2, the control of the duty-cycle does not change the phase of the second harmonic component of the output signal (Fig. 2.4a), meaning that impairments in the feedback loop, including the noise introduced by the OTA, may not degrade the phase noise performance of the frequency doubler.

2.2.4 Experimental Results

The photograph of the two realized frequency doublers is shown in Fig. 2.13. The core area occupation is 600 µm x 230 µm = 0.14 mm^2 and 180 µm x 420 µm = 0.075 mm^2 respectively for the quadrature-driven Gilbert cell (Fig. 2.13a), and for the proposed architecture (Fig. 2.13b). Including the input and output pads, the overall area of each implementation is 0.30 mm^2. For measurements, the die has been glued on a PCB which provides supply and biasing through bondwires. The input and output RF signals are interfaced with Cascade Infinity GSGSG probes. The differential input signal is provided through a pair of Agilent E8257D signal generators synchronized in antiphase through an external reference. On the output side, a balun is used for differential to single-ended conversion, and the output power is measured with Agilent PXA N9030A spectrum analyzer.

First, measurements are compared with simulations for the conventional quadrature-driven Gilbert-cell frequency doubler. Fig. 2.14 shows a sweep

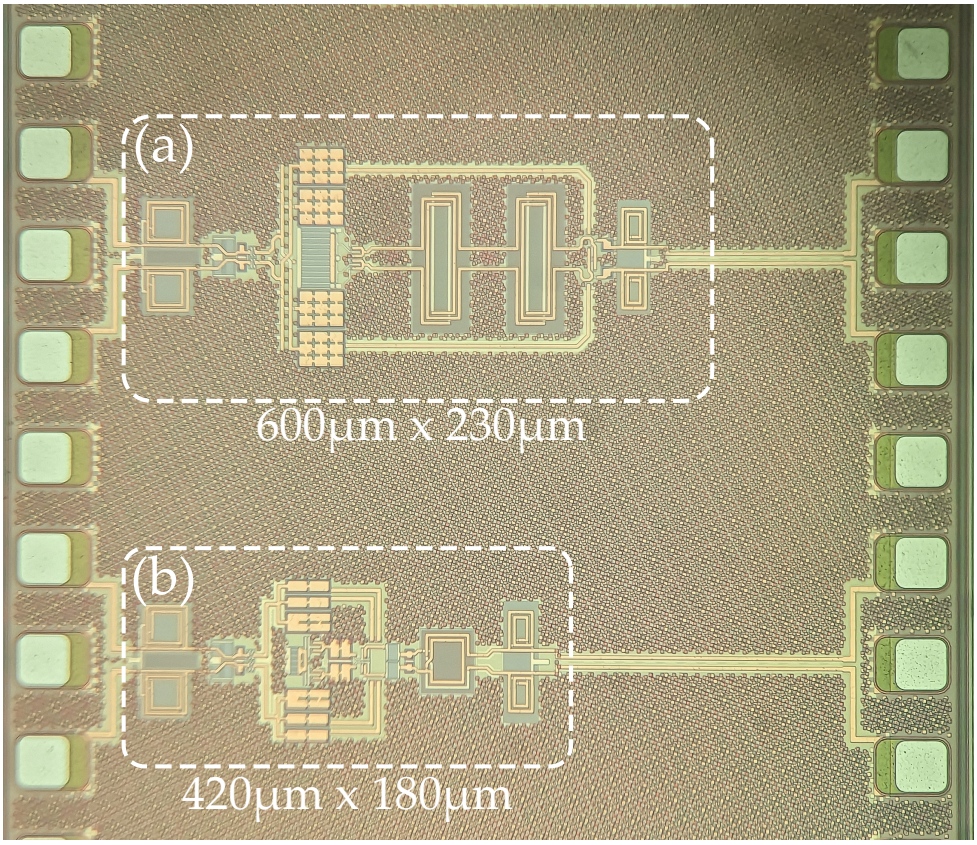


Figure 2.13: Photograph of the realized frequency doublers. Quadrature driven Gilbert-cell (a) and the proposed self-adjusted reduced duty-cycle (b).

of the input power at the center output frequency $f_{out} = 20\,GHz$, reporting a peak conversion gain of 5 dB. The conversion gain drops to below 0 dB for $P_{in} > 3\,dBm$. The maximum saturated output power is $P_{sat} = 3.3\,dBm$ and the collector efficiency ($\eta = P_{out}/P_{DC}$) is around 8%. The measured and simulated P_{sat} and efficiency versus the output frequency are plotted in Fig. 2.15, showing a peak $P_{sat} = 3.4\,dBm$ and a corresponding collector efficiency of 8.9%. The 3 dB-bandwidth, evaluated from the peak P_{sat}, is from 15 GHz to 24 GHz, corresponding to a 47% fractional bandwidth, with minor deviation from simulation results.

The same tests are performed for the proposed frequency doubler. Fig. 2.16 shows the results of the input power sweep at the output frequency $f_{out} = 20\,GHz$, reporting a peak conversion gain of 6 dB. The conversion gain drops to below 0 dB for $P_{in} > 5\,dBm$, after reaching P_{sat}. The saturated output power and efficiency versus output frequency are plotted in Fig. 2.17. The maximum saturated output power is $P_{sat} = 5.7\,dBm$, measured at $f_{out} = 24\,GHz$, where the power efficiency reaches 17%, almost 2 times higher than in the previous case. The 3 dB-bandwidth, still measured from the peak P_{sat}, is more than one octave, from 14 GHz to 32 GHz. The fractional bandwidth of 85% is nearly twice compared to the quadrature-driven Gilbert cell.

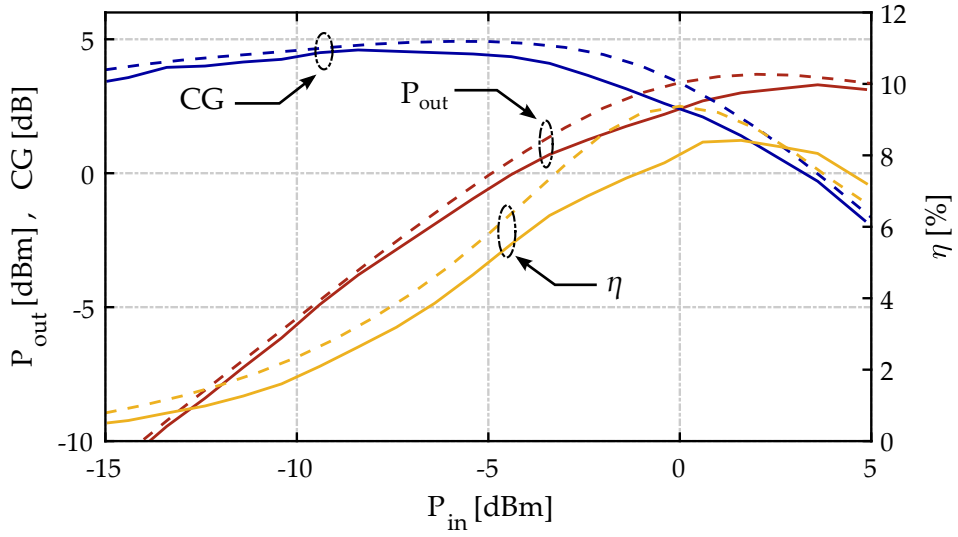


Figure 2.14: Quadrature-driven Gilbert Cell - Measured (solid) and simulated (dashed) output power (P_{out}), Gain (CG) and collector efficiency (η) vs input power P_{in} @ $f_{out} = 20\,GHz$.

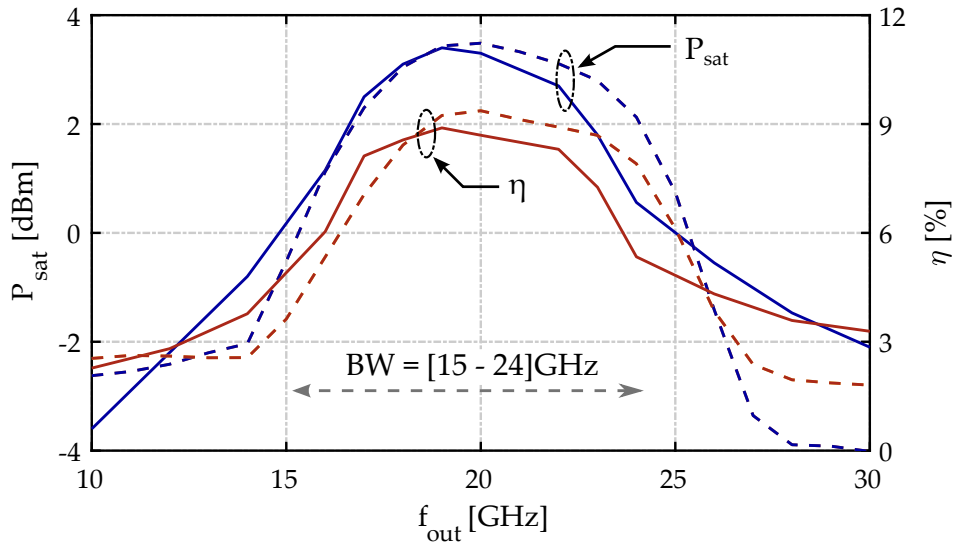


Figure 2.15: Quadrature-driven Gilbert Cell - Measured (solid) and simulated (dashed) output saturated power (P_{sat}), and collector efficiency (η) vs frequency.

A more extensive characterization has been performed for the proposed doubler with self-adjusted duty-cycle. The measured rejection of the driving signal (i.e. the fundamental component) is reported in Fig. 2.18, proving more than 40 dB across the full operational bandwidth. Fig. 2.19 shows the phase noise measured on the input signal (provided by the Agilent E8257D generator), at the output of the frequency doubler, and the difference between the two curves, ΔPN. The degradation of 6 dB, expected from frequency multiplication by 2, confirms the frequency doubler does not contribute to phase noise deterioration. The measured results on the two architectures are finally summarized

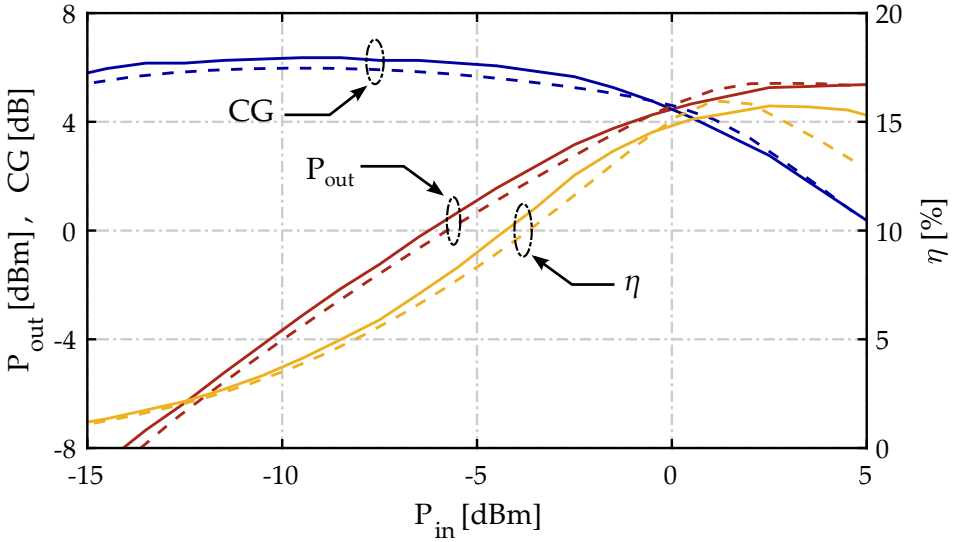


Figure 2.16: Proposed solution - Measured (solid) and simulated (dashed) output power (P_{out}), Gain (CG) and collector efficiency (η) vs input power P_{in} @ $f_{out} = 20\,GHz$.

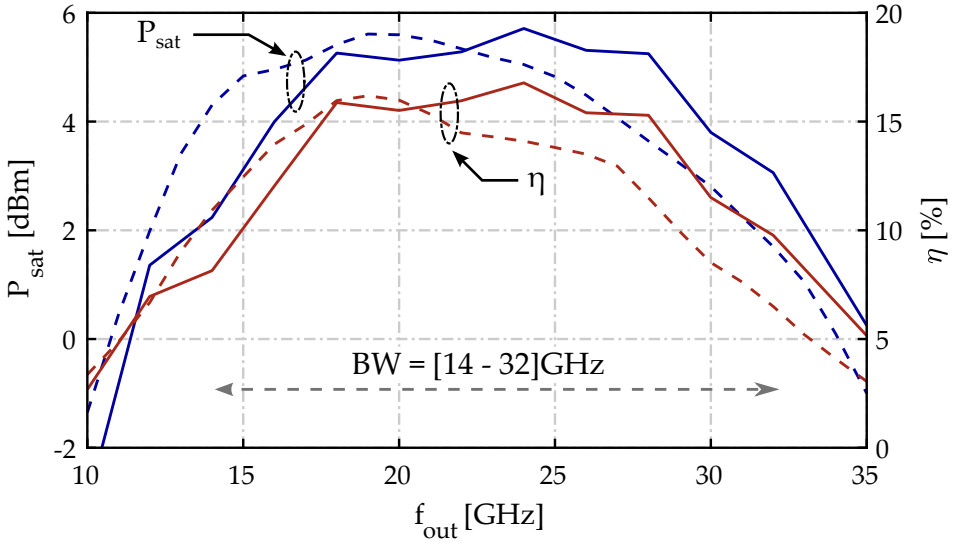


Figure 2.17: Proposed solution - Measured (solid) and simulated (dashed) output saturated power (P_{sat}), and collector efficiency (η) vs frequency.

in Table-2.1 and compared against previously reported frequency doublers operating in a similar frequency range. The implemented quadrature-driven Gilbert cell achieves a state-of-the-art bandwidth with good conversion gain, P_{sat} and η aligned with the average values of other works. The new proposed architecture highlights a remarkable improvement of the operating (fractional) bandwidth, except for [19] which lacks in terms of conversion gain and P_{sat}. This frequency doubler also demonstrates P_{sat} and efficiency (η) comparable or better than most of the previous works. It is worth noticing that the supply voltage of the presented doublers is 1.5 V, while the best efficiency in [17] [30] is achieved with the benefit of a remarkably higher supply, 2.5 V, which makes

the voltage headroom required to keep the stacked transistors in active region less relevant.

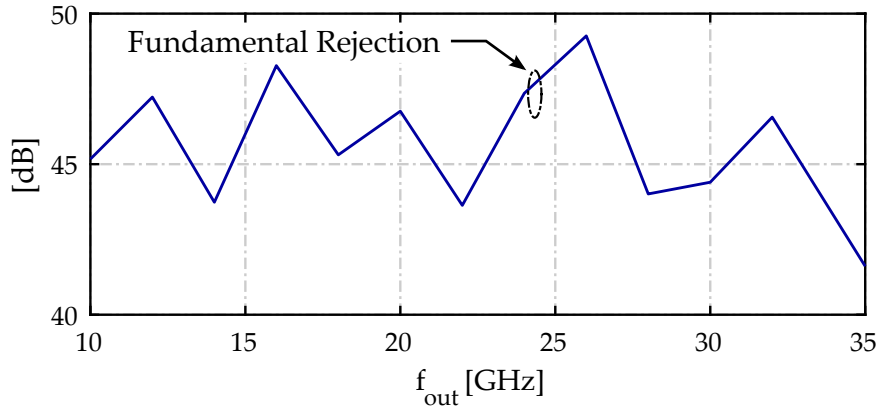


Figure 2.18: Proposed solution - Measured fundamental harmonic rejection vs frequency.

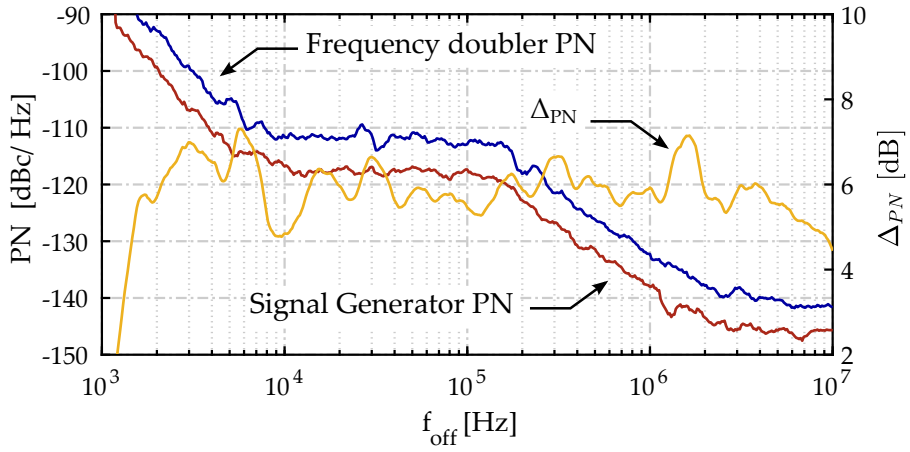


Figure 2.19: Proposed solution - Measured phase noise of the frequency doubler @ $f_{out} = 20\,GHz$ vs measured phase noise of the input signal generator.

Table 2.1: Performance summary and comparison table.

	This Work Reduced-δ	This Work 90°-driven	[17]	[18]	[19]	[25]	[30]	[31]	[32]	[33]	[34]	[35]
Technology	0.13 µm SiGe	0.13 µm SiGe	0.13 µm SiGe	65 nm CMOS	0.18 µm CMOS	90 nm CMOS	0.13 µm SiGe	0.13 µm SiGe	0.11 µm CMOS	0.15 µm GaAs	0.18 µm SiGe	55 nm CMOS
Frequency [GHz]	14 - 32	15 - 24	25 - ,40	23 - ,25	15 - 36	40 - 49	22 - 36	27 - 41	21.8 - 25.8	37 - 43	26 - 40	20.7 - 29.3
BW [%]	85	47	47	8.3	90	20.3	50	42	17	15	43	35
Conv. Gain [dB]	6	4	14	5	-10.2	-1.6	21	19.8	-4.2	0.9	-4	-8.8
P_{sat} [dBm]	5.7	3.4	13.0	5.0	-5.2	-1.6	11.9	8.0	0	2.0	5.0	-8.8
Peak η [%]	17.0	8.9	22.9	9.9	2.7	16.	27.4	18.0	16.6	2.1	2.0	1.40
Fund. Rejection [dB]	>40	/	>35	44	33	>25	32	26	39	6	14	>38
P_{DC}/V_{SUP} [mW/V]	21 / 1.5	25 / 1.5	87 / 2.5	31 / -	11 / 1	20 / 1.2	43.1 / 2.5	32 / 1.6, 2	6 / 1.2	86 / 2	66 / 2	9.6 / 1.2
Area [mm^2]	0.30	0.30	0.50	0.47	0.32	0.63	0.48	0.34	0.45	0.72	0.56	0.46

2.3 D-Band Frequency Doubler

Considering the potential for wide bandwidth with enhanced conversion gain, this section investigates the implementation of the proposed architecture in D-band. With the operation frequency above 100 GHz, pushed close to the technology limit (f_{max}), the major challenge is how to manage the intrinsic phase shift introduced by device parasitic and interconnections of a non-negligible length compared to the signal wavelength. A circuit topology is presented and implemented in a 55 nm BiCMOS technology. From experimental results, the chip delivers a peak output power of 6.5 dBm at 148 GHz with 7.4 % power conversion efficiency and 8 dB of conversion gain. The -3dB bandwidth is from 125 GHz to 170 GHz and output power remains greater than 0 dBm over the full D-band, from 110 GHz to 170 GHz.

2.3.1 Circuit Description and Implementation

The schematic of the proposed frequency doubler is shown in Fig. 2.20. HBTs $Q_{1,2}$ with size of 10 µm x 0.2 µm operate as transconductors converting the differential input voltage into a differential current $i_{IN} = i_{I,P} - i_{I,N}$. The input signal, single ended for measurement purposes, is converted to differential with an on-chip balun realized with a pair of coupled windings. The mixer switching quad is made of HBTs Q_3-Q_6, with drawn area of 6 µm x 0.2 µm. The parasitic capacitance at the output of the switching quad is resonated by inductors L_p, while a Marchand balun provides differential to single ended conversion and scales the 50 Ω off-chip termination to a 80 Ω differential load resistance for the mixer, optimal to maximize the output power. The circuit is supplied with a V_{CC} of 2 V and draws a DC current $I_{CC} = 30$ mA when driven into saturation, at an input power of 0 dBm. As discussed in the previous section, the average (DC component) of the differential output current ($i_{O,P} - i_{O,N}$) is nulled by a low-frequency feedback loop, drawn in grey in Fig. 2.20, which sets a differential bias voltage (V_{OS}) to the base of Q_3-Q_6, reducing the switching-quad duty-cycle. The differential DC component is sensed by resistors $R_{sense} = 5.5\ \Omega$ in series with inductors L_p. To not impair the quality factor of the load resonator, and avoid performance penalty, R_{sense} are shunted by capacitors $C_{big} = 1.5$ pF., large enough to be considered a short circuit in D-band. The error voltage across the sense resistors is amplified by a fully differential OTA. The output voltage of the OTA, V_{OS}, biases the bases of the switching quad via resistors $R_{big} = 1\ k\Omega$. The OTA is made of two gain stages allowing to reach a low frequency loop gain of 40 dB. The stability is ensured by Miller compensation which also limits the loop bandwidth to 200 MHz. The OTA draws 250 µA from the 2 V supply. The overall power consumption of the low frequency biasing loop is 3 mW (500 µW consumed by the OTA and 2.5 mW due to the 80 mV DC drop across R_{sense}) and represents only 5 % of the overall doubler power consumption.

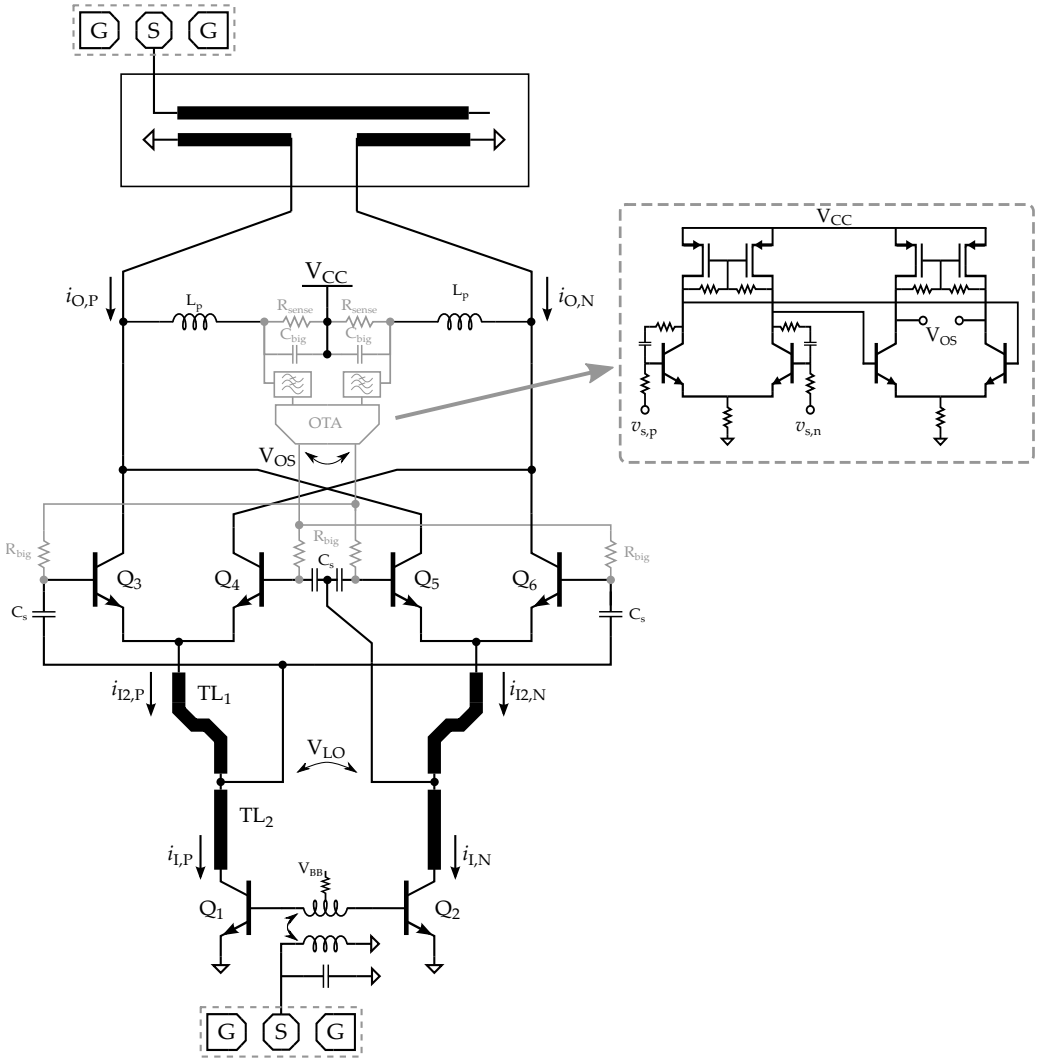


Figure 2.20: Schematic of the proposed frequency doubler.

For maximum 2nd harmonic conversion gain, the current entering the common emitter node of the switching quad ($i_{I2,P}$ - $i_{I2,P}$) must be in phase with the voltage driving the base of Q_3-Q_6 (V_{LO} in Fig. 2.20). At operation frequency far below the transistors cut-off frequency, as in the previous section, this condition is achieved by feeding the base of Q_3-Q_6 with the same voltage that drives the common emitter transconductors, Q_1, Q_2. As frequency approaches the technology f_t/f_{max}, this straightforward implementation is no longer viable, because of the non-negligible phase shift introduced by transistors parasitic and the delay of interconnections. As an example, the extrinsic HBTs base resistance, r_{bb}, forms a low-pass filter with the base-to-emitter capacitance, c_π, with an associated pole at about 140 GHz in the adopted technology. With a 75 GHz frequency of the input signal, the pole delays the effective voltage at the internal base of Q_3-Q_6 by roughly 30°. Moreover, while at low frequency the common-emitter transconductors are connected directly to the switching

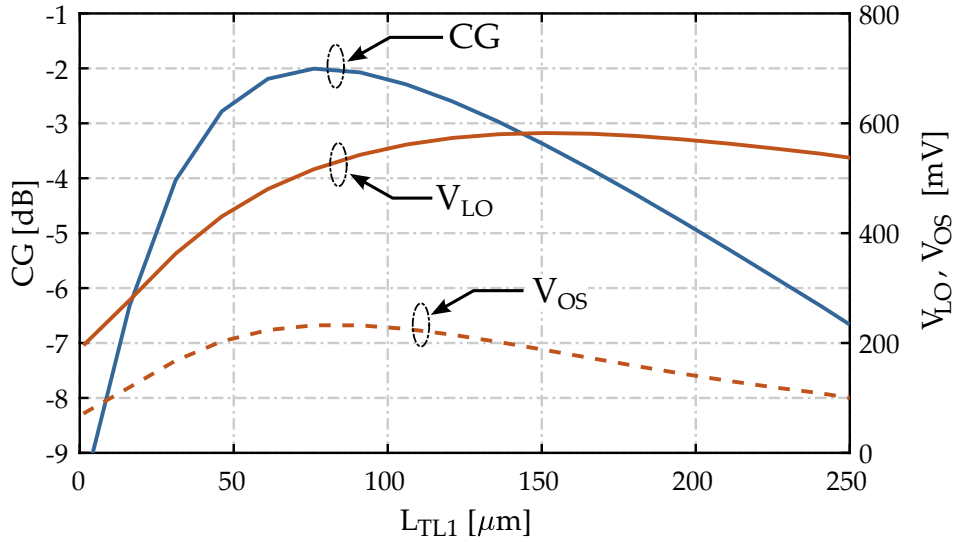


Figure 2.21: Frequency doubler conversion gain versus TL_1 length.

quad, the output resistance of Q_1, Q_2 at high frequency is drastically reduced, suggesting the introduction of an interstage matching network to rise the signal injection into the switching quad and increase the conversion gain. Looking again at Fig. 2.20, in the proposed frequency doubler the current provided by Q_1, Q_2 is injected into the switching quad through a transmission line (TL_1+TL_2) and the voltage V_{LO} that drives the base of Q_3-Q_6 is extracted from an intermediate tap. The first section of the line, TL_1, has a dual purpose: first, together with the stray capacitances of Q_3-Q_6, TL_1 provides step-up transformation of the impedance at the emitters of the switching quad, rising the amplitude of the voltage V_{LO} thus leading to a better current commutation of the switching quad. Second, TL_1 compensates the phase shift introduced by parasitics of Q_3-Q_6 by introducing a delay between the current which is finally entering into the switching quad and V_{LO}. To gain insight, Fig. 2.21 plots the current conversion gain $\left(CG = \frac{(i_{O,P}-i_{O,N})|_{2fin}}{i_{I2,P}-i_{I2,N}}\right)$, the amplitude of V_{LO} and the bias voltage produced by the OTA, V_{OS}, versus the length of TL_1 (L_{TL1}) when the multiplier is driven at 0 dBm input power. The amplitude of V_{LO} rises with the length of TL_1, reaching the maximum of 600 mV for $L_{TL1} = 150$ µm. On the other hand, the CG peaks to -2 dB at $L_{TL1} = 75$ µm, when the phase delay is optimally compensated, despite a V_{LO} slightly below its maximum. The bias voltage V_{OS} is also maximized for $L_{TL1} = 75$ µm, confirming that at this length of TL_1 the duty-cycle of the switching quad is minimized. TL_2 provides conjugate matching to the output impedance of Q_1, Q_2 further increasing the conversion gain. Fig. 2.22 plots the same quantities of Fig. 2.21 versus the length of TL_2 (L_{TL2}). V_{LO} rises close to 1 V and the $\left(CG = \frac{(i_{O,P}-i_{O,N})|_{2fin}}{i_{I,P}-i_{I,N}}\right)$ increases from -2 dB to roughly 0 dB at $L_{TL2} = 300$ µm. Tlines TL_1 and TL_2 are realized as a shielded coplanar structure with the signal in the topmost metal (M9) and the coplanar ground on the second topmost metal (M8). The characteristic impedance is

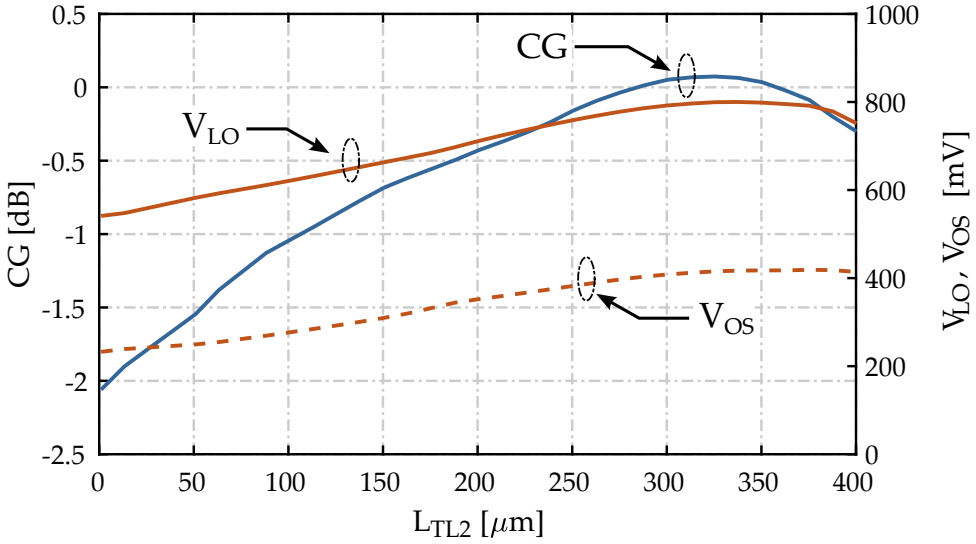
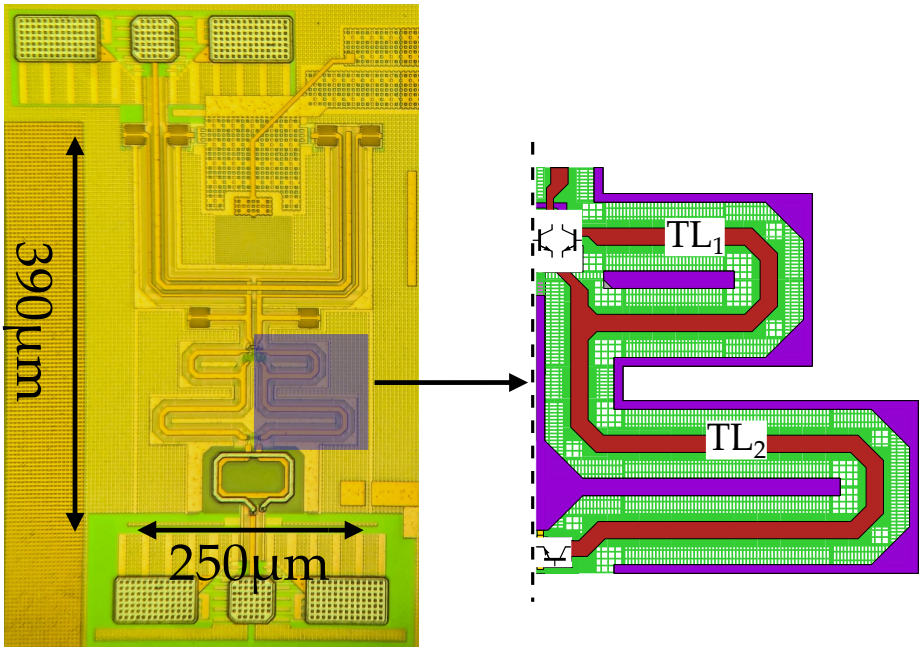


Figure 2.22: Frequency doubler conversion gain versus TL_2 length.

65 Ω with a quality factor ≈ 25. TL_1 and TL_2 are also easily laid without additional interconnections that would add parasitic elements in D-band.
The frequency doubler is realized in STM BiCMOS 55 nm technology. The chip photograph is reported in Fig. 2.23a, with core area 390 x 250 μm^2 excluding GSG pads. Not considering input and output baluns, only required for measurements, the area of the frequency doubler is 200 x 140 μm^2. The layout of half of the core is highlighted in Fig. 2.23b. TL_2 is folded on top of Q_1,Q_2 while TL_1 is wrapped around the switching quad, allowing a straight connection to the base and emitter terminals of Q_3-Q_6.



(a) (b)

Figure 2.23: Photograph of the realized frequency doubler.

2.3.2 Experimental Results

The chip is measured with direct die probing. The input signal is provided by an Agilent E8257D signal generator to cover the 50 - 67 GHz band and with an OML N5256BW12 frequency extension module for the 67 - 85 GHz band. Output power at twice the input frequency is measured with an ELVA-1 DPM-06 D-band power meter, while the fundamental leakage component is characterized with harmonic mixers and a PXA N9030A spectrum analyzer.
Fig. 2.24 shows the measured and simulated output power, P_{sat}, and collector efficiency ($\eta = P_{sat}/P_{DC}$). P_{sat} peaks to 6.5 dBm at 148 GHz and remains within -3 dB from 125 GHz to at least 170 GHz, the upper limit of the measurement setup, corresponding to a fractional bandwidth larger than of 31%. P_{sat} is above 0 dBm over the full D-band [110 - 170] GHz. Measurements are well aligned with simulations, which predict a 3 dB bandwidth of [125 - 175] GHz and a remarkable $P_{sat} > 0$ dBm bandwidth [110 - 200] GHz, corresponding to a 60% fractional bandwidth.
Fig. 2.25 shows the 2nd harmonic conversion gain (CG), η and output power (P_{out}) at input frequency of 150 GHz versus the input power (P_{in}). The CG peaks to 8.5 dB at P_{in} = -4 dBm. With $P_{in} = 0$ dBm, used for the measurements in Fig. 2.24, the conversion gain penalty is <1 dB.

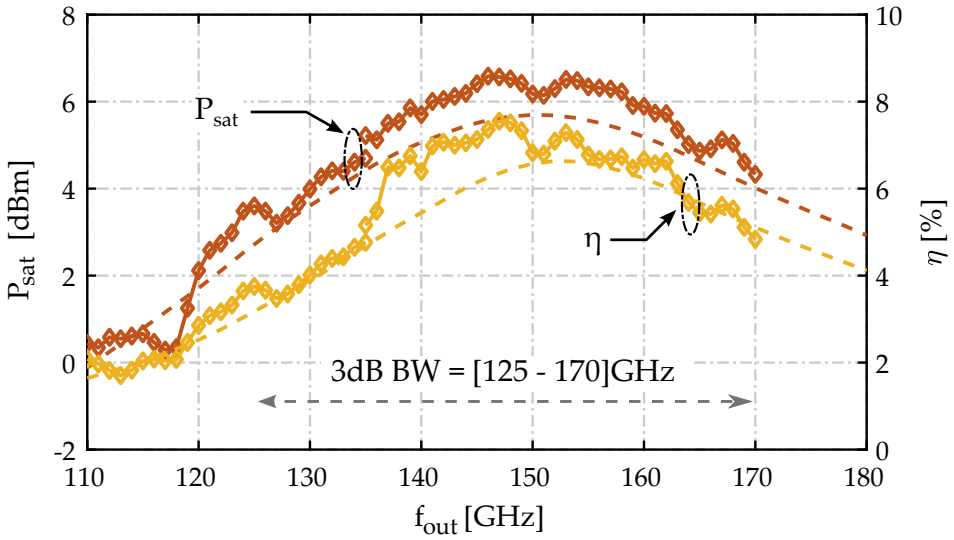


Figure 2.24: Measured (solid) and simulated (dashed) output saturated power (P_{sat}), and collector efficiency (η) vs frequency.

The fundamental rejection of the input signal is measured at $P_{in} = 0$ dBm. The unavoidable coupling between input and output probes has been characterized and de-embedded from the measurement. Results are reported in Fig. 2.26, showing a fundamental rejection above 40 dB over the entire bandwidth. Figure 2.27 shows the phase noise profile at the doubler output, compared to the one of the input source, as well as the expected phase noise degradation of 6 dB. The higher noise floor at frequency offsets above 1 MHz may be limited

by the D-band downconverter in the measurement setup.
The measured results are finally summarized in Table 2.2 and compared against previously reported frequency doublers operating in a similar frequency range. The implemented frequency doubler displays high P_{sat} and CG simultaneously and the highest rejection of the fundamental signal. The -3 dB fractional bandwidth of 31% is also the largest reported in a silicon-based technology. [36], in a compound semiconductor technology, demonstrates a wider bandwidth but with significantly lower P_{sat} and a high conversion loss.

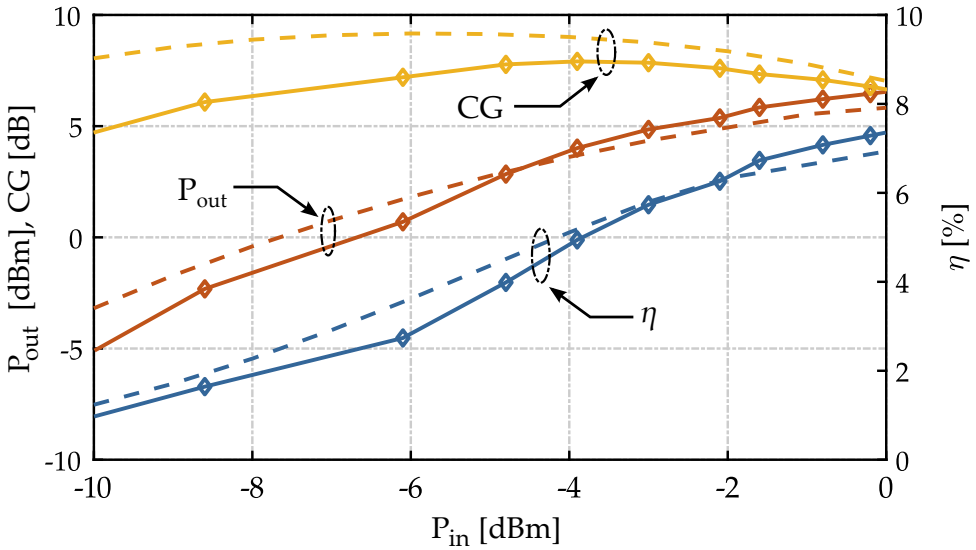


Figure 2.25: Measured output power (P_{out}), Conversion Gain (CG) and collector efficiency (η) vs input power P_{in} @ $f_{out} = 150$ GHz.

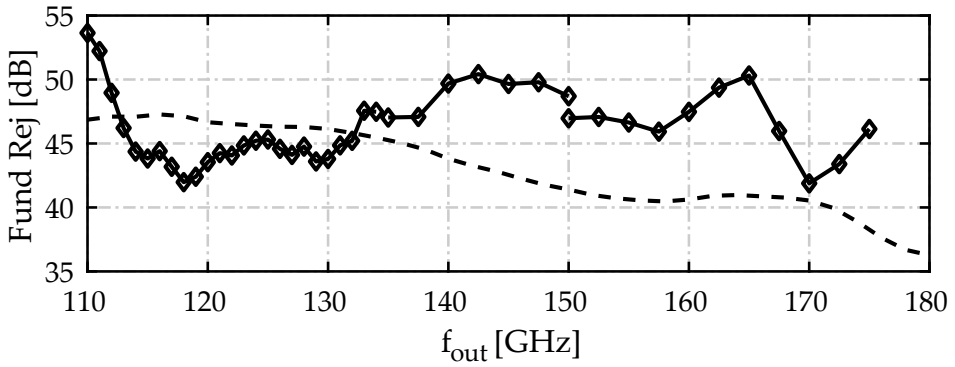


Figure 2.26: Measured (solid) and post-layout simulated (dashed) fundamental harmonic rejection vs frequency.

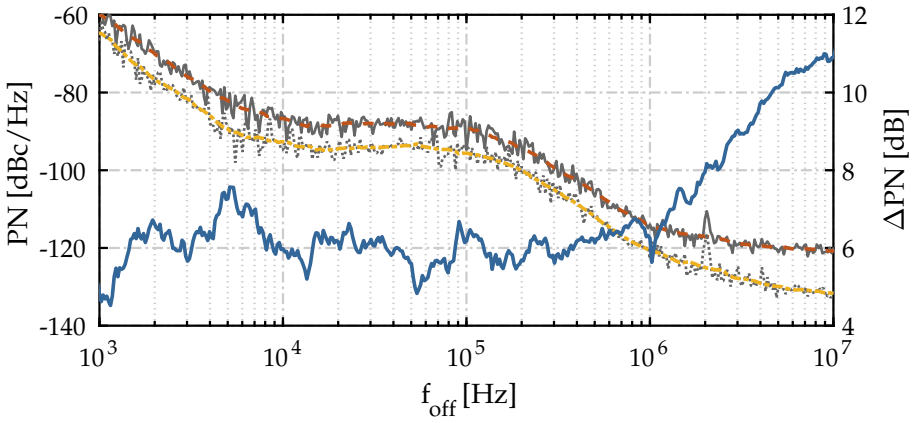


Figure 2.27: Proposed solution - Measured phase noise of the frequency doubler @ $f_{out} = 150\,GHz$ vs measured phase noise of the input source.

Table 2.2: Performance summary and comparison table.

	This Work	[14]	[37]	[38]	[39]	[40]	[41]	[42]	[36]
Technology	55 nm SiGe	55 nm SiGe	0.13 µm SiGe	90 nm SiGe	0.13 µm SiGe	22 nm FDSOI	55 nm CMOS	0.1 µm GaAs	InGaAs
Architecture	Reduced-δ Gilbert-cell	Push-Push	Push-Push	Push-Push	Push-Push	Push-Push	Push-Push	Common Source	Push-Push
Frequency [GHz]	125 - 170	116 - 144	138 - 170	128 - 140	166 - 182	125 - 145	112 - 125	110 - 130	100 - 208
BW [%]	31	22	21	9	9	15	11	17	75
P_{sat} [dBm]	6.5	4.3	5.6	9.4	4.5	4.1	7.8	5	1.4
CG@P_{sat} [dB]	8	9.3	4.9	-6	5	-7.6	-2.2	2	-12.6
η [%]	7.4	7.2	10.1	12.1	8.4	10.4	6.8	4.9	9.6
PAE@P_{sat} [%]	6.3	6.4	6.8	<0	5.8	<0	<0	1.8	<0
Fund. Rejection [dB]	>40	>32	37	20	-	15	20	25	-
P_{DC}/V_{CC} [mW/V]	60 / 2	37.4 / 2	36 / 1.5	72 / 1.9	33.5 / 2.5	24.7 / 0.8	88 / 1.2	65 / 1	14.4 / 0.8

2.4 Chapter Summary

This chapter presented a simple technique to enhance the overall performance of frequency doublers based on Gilbert-cell mixers. The conversion gain is improved by applying a DC offset to the switching-quad transistors, such that the duty-cycle is reduced and the output current assumes an almost square-wave shape at twice the input frequency. The DC offset is self-adjusted by a low-frequency feedback loop to maintain optimal performance against input power and PVT variations. Compared to the conventional architecture made of a Gilbert-cell driven by quadrature signals, the proposed technique yields wider bandwidth (not requiring a 90° phase shifter), enhanced gain and robustness to impairments.
The claimed advantages are supported by simulations and verified experimentally on prototypes of the conventional quadrature-driven mixer and of the proposed architecture in the same technology for K-band operation. Compared to previously reported frequency doublers, the presented solution achieved state-of the-art output power and efficiency, at low supply voltage, with a remarkable advantage on the operation bandwidth.
The same operating principle is proven in D-band by experiments on a test chip in 55 nm SiGe BiCMOS. A transmission line network that compensates the phase shift introduced by transistors parasitic is proposed to generate the LO signal and drive the mixer optimally. Compared to previous works, the doubler displays the widest operation bandwidth and the highest suppression of the fundamental component, with high P_{sat} and conversion gain, simultaneously.

3 Phase Shifters

As seen in the Introduction chapter, active phased-arrays need to coherently combine the transmitted and received signals at each antenna element in order to perform beamforming and beam steering. Even though the ideal solution would involve true time delay, we have seen that this is only possible in digital or hybrid beamforming systems, as the required delay range increases with the array size. On the other hand, at D-band, although the transceivers may support wide frequency range, the fractional channel (instantaneous) bandwidth is, in most of the applications, limited, relaxing the issues of beam squinting [4] and inter-symbol interference [5]. Therefore, phase shifter (PS) can be used in place of true time delay in fully analog beamforming solutions with little penalty.

The programmable phase shifter remains a crucial component: on the transmitter side it precedes the power amplifier, and achieving a high output power at 1 dB gain compression (OP_{1dB}) is desirable to relax PA requirements and improve the power efficiency. Conversely, in the receiver, the PS follows the low-noise amplifier, and both low noise and high linearity are desirable not to compromise the dynamic range. A relatively high gain compression point is necessary in radar sensors, to make the front-end resilient against close-by reflections, but also in wireless communications to support spectrally efficient high-order modulations [43]. Phase shifters can be implemented with passive circuits, based on programmable filters [44], reflective type structures [45] or switched delay paths [46], [47], offering high linearity at the expense of limited phase resolution, high losses, bandwidth limitation and large area occupation. Conversely, active phase shifters, built around the vector interpolation principle [48]–[55], can easily cover the 360° circle with high phase resolution and a compact area, but suffer from limited linearity. The latter can be improved by increasing power consumption, but penalizing the system efficiency. The linearity issue arises from the need for variable gain amplifiers (VGAs) which are required to operate across a relatively high dynamic range of gain control.

This first section of this chapter focuses on the vector interpolation phase shifter, investigating the impact of VGA impairments on the vector-interpolated

output, with focus on the AM-AM and AM-PM distortions. Common techniques to implement VGAs are then studied and compared, identifying the preferable choice to maximize the phase shifter linearity. A D-band phase shifter is designed and implemented in the STMicroelectronics 55 nm BiCMOS technology. The chip displays 3.5 dB gain across the [130 - 175] GHz band. The phase shift is programmable in 10° step with RMS phase and amplitude errors across the full frequency range within 5° and 0.8 dB. The VGAs bias currents and operation mode are controlled by a simple on-chip logic circuit. The latter is used to validate the theoretical results by testing the phase shifter linearity in the different VGA operation modes considered in the analysis. Using the preferred VGA configuration, the output power at 1 dB gain compression (OP_{1dB}) at center frequency is above 1.8 dBm with AM-PM <10° at 64 mW power consumption from 2 V supply. Experimental results compare favorably against previous works in the same band and with similar technology, particularly considering the linearity and power efficiency.

The second section proposes a digital phase shifter, where elementary passive networks presented in [44] are combined in a way to minimize power loss and to preserve a broadband response. The input signal is split in two quadrature paths, later recombined by amplifiers to compensate for the networks losses. The amplitude of the output signal is controlled by adjusting independently the relative phase shift of the I/Q paths, similarly to the working principle of outphasing amplifiers [56], thus avoiding the need of VGAs. This choice allows the subsequent amplifiers to operate at constant-gain and at the optimal biasing condition for maximum linearity, leading to constant and high OP_{1dB}. The I/Q relative phase shift is also exploited for the correction of the quadrature and phase-inversion errors through proper calibrations. Experiments on a 55 nm SiGe BiCMOS test chip prove -2.3 dB gain and a broadband response from 125 GHz to 170 GHz. The phase-control resolution is 9° and, with calibrations applied, the RMS phase and amplitude errors are limited to 5° and 0.8 dB, respectively, across the full operation bandwidth. The OP_{1dB} is greater than 2 dBm over 0°-360° phase settings and over the entire frequency range with 31 mW power consumption from 2 V supply.

3.1 Vector-interpolation phase shifter

3.1.1 Operation principle and AM-AM and AM-PM Distortion

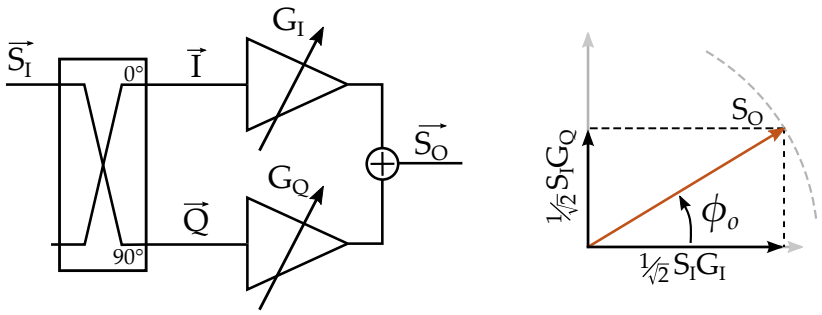


Figure 3.1: Vector-interpolation phase shifter block diagram.

The simplified block diagram of a vector-interpolation phase shifter is depicted in Fig. 3.1. As implied by its name, the output vector, $\vec{S_O}$, is generated by combining two orthogonal vectors, $\vec{I}$ and $\vec{Q}$, suitably weighted by two independent amplifiers with variable gains G_I, G_Q. The $\vec{I}$ and $\vec{Q}$ vectors are obtained by feeding a quadrature hybrid coupler with the input signal, $\vec{S_I}$, assumed with zero phase as reference. Through straightforward trigonometric analysis, the magnitude and phase of the gain, $\vec{G_O} = \vec{S_O}/\vec{S_I}$, can be determined as follows:

$$|\vec{G_O}| = \frac{1}{\sqrt{2}}\sqrt{G_I^2 + G_Q^2} \tag{3.1}$$

$$\angle\vec{G_O} = \phi_o = \tan^{-1}\frac{G_Q}{G_I} \tag{3.2}$$

where the $1/\sqrt{2}$ accounts for the 3-dB split of the hybrid coupler.
If G_I and G_Q span positive and negative values within a maximum range (G_{MAX}), $G_{I,Q} = \alpha_{I,Q}\, G_{MAX}$ with $\alpha_{I,Q} \in [-1, +1]$, by controlling α_I and α_Q such that (3.1) is constant, it is possible to sweep the phase shift of the output signal, ϕ_o, in the 0° - 360° range with constant amplitude. It is worth noticing that the minimum gain ($\Delta\alpha$) sets the minimum achievable phase step close to a cardinal axis. In fact, looking at Fig. 3.1, the minimum phase step e.g. from 0° (close to the I axis), is achieved with $G_I \approx G_{MAX}$ and $G_Q = \Delta\alpha\, G_{MAX} = G_{MIN}$, thus $\Delta\phi_o = \tan^{-1}|\Delta\alpha|$. Based on this observation, a phase step consistently below 10° requires $\Delta\alpha < 0.18$ (or, equivalently, a gain control range of the VGA $20\log(G_{MAX}/G_{MIN}) > 15$ dB).
The large-signal amplitude and phase distortion of the VGAs (AM-AM_{VGA}, AM-PM_{VGA}) leads to amplitude and phase distortion on the phase shifter (AM-AM_{PS} and AM-PM_{PS}). The impact depends on the phase of the output vector. The two extreme cases are when the output vector is in the middle of a quadrant or close to a cardinal axis. The vector diagrams representative of the

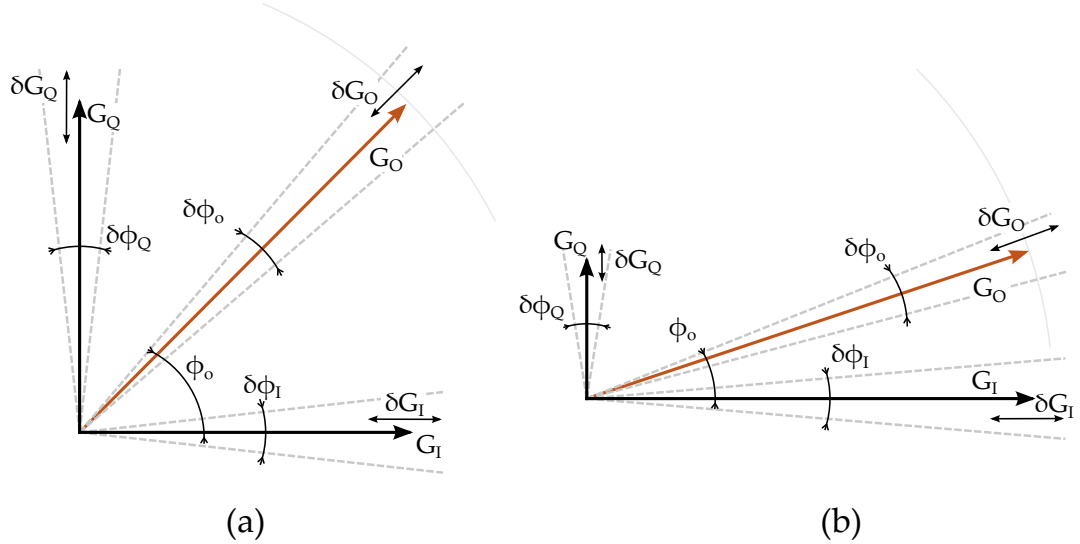


Figure 3.2: Vector interpolation in the case of $\phi_o = 45°$ (a) and small angle $\phi_o \approx \Delta\phi_o$ (b).

two conditions are depicted in Fig. 3.2. The small-signal gain is the sum of the two quadrature vectors, $\vec{G_O} = \frac{1}{\sqrt{2}}(G_I + jG_Q)$. Accounting for the large-signal distortions of the VGAs, the gain can be expressed in the general form:

$$\vec{G_O} = \frac{1}{\sqrt{2}}(1+\delta G_I)G_I e^{j\delta\phi_I} + j\frac{1}{\sqrt{2}}(1+\delta G_Q)G_Q e^{j\delta\phi_Q} \tag{3.3}$$

where $\delta G_{I,Q} \triangleq \delta G_{I,Q}(S_I)$ and $\delta\phi_{I,Q} \triangleq \delta\phi_{I,Q}(S_I)$ represent the variation of the gain magnitude (AM-AM$_{VGA}$) and phase (AM-PM$_{VGA}$), of the two VGAs with respect to the input signal magnitude $S_I \triangleq |\vec{S_I}|$.
Let us focus first on the diagram in Fig. 3.2a, where the phase shifter introduces $\phi_o = 45°$ (the behavior is the same at the center of each quadrant, i.e. $\phi_o = 45° + n \cdot 90°$, n integer). In this case, the two VGAs are operated at the same gain, 3 dB below the maximum ($G_I = G_Q = G_{MAX}/\sqrt{2}$) and thus introduce equal distortions: $\delta G_I = \delta G_Q = \delta G|_{G_{MAX\text{-}3\,dB}}$ and $\delta\phi_I = \delta\phi_Q = \delta\phi|_{G_{MAX\text{-}3\,dB}}$. Eq. (3.3) can thus be simplified to:

$$\vec{G_O} = \frac{1}{\sqrt{2}}(1+\delta G|_{G_{MAX-3dB}})G_{MAX}\cdot e^{j\left(\frac{\pi}{4}+\delta\phi|_{G_{MAX-3dB}}\right)} \tag{3.4}$$

that is:

$$\begin{aligned} \text{AM–AM}_{PS} &= \delta G|_{G_{MAX-3dB}} \\ \text{AM–PM}_{PS} &= \delta\phi|_{G_{MAX-3dB}} \end{aligned} \tag{3.5}$$

Eq. (3.5) shows that the output amplitude and phase distortion is one-to-one exposed to the distortion of a single VGA. In other words, besides the 3-dB power split of the input quadrature coupler, the input power at 1 dB gain variation (IP$_{1dB}$) of the phase shifter is the same of a VGA, and the same

holds for the AM-PM. The behavior changes when the two VGAs are operated at different gain, and the limit case is when the output vector is steered towards one of the four cardinal axes. Fig. 3.2b considers a minimum positive phase step from 0°, $\phi_o = \Delta\phi_o$ with the I-path VGA roughly at maximum gain, $G_I \approx G_{MAX}$, while the other is at the minimum gain $G_Q = G_{MIN}$. In this situation, the magnitude of the output vector is mostly determined by G_I solely, and thus AM-AM$_{PS} \approx \delta G_I|_{G_{MAX}}$. For the same reason, the AM-PM of the I-path VGA, $\delta\phi_I|_{G_{MAX}}$, is also directly transferred to the phase of the output vector, ϕ_o. But the latter is equal to the ratio between the magnitudes the of two quadrature vectors ($\phi_o = \tan^{-1}(G_Q/G_I) \approx G_Q/G_I$) and thus it is also sensitive to the VGAs AM-AM distortions.

Starting from (3.3), we can derive a simplified expression for ϕ_o. First, assuming small AM-AM$_{VGA}$ and AM-PM$_{VGA}$ ($\delta G_I, \delta G_Q, \delta\phi_I, \delta\phi_Q \ll 1$), (3.3) can be approximated as:

$$\vec{G_O} = \frac{1}{\sqrt{2}} G_I (1 + \delta G_I + j\,\delta\phi_I) + j\frac{1}{\sqrt{2}} G_Q (1 + \delta G_Q + \delta\phi_Q) \tag{3.6}$$

ϕ_o is the phase of (3.6). With $G_I = G_{MAX}$ and $G_Q = G_{MIN}$, $\phi_o = \Delta\phi_o \ll 1$ (i.e. $\tan^{-1}(\phi_o) \approx \phi_o$) and thus:

$$\phi_o \approx \frac{G_{MIN}}{G_{MAX}} \frac{1 + \delta G_Q + \frac{G_{MAX}}{G_{MIN}}\delta\phi_I}{1 + \delta G_I - \frac{G_{MIN}}{G_{MAX}}\delta\phi_Q} \tag{3.7}$$

$$\phi_o \approx \frac{G_{MIN}}{G_{MAX}} \frac{1 + \delta G_Q + \frac{G_{MAX}}{G_{MIN}}\delta\phi_I}{1 + \delta G_I}$$

where $\frac{G_{MIN}}{G_{MAX}} \cdot \delta\phi_Q$ is neglected because $\frac{G_{MIN}}{G_{MAX}} \ll 1$.

With small δG_I, $1/(1+\delta G_I) \approx (1-\delta G_I)$, thus (3.7) can be further approximated as:

$$\phi_o \approx \frac{G_{MIN}}{G_{MAX}} \left(1 + \delta G_Q + \frac{G_{MAX}}{G_{MIN}}\delta\phi_I\right)(1 - \delta G_I) \tag{3.8}$$

By further developing and removing second order terms:

$$\phi_o \approx \frac{G_{MIN}}{G_{MAX}} + \frac{G_{MIN}}{G_{MAX}}\delta G_Q - \frac{G_{MIN}}{G_{MAX}}\delta G_I + \delta\phi_I \tag{3.9}$$

By replacing $\delta G_Q = \delta G_Q|_{G_{MIN}}$, $\delta G_I = \delta\, G_I|_{G_{MAX}}$, $\delta\phi_I = \delta\phi_I|_{G_{MAX}}$ we obtain:

$$\phi_o \approx \frac{G_{MIN}}{G_{MAX}} + \frac{G_{MIN}}{G_{MAX}}(\delta G_Q|_{G_{MIN}} - \delta G_I|_{G_{MAX}}) + \delta\phi_I|_{G_{MAX}} \tag{3.10}$$

The AM-AM distortion of a VGA typically degrades when the gain is reduced (as it will be shown in the next section) thus (3.10) can be further simplified considering $\delta G_Q|_{G_{MIN}}/G_Q \gg \delta G_I|_{G_{MAX}}/G_I$:

$$\phi_o \approx \frac{G_{MIN}}{G_{MAX}} + \frac{G_{MIN}}{G_{MAX}}\delta G_Q|_{G_{MIN}} + \delta\phi_I|_{G_{MAX}} \tag{3.11}$$

Extending (3.11) to any small phase step (positive or negative) at integer multiples of 90°, $\phi_o = \pm\Delta\phi_o + n \cdot 90°$ (n integer), where the role of I and Q VGAs may be exchanged, the phase shifter amplitude and phase distortion are finally found:

$$\text{AM–AM}_{PS} \approx \delta G|_{G_{MAX}} \tag{3.12}$$

$$\text{AM–PM}_{PS} \approx \pm\frac{G_{MIN}}{G_{MAX}}\delta G|_{G_{MIN}} + \delta\phi|_{G_{MAX}}$$

The result shows that, while the amplitude distortion is the same of the VGA at the maximum gain, the phase is impaired by the AM-PM$_{VGA}$ of the VGA at maximum gain and by the AM-AM$_{VGA}$ of the VGA at minimum gain.

To sum up, the two VGAs must support a relatively high dynamic range of gain regulation, $20\log(G_{MAX}/G_{MIN}) \approx 15$ dB, to ensure a consistent phase resolution of ≈10°. Moreover, to limit the phase shifter distortion, they should feature low AM-AM and AM-PM at $G_{MAX\text{-}3dB}$, according to eqq. (3.5), and, according to eqq. (3.12), low AM-AM and AM-PM at G_{MAX} and low AM-AM at G_{MIN}.

3.1.2 Comparison of VGA Topologies

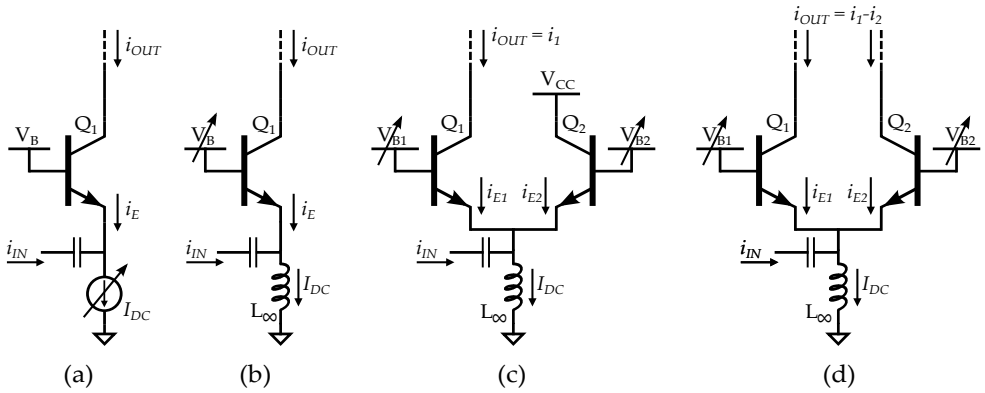


Figure 3.3: VGA configurations. Gain controlled by the bias current in a single HBT with a tail current source (a) and a tail inductor (b). VGA with current bleeding to V_{CC} (c) and VGA with current steering (d).

Different VGA options are now analyzed with focus on the amplitude and phase distortion. The core schematics are drawn in Fig. 3.3, all realized with HBTs in the common base (CB) configuration. The input current is i_{IN}, while the output current, i_{OUT}, will be injected into a load (not shown) $Z_L = R_L + jX_L$[1].

[1]Variation of the load or output impedance may cause distortion at large voltage swing, as in any kind of amplifier. In the analysis it is assumed that the load impedance and voltage headroom are selected properly to not be the limiting factors to the VGAs linearity.

In all the cases, the power gain, G_P, can be expressed as:

$$G_P = \frac{i_{OUT}^2 R_L}{i_{IN}^2 R_{IN}} = A_I^2 \frac{R_L}{R_{IN}} \tag{3.13}$$

where $A_I = i_{OUT}/i_{IN}$ is the current gain and R_{IN} is the real part of the impedance presented by the circuit to the input current i_{IN}. Drawn in Fig. 3.3a and Fig. 3.3b, the simplest VGA (referred to as VGA_{CB}) is made of a single device, Q_1, with gain regulated by the DC bias current. In Fig. 3.3a the quiescent current, I_{DC}, is set by a current source, while in Fig. 3.3b the emitter of Q_1 is DC grounded by an inductor and I_{DC} is regulated by the base voltage V_B. In both cases, neglecting the HBT base-emitter capacitance (which can be resonated out or absorbed by an input matching network), the current gain and input resistance are, as a first-order approximation, $A_I = 1$ and $R_{IN} = 1/g_m = v_T/I_{DC}$ (being g_m the transconductance of Q_1 and v_T the thermal voltage). At small signal ($i_{IN} \ll I_{DC}$), G_P of the amplifiers in Fig. 3.3a and 3.3b is the same, but the AM-AM distortion is completely different. With a tail current source (Fig. 3.3a), the DC current in Q_1 is forced to be constant, and when the input signal amplitude exceeds I_{DC} ($|i_{IN}| > I_{DC}$), Q_1 turns off for a fraction of the period, leaving the Class-A regime. This leads to an increase of the equivalent R_{IN} (defined in large signal as the ratio between the fundamental component of the input voltage and current) and, according to (3.13), causes a G_P compression.
With the circuit of Fig. 3.3b, the average current in L_∞ (hence in Q_1) can rise above the quiescent level, when $|i_{IN}| > I_{DC}$, due to current-clamping, a mechanism analyzed in [57] and exploited to improve the efficiency of CB power amplifiers. As a result of the DC current expansion with $|i_{IN}|$, the large-signal input resistance of the circuit in Fig. 3.3b decreases, leading to expansion of G_P, more pronounced when I_{DC} is decreased. The ongoing discussion is validated by the plots in Fig. 3.4, showing simulations of the two VGA_{CB} with the same Q_1 emitter area $A_e = 10\,x\,0.2\,\mu m^2$. Fig. 3.4a plots G_P for the circuit in Fig. 3.3a, normalized to its maximum (G_{MAX}), sweeping the input power (P_{IN}=$i_{IN\text{-}rms}^2 \cdot R_{IN}$). I_{DC} is reduced from 10 mA to ≈0.2 mA to attain the 15 dB gain reduction, as required by the analysis in Sec. 3.1.1. With increasing P_{IN}, G_P experiences compression, and the P_{IN} giving 1 dB AM-AM_{VGA} (IP_{1dB}) decreases when reducing I_{DC}. Looking at Fig. 3.4b, the gain of the VGA_{CB} of Fig. 3.3b expands, particularly when I_{DC} is reduced. Notably, thanks to the average current expansion in Q_1, the P_{IN} at 1 dB AM-AM_{VGA} distortion is also improved, compared to VGA_{CB} of Fig. 3.3a.
The root cause of AM-AM distortion (either compression or expansion) in the simple VGA_{CB} is that G_P is reduced by increasing R_{IN}, and the latter experiences a significant variation with the magnitude of i_{IN} at low I_{DC}.
The VGAs in Fig. 3.3c and Fig. 3.3d, referred to as VGA_{VCC} and VGA_{DIFF}, respectively, mitigate the issue by keeping I_{DC} constant, and thus presenting roughly constant R_{IN}, while changing G_P by regulating the current gain, A_I.

The operation of the two circuits is the same, but again with different AM-AM distortion. Q_1 and Q_2 share the same emitter node and implement a current divider for i_{IN}. In Fig. 3.3c, i_{OUT} is the current in Q_1, $\approx i_{E1}$, while the bleeding current in Q_2, i_{E2}, is wasted toward V_{CC}. In Fig. 3.3d, $i_{OUT} = i_{E1} - i_{E2}$. The quiescent currents in the two HBTs ($I_{DC\text{-}Q1}$, $I_{DC\text{-}Q2}$) and A_I are controlled by the bias voltages V_{B1} and V_{B2}. If $I_{DC\text{-}Q1}$ and $I_{DC\text{-}Q2}$ are regulated at constant sum ($I_{DC\text{-}Q1} + I_{DC\text{-}Q2} = I_{DC}$), R_{IN} remains roughly constant (as long as $i_{IN} < I_{DC}$). Assuming the ideal exponential I-V characteristic for Q_1, Q_2 and neglecting parasitics, the following relation holds:

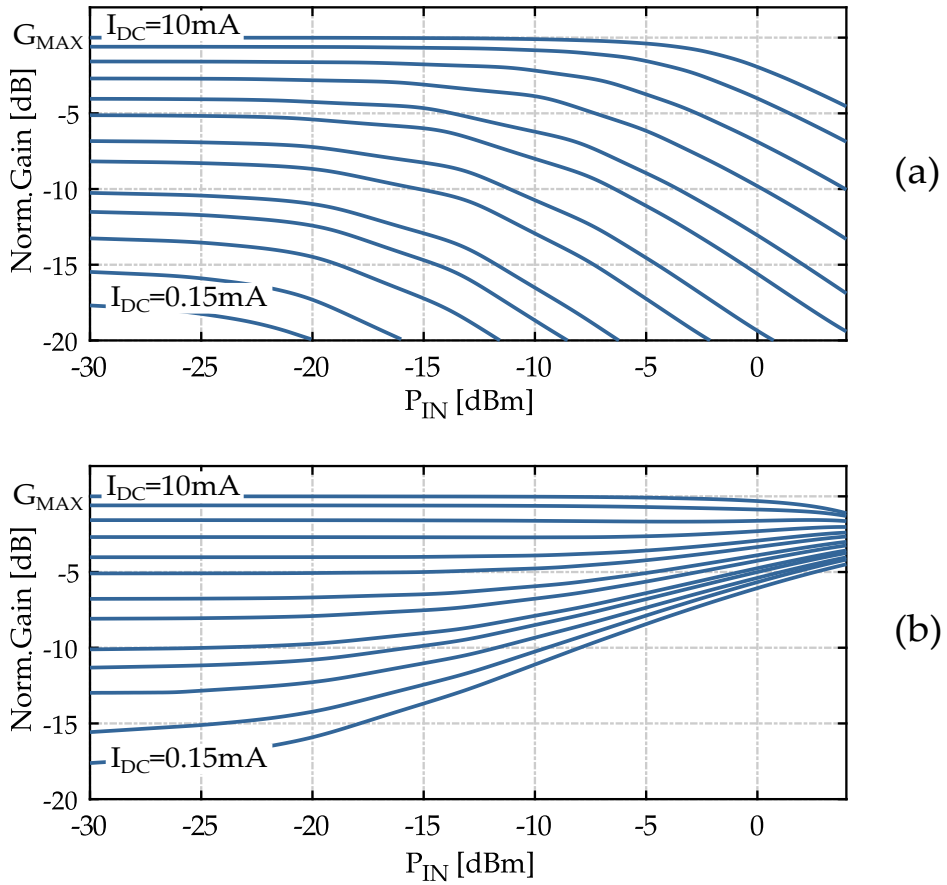


Figure 3.4: G_P curves, normalized to G_{MAX}, for the VGA_{CB} with tail current source (a) with tail inductor (b).

$$\frac{I_{DC-Q1}}{I_{DC}} = \frac{i_{E1}}{i_{IN}} = \frac{e^{V_{B1}/v_T}}{e^{V_{B1}/v_T} + e^{V_{B2}/v_T}} \qquad (3.14)$$
$$\frac{I_{DC-Q2}}{I_{DC}} = \frac{i_{E2}}{i_{IN}} = \frac{e^{V_{B2}/v_T}}{e^{V_{B1}/v_T} + e^{V_{B2}/v_T}}$$

The equations above prove that the ratios between signal currents and DC currents in each HBT are equal. As a result, the current gain for the VGA_{VCC} in Fig. 3.3c is:

$$A_I = \frac{I_{DC-Q1}}{I_{DC}} \qquad (3.15)$$

while for the VGA_{DIFF} in Fig. 3.3d:

$$A_I = \frac{I_{DC-Q1} - I_{DC-Q2}}{I_{DC}} \tag{3.16}$$

(3.15) and (3.16) show that A_I is solely dependent on the ratio of DC currents. Consequently, with R_{IN} constant, the two VGAs are ideally free of AM-AM distortion. This is confirmed by simulations, provided the HBT models are deliberately modified to remove the emitter parasitic resistance, r_e, not considered so far. With non-negligible r_e, (3.14) loses validity. In this case a large-signal analysis does not find a closed-form solution, but we can gain insight by considering the small-signal current gain. Let us first focus on the VGA_{VCC}. Straightforward circuit analysis leads to:

$$\frac{i_{E1}}{i_{IN}} = \frac{g_{m1} + g_{m1}g_{m2}r_e}{g_{m1} + g_{m2} + 2g_{m1}g_{m2}r_e} \neq \frac{I_{DC-Q1}}{I_{DC}} \tag{3.17}$$

with $g_{m1,2} = I_{DC1,2}/v_T$ the device transconductances, and r_e is the same for Q_1 and Q_2. Differently from the case of $r_e = 0$, (3.17) proves that the ratio between the signal currents, $A_I = i_{E1}/i_{IN}$, is no longer equal to the ratio of the DC currents, $\eta_{I\text{-}Q1} = I_{DC\text{-}Q1}/I_{DC}$.

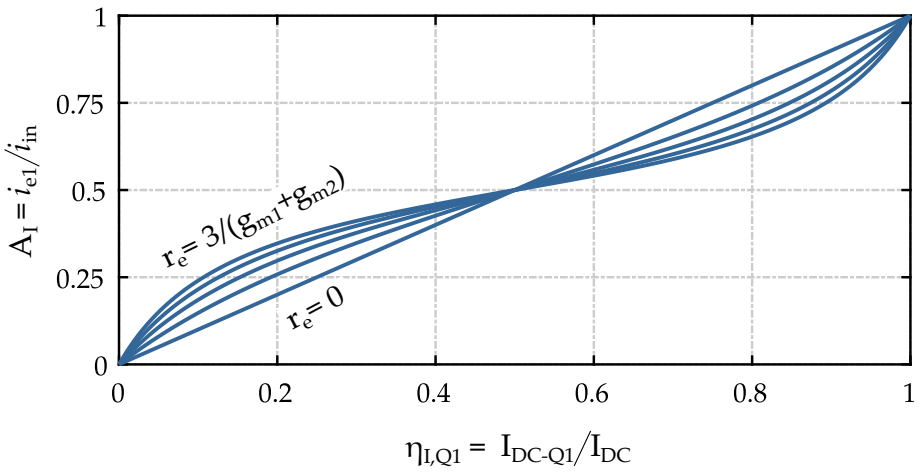


Figure 3.5: Small-signal current gain A_I for different r_e versus DC bias current steering, $\eta_{I\text{-}Q1}$.

Fig. 3.5 plots A_I against $\eta_{I\text{-}Q1}$ for different values of r_e. As r_e increases, the curve deviates from a straight-line, and it can be noted that, for any value of $I_{DC\text{-}Q1}/I_{DC}$, the signal current splits in favor of the HBT with the lowest DC current. It follows that the HBT with lower DC current expands faster than the other, which is then compressed. The behavior can be appreciated by looking at the simulation of the normalized G_P, against P_{IN}, for the VGA_{VCC}, plotted in Fig. 3.6a. The circuit is designed with equal HBTs ($A_e = 10\,x\,0.2\,\mu m^2$) and a total bias current $I_{DC} = 10\,mA$. $G_P = G_{MAX}$ is obtained when $I_{DC\text{-}Q1} = 10\,mA$ and $I_{DC\text{-}Q2} = 0$. To reduce G_P, $I_{DC\text{-}Q1}$ is decreased and $I_{DC\text{-}Q2}$ is increased. As long

as $I_{DC\text{-}Q1} > I_{DC\text{-}Q2}$, $i_{E1}/I_{DC\text{-}Q1} < i_{E2}/I_{DC\text{-}Q2}$ and when P_{IN} (hence i_{IN}) increases, Q_1 is compressed while Q_2 expands. Being $i_{OUT} = i_{E1}$, the current gain A_I and G_P show an AM-AM compression behavior, clearly visible in the topmost curves of the plot. When $I_{DC\text{-}Q1} = I_{DC\text{-}Q2}$, A_I is halved and G_P is reduced by 6 dB. In this case $i_{E1}/I_{DC\text{-}Q1} = i_{E2}/I_{DC\text{-}Q2}$ and G_P is ideally flat against P_{IN} (the slight G_P variation at very high P_{IN} is due to the HBTs pushed into the high-injection regime). To reduce G_P by more than 6 dB, $I_{DC\text{-}Q1}$ becomes lower than $I_{DC\text{-}Q2}$, leading to $i_{E1}/I_{DC\text{-}Q1} > i_{E2}/I_{DC\text{-}Q2}$. In this region the behavior of the two HBTs is flipped, i.e. Q_1 expands while Q_2 is compressed, leading to G_P expansion visible on the bottom curves.

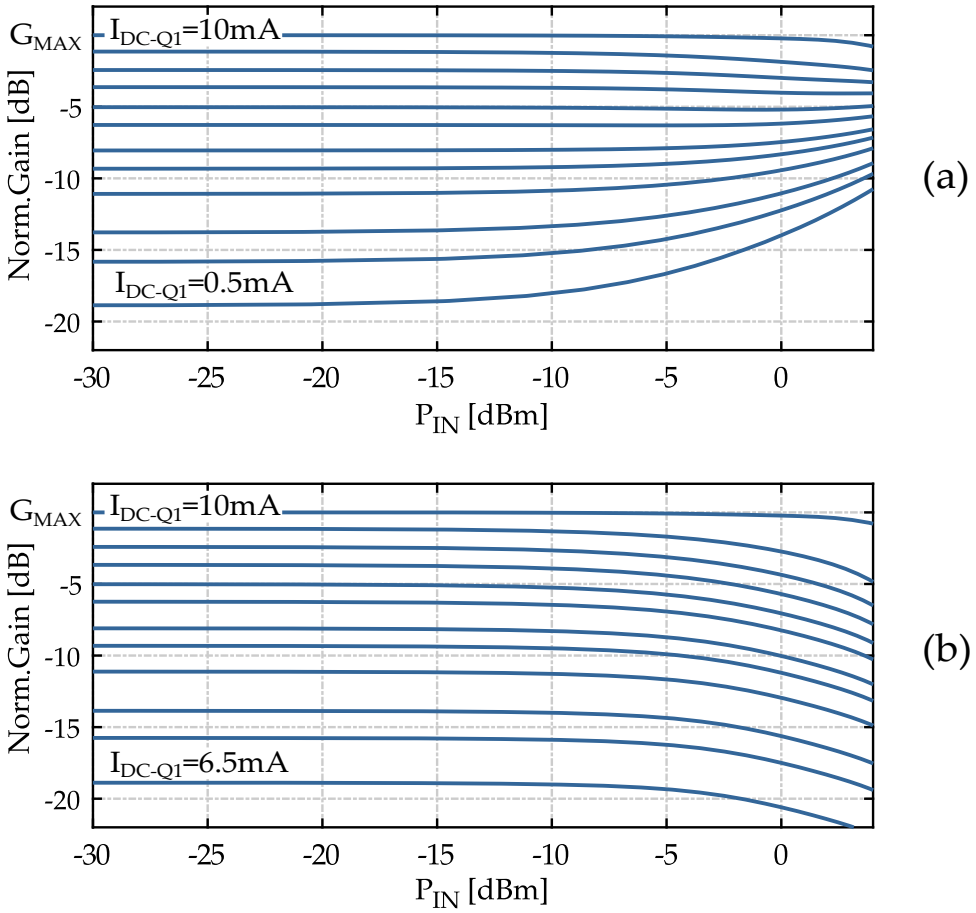


Figure 3.6: G_P curves for the VGA_{VCC} (a) and VGA_{DIFF} (b).

In the VGA_{DIFF} of Fig. 3.3d the behavior of Q_1, Q_2 is the same but with a different outcome. Being $i_{OUT} = i_{E1} - i_{E2}$, $A_I = 0$ (and $G_P = 0$) is obtained when the DC current is split equally between Q_1 and Q_2 (in this situation, G_P is reduced by 6 dB in the VGA_{VCC}). This means that for $0 < G_P \leqslant G_{MAX}$, $I_{DC\text{-}Q1} > I_{DC\text{-}Q2}$ and thus Q_1 always compresses while Q_2 expands.
With $i_{OUT} = i_{E1} - i_{E2}$, the overall VGA characteristics shows a compressing behavior, worsened by the simultaneous compression of i_{E1} and expansion of i_{E2}. Simulations in Fig. 3.6b confirm the analysis. At $G_P = G_{MAX}$, Q_2 is off and

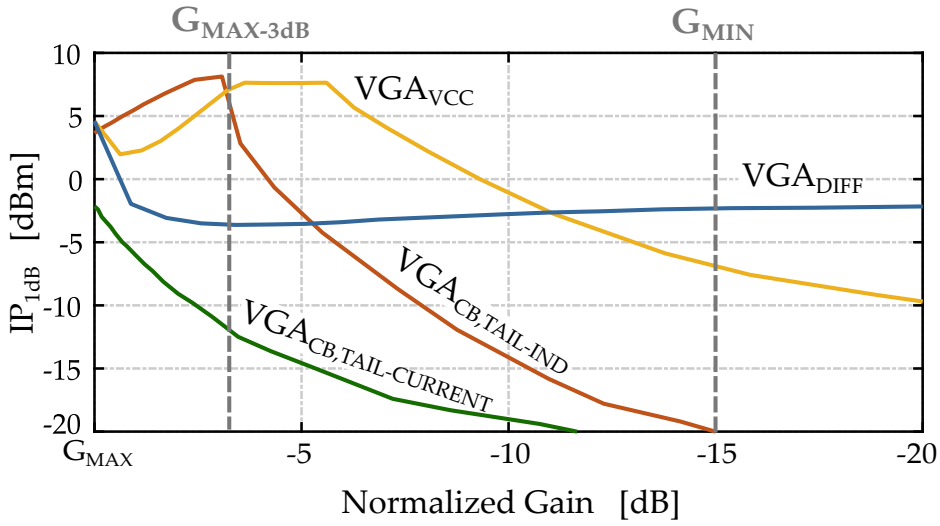


Figure 3.7: IP_{1dB} for the VGAs in Fig.3.

the circuit reduces to a single CB transistor as in Fig. 3.3b. However, when G_P decreases, a significant AM-AM compression is visible.
P_{IN} giving 1 dB AM-AM_{VGA}, either compression or expansion, is finally plotted in Fig. 3.7 versus the G_P variation for all the VGAs in Fig. 3.3. The VGA_{CB} with a tail current source shows the worst IP_{1dB} and it is not considered further. The other three options have the same $IP_{1dB} = 4$ dBm at $G_P = G_{MAX}$. IP_{1dB} of the VGA_{DIFF} drops sharply and settles to -4 dBm, nearly independent from G_P variation. The IP_{1dB} of VGA_{CB} and VGA_{VCC} is 7 dBm at G_{MAX}-3dB and then decreases to -20 dBm and -7 dBm, respectively, at G_{MIN}.

Let's now focus on the AM-PM distortion. In all the VGAs of Fig. 3.3, the input current to each HBT is partitioned between the admittance and the susceptance at the emitter node (at first order equal to g_m and ωc_π respectively, in the small signal regime, with c_π the base-to-emitter capacitance). The bias-dependent pole frequency (approximately at the device's $f_T = g_m/c_\pi$) results in an input-output phase shift that varies with G_P. Referring to the phase shifter output, this gain-to-phase variation may be seen as a quadrature error on the I/Q interpolated vectors that can be corrected through calibration. Conversely, when the average current in the HBTs is either expanded or compressed by a large input signal, the phase shift is affected by the input power level, P_{IN}, leading to AM-PM distortion. Fig. 3.8 plots the simulated AM-PM_{VGA} at $P_{IN} = IP_{1dB}$ against the variation of G_P for the three VGAs (the VGA_{CB} with the tail current source is not considered). Simulations highlight a similar performance for the three VGAs with AM-PM_{VGA} within 5° in all the cases.

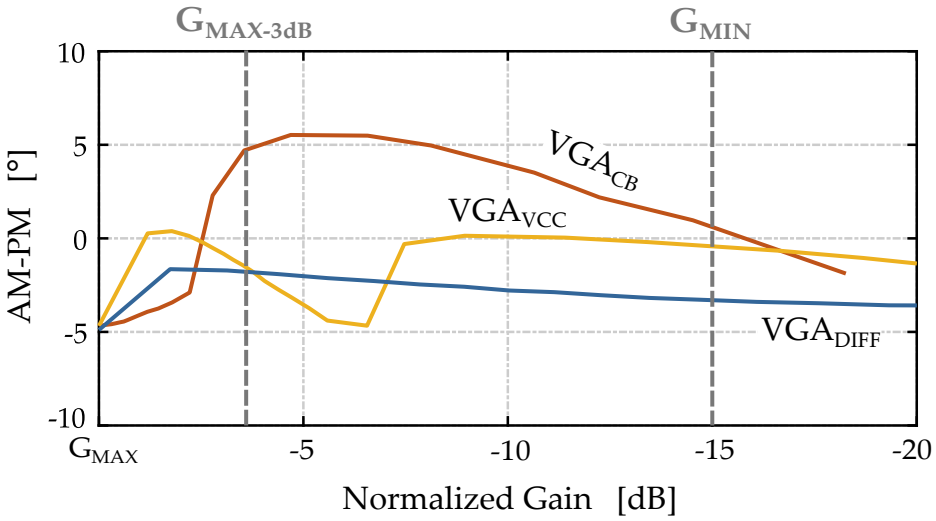


Figure 3.8: AM-PM @ P_{1dB} of the VGAs versus gain setting.

Performance Summary and Impact on the Phase Shifter

All the considered VGAs can provide the 15 dB gain control required to support a consistent phase resolution of 10°. From the analysis in Sec. 3.1.1, the AM-AM_{VGA} and AM-PM_{VGA} impair the phase shifter distortion in a different way, depending on the output phase. The two limit cases are when $\phi_o = 45° + n \cdot 90°$ and when $\phi_o = \pm \Delta\phi_o + n \cdot 90°$.
In the first case, eq. (3.5) predicts that the IP_{1dB} and the AM-PM of the phase shifter, are the same of a VGA operating at $G_P = G_{MAX\text{-}3dB}$ ($IP_{1dB,GMAX\text{-}3dB}$ and AM-PM_{VGA} at $G_P = G_{MAX\text{-}3dB}$, $P_{IN} = IP_{1dB,GMAX\text{-}3dB}$). The IP_{1dB} is then increased by 3 dB due to the power split of the input quadrature coupler.
If $\phi_o = \pm \Delta\phi_o + n \cdot 90°$, based on eq. (3.12) the phase shifter IP_{1dB} is 3-dB higher (again because of the input coupler) than the one of the VGA at $G_P = G_{MAX}$ ($IP_{1dB,GMAX}$), but eq. (3.12) shows that the phase shifter AM-PM distortion is influenced by both the AM-PM of the VGA at G_{MAX} (AM-PM_{VGA} at $G_P = G_{MAX}$, $P_{IN} = IP_{1dB,GMAX}$) and by the large AM-AM of the other VGA which is working at $G_P = G_{MIN}$ but it is driven by same P_{IN} of the other VGA (AM-AM_{VGA} at $G_P = G_{MIN}$, $P_{IN} = IP_{1dB,GMAX}$).

The performance of the three VGAs, in the conditions of interest, are extracted from simulations and summarized in Table 3.1. $IP_{1dB,GMAX}$ is the same in all the cases, but $IP_{1dB,GMAX\text{-}3dB}$ is remarkably different, ranging from -4 dBm for VGA_{DIFF} to +7 dBm for the VGA_{VCC}. The same happens for the AM-AM at $G_P = G_{MIN}$, $P_{IN} = IP_{1dB,GMAX}$. In this condition, G_P expands by 10 dB and 5 dB in the VGA_{CB} and VGA_{VCC}, respectively, while it shows a compression of -8 dB in the VGA_{DIFF}. The AM-PM is comparable for all the three VGAs and relatively limited.

Table 3.1: VGAs AM-AM and AM-PM Performance Summary.

		VGA_{CB}	VGA_{VCC}	VGA_{DIFF}
IP_{1dB} @ $G_P = G_{MAX}$	[dBm]	+4	+4	+4
$AM\text{-}PM_{VGA}$ @ $G_P = G_{MAX}$, $P_{IN} = IP_{1dB,GMAX}$	[°]	-5	-5	-5
IP_{1dB} @ $G_P = G_{MAX}$ - 3 dB	[dBm]	+7	+7	-4
$AM\text{-}PM_{VGA}$ @ $G_P = G_{MAX}$ - 3 dB, $P_{IN} = IP_{1dB,GMAX\text{-}3dB}$	[°]	+4	-2	-2
$AM\text{-}AM_{VGA}$ @ $G_P = G_{MIN}$, $P_{IN} = IP_{1dB,GMAX}$	[dB]	+10	+5	-8

The predicted phase shifter performance, considering the VGAs impairments through eqq. (3.5), (3.12), are reported in Table 3.2. VGA_{DIFF} gives the lowest AM-PM, within 5°, but IP_{1dB} is poor, limited to -1 dBm when the VGA is used with G_P below G_{MAX}. VGA_{CB} and VGA_{VCC} enable a substantially higher $IP_{1dB} = 7$ dBm. The use of VGA_{CB} leads to a very large $AM\text{-}PM_{PS}$, above 25°. VGA_{VCC} gives the best compromise between AM-AM and AM-PM distortion. A final aspect deserving attention is the noise performance, which may be critical when the phase shifter is used in a receiver. Although the effect of the phase shifter noise is attenuated by the gain of the preceding low-noise amplifier, a low noise figure (NF) remains desirable. Qualitatively, VGA_{CB} and VGA_{VCC} have similar performance, as only the noise of Q_1 sees a direct path towards the output. On the other hand, in the VGA_{DIFF}, two devices, Q_1 and Q_2, inject uncorrelated noise, leading to a roughly 3 dB NF penalty with respect to the other VGA alternatives.

Table 3.2: Impact of VGAs on Phase Shifter Distortion.

		VGA_{CB}	VGA_{VCC}	VGA_{DIFF}
IP_{1dB} @ $\phi_o = 45° + n \cdot 90°$	[dBm]	+10	+10	-1
AM-PM @ $\phi_o = 45° + n \cdot 90°$	[°]	+4	-2	-2
IP_{1dB} @ $\phi_o = \pm \Delta\phi_o + n \cdot 90°$	[dBm]	+7	+7	+7
AM-PM @ $\phi_o = \pm \Delta\phi_o + n \cdot 90°$	[°]	-5 ± 22	-5 ± 7.5	-5

3.1.3 Circuit Design

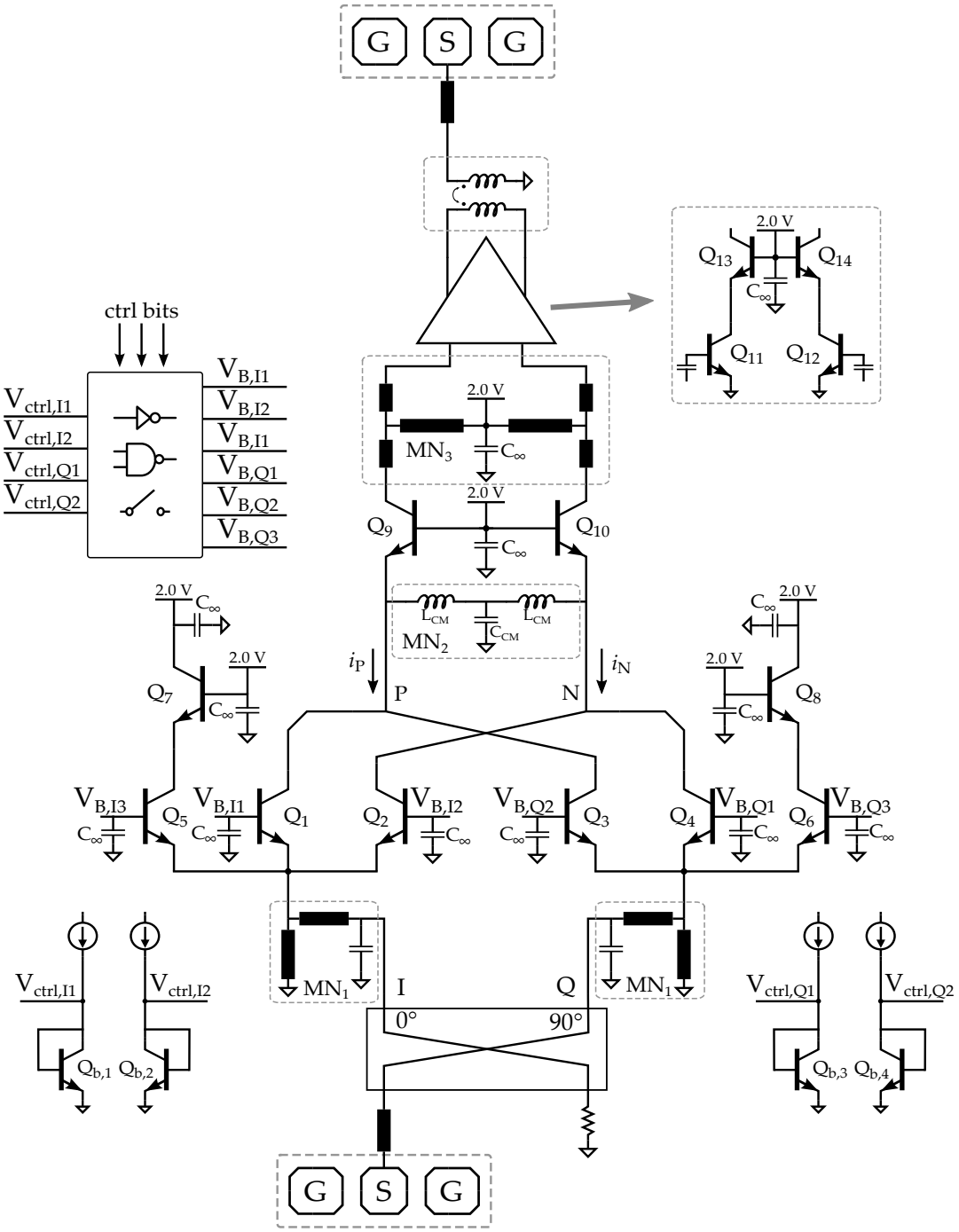


Figure 3.9: Schematic of the implemented vector-interpolation phase shifter.

The design of a vector-interpolation phase shifter in D-band is presented in this section. The complete circuit schematic is drawn in Fig. 3.9. The core of the phase shifter, on the bottom side, delivers the currents i_P, i_N. In the top side, buffer stages rise the gain and a balun provides an output signal proportional to i_P - i_N.
After the input GSG pad, a 3-dB coupled-line hybrid coupler generates two

single-ended signals with 90° phase difference (I and Q). The coupler is inherently broadband, with both low quadrature error and amplitude unbalance [49], [58]. The I and Q signals are then fed into the VGA core through the matching networks MN_1. To cover a 0°- 360° phase shift range, both the sum and difference of the I and Q signals are required. This can be achieved by implementing differential VGAs, as in [54], [59], [60], at the price of two baluns after the 3 dB hybrid coupler to make the signals differential. To avoid the bandwidth penalty of the baluns and the large footprint, the phase shifter architecture is the same originally introduced in [48] and subsequently implemented, in different fashions, in [51], [52]. The VGAs have a single-ended input, but the positive or negative gain can be achieved by injecting the output signal into node P or node N respectively.
The analysis in Sec. 3.1.2 suggests that the VGA based on current bleeding to V_{CC}, with the core circuit topology in Fig. 3c and referred to as VGA_{VCC}, promises the best trade-off between AM-AM_{PS} and AM-PM_{PS} distortions. This VGA architecture is thus implemented in the phase shifter with HBTs Q_1 - Q_6. Q_5 and Q_6 are the current-bleeding devices, steering part of the I and Q currents toward V_{CC} to reduce gain. Q_1 and Q_2 are used, respectively, to sum and subtract the I vector. The same applies for Q_3 and Q_4 but for the Q vector.
The VGA output currents, i_P, i_N, for any desired phase shift, ϕ_o, can be written in the four quadrants as follow:

$$\begin{aligned}
\phi_o \in [0^\circ - 90^\circ] \quad &\rightarrow \quad \begin{cases} i_P = i_o(|\cos\phi_o| + j|\sin\phi_o|) \\ i_N = 0 \end{cases} \\
\phi_o \in [90^\circ - 180^\circ] \quad &\rightarrow \quad \begin{cases} i_P = j\, i_o|\sin\phi_o| \\ i_N = i_o|\cos\phi_o| \end{cases} \\
\phi_o \in [180^\circ - 270^\circ] \quad &\rightarrow \quad \begin{cases} i_P = 0 \\ i_N = i_o(|\cos\phi_o| + j|\sin\phi_o|) \end{cases} \\
\phi_o \in [270^\circ - 360^\circ] \quad &\rightarrow \quad \begin{cases} i_P = i_o|\cos\phi_o| \\ i_N = j\, i_o|\sin\phi_o| \end{cases}
\end{aligned} \tag{3.18}$$

The balun, after the output buffer in Fig. 3.9, delivers a signal proportional to the differential-mode current component, $i_{DM} = (i_P - i_N) / 2$. Using (3.18), the latter can be written, for any value of ϕ_o, as:

$$i_{DM} = \frac{1}{2} i_o(\cos\phi_o + j\, \sin\phi_o) = \frac{1}{2} i_o\, e^{j\phi_o} \tag{3.19}$$

confirming that the output signal is phase shifted by ϕ_o at constant amplitude. Interestingly, if the current-bleeding transistors are turned-off, the remaining HBTs, Q_1 - Q_4, can be exploited to test the other VGA architectures analyzed in the previous section, VGA_{CB} and VGA_{DIFF}, allowing an experimental validation

of the analysis in Sec. 3.1.1 and Sec. 3.1.2. To implement VGA_{CB}, Q_1 and Q_2 are alternately turned on to sum and subtract the I vector, with gain controlled by the quiescent current of the active transistor through its base voltage ($V_{B,I1}$ or $V_{B,I2}$). The same applies for Q_3, Q_4, used to sum and subtract the Q vector with a gain controlled by the respective base voltages ($V_{B,Q1}$ or $V_{B,Q2}$). In this case, i_P, i_N and the differential-mode component, i_{DM}, are still given by (3.18) and (3.19).
To implement the VGA_{DIFF} the transistors in each pair (Q_1 - Q_2 and Q_3 - Q_4) are biased at constant current and operated concurrently. Q_1 - Q_2, controlled by the differential voltage $V_{B,I1}$ - $V_{B,I2}$, modulate the amplitude and sign of the I vector by splitting the in-phase input current and injecting it into node N and node P with proper weights. Q_3 - Q_4, controlled by the differential voltage $V_{B,Q1}$ - $V_{B,Q2}$, do the same for the Q vector. With transistors implementing VGA_{DIFF}, i_P and i_N are always nonzero and contain both I and Q current components in all the four quadrants. To have the same differential-mode output current given by (3.19), lengthy but straightforward calculations prove that:

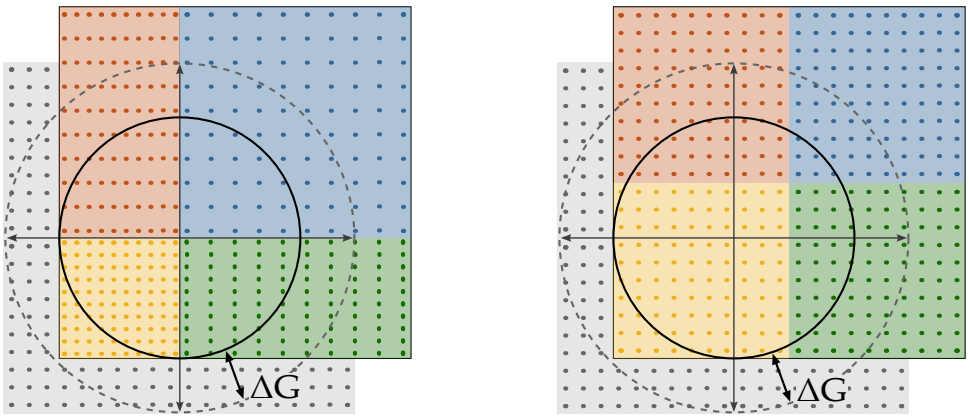
$$\begin{cases} i_P = \frac{1}{2} i_o [(1 + \cos\phi_o) + j(1 + \sin\phi_o)] \\ \\ i_N = \frac{1}{2} i_o [(1 - \cos\phi_o) + j(1 - \sin\phi_o)] \end{cases} \tag{3.20}$$

Following the core of the VGA, Q_9 and Q_{10}, stacked in common-base under the same supply, are working as current buffers. Q_7 and Q_8 are dummy common-base HBTs to replicate the boundary conditions at the collectors of Q_5 - Q_6 with Q_1 - Q_4. The matching network MN_3 performs impedance match between the collectors of Q_9 and Q_{10} and the output buffer. The latter consists of a pseudo-differential cascode stage, composed of HBTs Q_{11} - Q_{14}, with the purpose of increasing the overall gain and to rise the output power at 1 dB gain compression (OP_{1dB}) of the phase shifter. All the transistors have a drawn emitter area of 8 x 0.2 μm^2 and the maximum bias current for each single branch is 8 mA. The bias currents of the VGA's HBTs are controlled via external current DACs which feed diode-connected transistors Q_{b1} - Q_{b4} and generate the four bias voltages $V_{ctrl,I1}$, $V_{ctrl,I2}$, $V_{ctrl,Q1}$, $V_{ctrl,Q2}$. The latter are routed to the base of the HBTs through pass-gates and a simple logic circuit (drawn on the top-left in Fig. 3.9) which select the VGA operating mode, among the three possibilities, and the active HBTs in each quadrant through externally provided control bits. In all the possible operating modes, VGAs have a single-ended input and, ideally, a differential output. With this phase shifter architecture, attention has to be paid to suppress the high common-mode output current component, $i_{CM} = (i_P + i_N)$, an issue which was recognized, but only qualitatively discussed, in [48]. When Q_1 - Q_4 are implementing VGA_{VCC} or VGA_{CB}, i_{CM} can be calculated from (3.18):

$$i_{CM} = i_o(|\cos\phi_o| + j|\sin\phi_o|) \tag{3.21}$$

while for the VGA_{DIFF}, from (3.20):

$$i_{CM} = i_o(1+j) = \sqrt{2}\, i_o\, e^{j\frac{\pi}{4}} \tag{3.22}$$



(a) (b)

Figure 3.10: Output polar map distortion with finite CMRR for VGA_{CB}/VGA_{VCC} (a) and VGA_{DIFF} (b).

The common-mode rejection ratio, $CMRR = i_{DM}/i_{CM}$, of 0 dB for the VGA_{VCC} and VGA_{CB}, and of -3 dB for the VGA_{DIFF}, is definitely poor. Notably, VGA_{DIFF}, which resembles a differential-pair, has (slightly) worse CMRR than the other VGAs. The low CMRR causes two issues. First, the large common mode current propagating through the cascaded stages (Q_9 - Q_{10} and the output buffer) leads to a useless and undesirable increase of swing in the HBTs. The latter must be oversized and biased with higher current to avoid gain compression. The issue can be solved introducing some common-mode rejection at the early stage of the phase shifter. To this purpose, the network MN_2 (with components $L_{CM} = 15$ pH and $C_{CM} = 145$ fF) introduces a common-mode series resonance at 150 GHz, enough to ensure a minimum 10 dB common-mode rejection over the 125 - 175 GHz range. This network effectively reduces by at least a factor of 3 the undesired common mode current entering in Q_9 - Q_{10}. Moreover, L_{CM} is sized to resonate with the parasitic capacitance at the nodes P-N, increasing gain by 3 dB. At the same time, this reduces the noise contribution of Q_9 - Q_{10}, effectively reducing the noise figure of the overall phase shifter by 4 dB.
A second issue is the distortion of the phase shifter output polar map. Sweeping all the possible gain values of the I and Q VGAs independently, the vector representing the differential component of the output current is moved within a square in the I - Q plane and centered at the origin. If the common-mode component is not totally suppressed, the square is shifted and distorted. To gain insight, Fig. 3.10 plots the shape of the output polar map in the ideal case ($i_{CM} = 0$) and with finite CMRR for the VGA_{VCC} or VGA_{CB} (Fig. 3.10a) and for the VGA_{DIFF} (Fig. 3.10b). Focusing first on Fig. 3.10b, (3.22) shows that the common-mode current of the VGA_{DIFF} is a vector pointing toward 45°, i.e. the

center of the first quadrant. Consequently, the finite CMRR shifts the ideal polar map toward the first quadrant. From (3.21) the common-mode current of VGA_{VCC} and VGA_{CB} is a vector moving inside the first quadrant for any ϕ_o. Therefore, as shown by Fig. 3.10a, a finite suppression of the i_{CM} expands the points on the positive I e Q directions and compresses the points in the negative directions. In all the cases, the output polar map has still a square shape, but it is no longer centered at the origin. The radius of the largest possible circle centered at the origin and inscribed in the polar map, which represents the maximum achievable constant gain across the 0° - 360° phase shift, is reduced. Through geometrical considerations, it is possible to prove that the gain penalty is:

$$\frac{\Delta G}{G} = 20 \log \left(1 - \frac{1}{|CMRR|} \right) \tag{3.23}$$

As a numerical example, a CMRR of 20 dB introduces a gain penalty of 1 dB, which reduces to 0.3 dB if the CMRR is increased to 30 dB. Targeting a minimum CMRR of 30 dB, and accounting for the 10 dB common-mode rejection of MN_2, the CMRR of the output balun in Fig. 3.9 must be greater than 20 dB. The balun must provide differential to single-ended conversion and, possibly, it should also upscale the 50 Ω off-chip load into a higher impedance to rise the gain of the output buffer. The differential load impedance seen at the collector of Q_{13} - Q_{14} is set to 200 Ω. A traditional transformer layout, made of concentric intertwined coils, with equivalent circuit in Fig. 3.11a, requires the inductance at the differential port, L_1, to be four times the inductance at the single-ended port, L_2. The high L_1/L_2 ratio limits the magnetic coupling and rises losses [61].

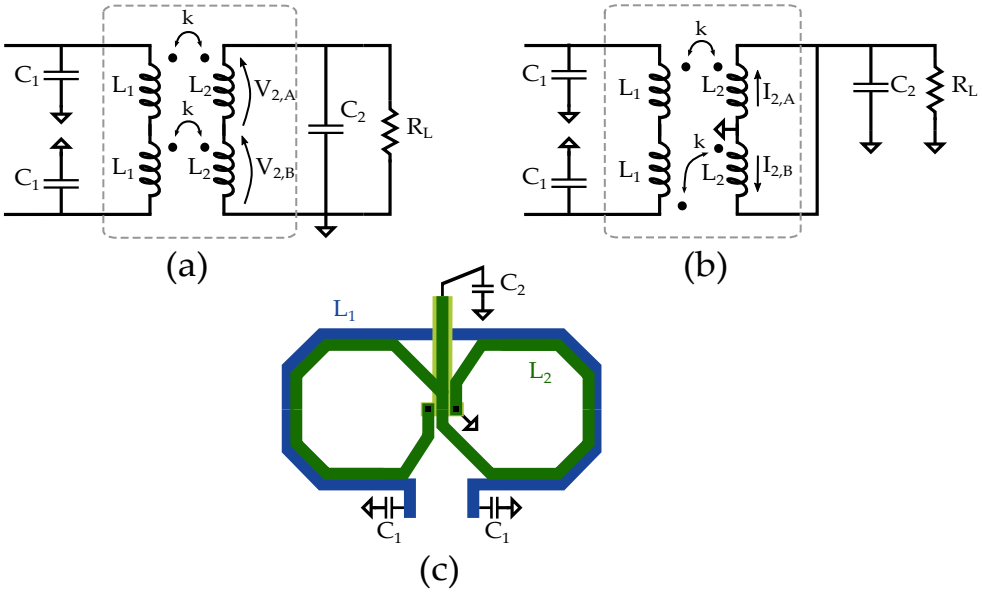


Figure 3.11: Equivalent circuit of a coupled windings balun: the conventional (a) and proposed (b). Layout implementation of the proposed balun (c).

A different balun geometry is investigated and implemented in the phase shifter to solve the issue above. The equivalent circuit model is shown in Fig. 3.11b. The single-ended inductor L_2 consists of two windings in parallel, rather than in series, coupled to the two halves of the single-ended inductor L_1 with opposite signs. In this case, the single-ended output is produced summing the currents in L_2, $I_{2,A}$ and $I_{2,B}$, rather than the voltages, $V_{2,A}$ and $V_{2,B}$ as in the conventional balun topology.
The physical layout of the proposed balun is drawn in Fig. 3.11c. L_1 is the blue external coil. L_2 is realized by two coils, winded in opposite directions and forming the 8-shape to have the positive and negative couplings with L_1. Through standard network analysis, the following Z-matrix can be derived for the proposed balun:

$$Z = \begin{bmatrix} 2sL_1 & sM \\ sM & s\frac{L_2}{2} \end{bmatrix} \tag{3.24}$$

where $M = k\sqrt{L_1 L_2}$ represents the mutual inductance (with k being the magnetic coupling factor). Notably, with $L_1 = L_2$, (3.24) shows that the proposed balun is equivalent to a conventional balun of Fig. 3.11a with a 4:1 inductance ratio, meaning that 4:1 impedance transformation of 50 Ω into 200 Ω can be achieved with a nearly equal size of the inductors.
To perform broadband matching, the balun is tuned to achieve a 4^{th} order response [61] with values $L_1 = L_2 = 44$ pH, $k = 0.4$, $C_2 = 60$ fF, and C_1=30 fF being the equivalent output parasitic capacitance of the buffer. Notably, thanks to the 8-shaped secondary winding, the coupling factor when the primary side is driven by a common mode signal is ideally null (electromagnetic simulations point out $k_{CM} < 0.05$), ensuring a good common mode rejection ratio. Fig. 3.12a plots the simulated differential and common-mode impedance. Over the band of interest, $Z_{DM} > 200\,\Omega$ while maintaining a low common mode impedance, $Z_{CM} < 50\,\Omega$. This ensures a low common-mode voltage swing at the collectors of Q_{13} - Q_{14}, not lowering their voltage headroom and thus not penalizing the linearity of the buffer. Fig. 3.12b shows the simulated insertion loss, of roughly 2 dB and a CMRR above 25 dB, sufficient to meet the design target.

Post-layout simulations of the overall phase shifter are reported in Fig. 3.13 and Fig. 3.14. Fig. 3.13a shows separately the power gain, G_P, of the phase shifter core up to matching network MN_3 (included), and of the following buffer stage. The curves are obtained in the 0° phase setting (i.e. with the I-path VGA at maximum gain and the Q-path VGA off) for the different VGA configurations. Results report an average insertion loss of ~3 dB for the phase shifter core and a gain of ~8 dB for the buffer stage. Fig. 3.13b shows the overall forward transducer gain S_{21} and input reflection coefficient S_{11} in the same configurations. The gain is 4-5 dB with a -3-dB bandwidth ranging from 130 GHz to 180 GHz in all the VGA operating modes. S_{11} is well below -10 dB

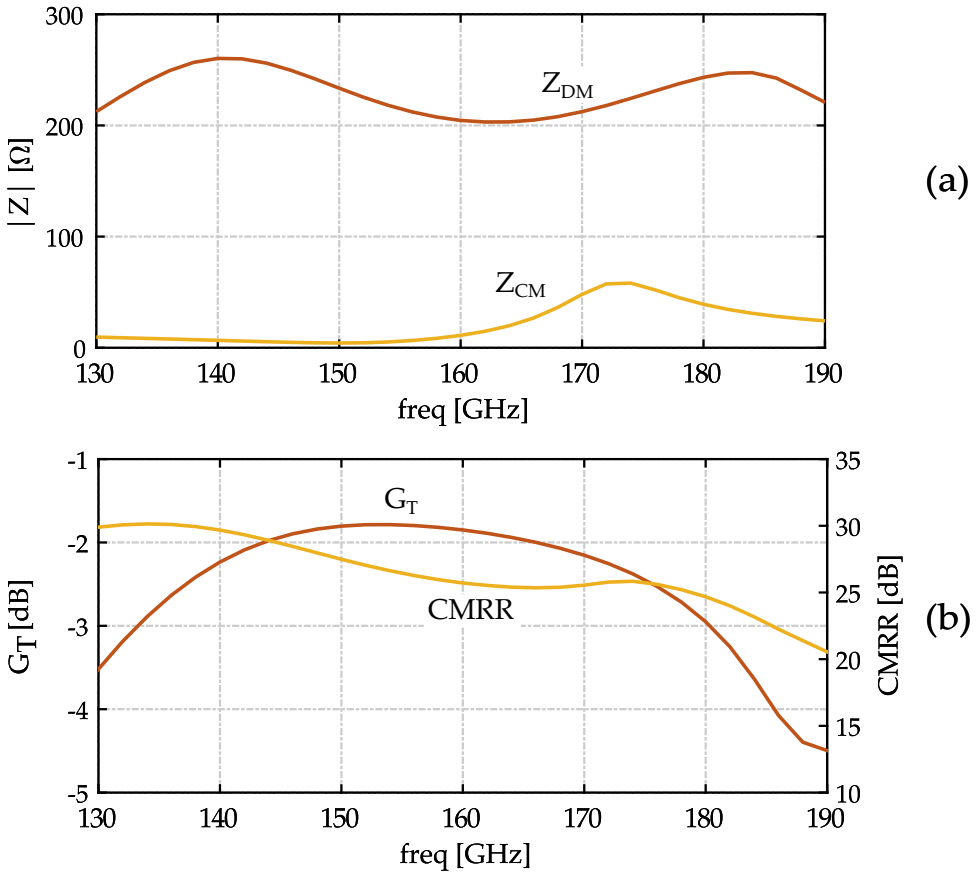


Figure 3.12: Simulated performance of the implemented balun: input differential mode Z_{DM} and common mode Z_{CM} impedance (a), power gain G_T and CMRR (b).

over the entire operating range for the VGA_{VCC} and VGA_{DIFF}, presenting a symmetrical loading to the I and Q ports of hybrid coupler. S_{11} is worse, but close to -10dB, for the VGA_{CB} because the ports of the hybrid coupler are not equally terminated.

Fig. 3.13 reports the linearity of the phase shifter in terms of OP_{1dB} (a) and AM-PM_{PS} (b). The results are plotted only over the 0°-90° output phase range because the same behavior is observed across the four quadrants. Solid lines refer to the single-ended signal, after the output balun, while dashed lines are referred to the differential signal at the collectors of Q_1 - Q_4, before the cascode output buffer. Let us first focus on the dashed lines. Simulations clearly confirm the performance difference in the three VGA modes expected from the analysis in Sec. 3.1.1 and III. VGA_{DIFF} shows a sharp OP_{1dB} degradation of 8 dB when moving away from the $n \cdot 90°$ phase shift settings, while VGA_{CB} and VGA_{VCC} demonstrate a roughly constant OP_{1dB}. On the other hand, looking at the AM-PM_{PS}, VGA_{DIFF} and VGA_{VCC} show the best performance with a phase distortion in both cases below 10°. VGA_{CB} gives the worst AM-PM_{PS}, as predicted by the analysis in Sec. 3.1.2, with a peak to 30°. Considering now the phase shifter with output buffer (solid lines), the buffer increases the OP_{1dB} by 2 dB but, with 8 dB gain, decreases the IP_{1dB} by 6 dB. The reduced input

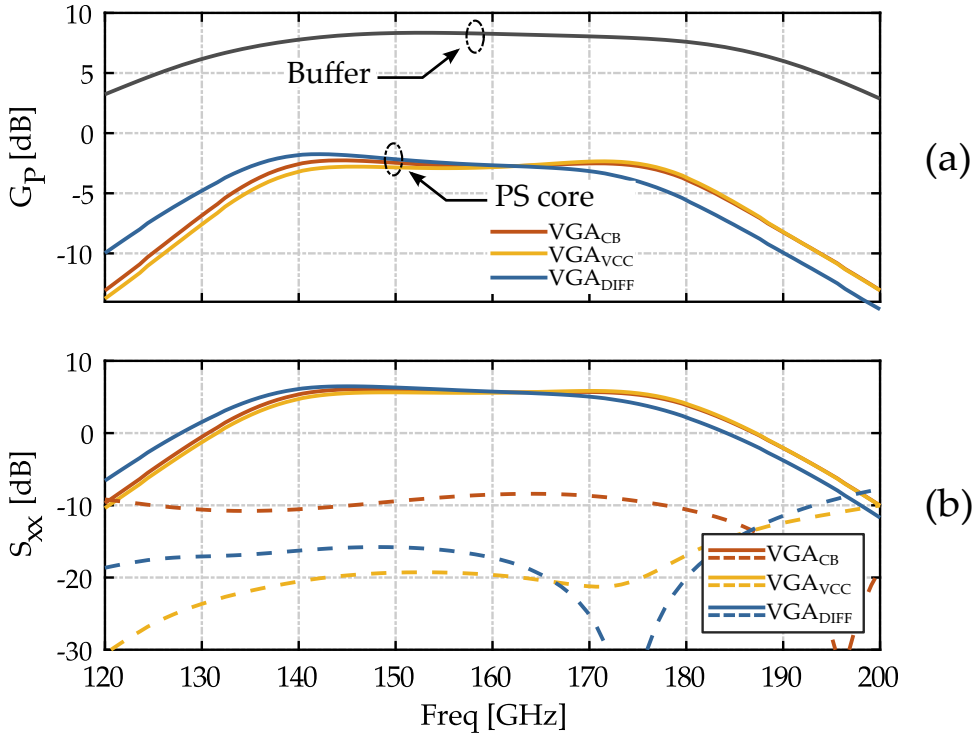


Figure 3.13: (a) Simulated power gain (G_P) of the phase shifter core, up to MN_3 (included), and buffer stage in the three VGA configurations. (b) Simulated forward gain (S_{21}) and input matching (S_{11}) of the overall phase shifter chain.

power to the phase shifter brings the VGAs to operate in a more linear region and smooths the performance differences. However, also in this condition the VGA_{VCC} preserves the best results with an $OP_{1dB} = 2\,dBm$ and AM-PM $< 8°$ across the full range of ϕ_o.
From simulations (not shown), the output third order intercept point (OIP_3) is in agreement with the approximated value of $OP_{1dB} + 9.6\,dB$. This holds for the three VGA operating modes and across 0°-90° phase-shift range.

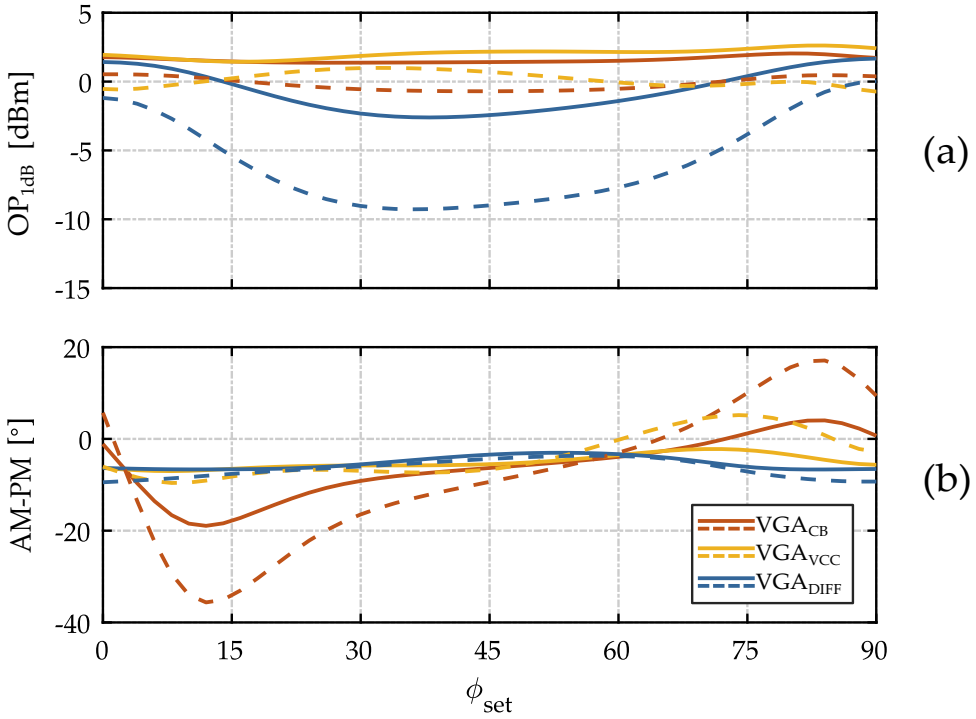


Figure 3.14: Simulated OP_{1dB} (a) and AM-PM (b) of the phase shifter in the three VGA configurations. Performance at the differential output of the core (dashed lines) and single-ended output after the buffer (solid lines).

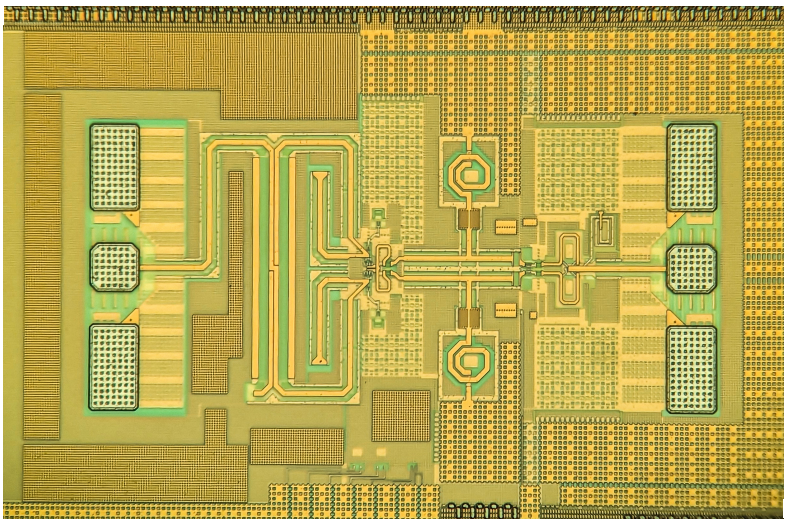


Figure 3.15: Die photograph of the realized vector-interpolation phase shifter.

3.1.4 Experimental Results

The phase shifter is realized in the 55 nm SiGe BiCMOS technology by STMicroelectronics. Fig. 3.15 reports the chip photo, with a core area of 360 x 240 μm^2, excluding GSG pads. For measurements, the chip is glued on a PCB and the supply, biasing and control signals are wire bonded. A second PCB embeds current DACs to control the VGA bias currents, and a microcontroller sets the on-chip control logic. Measurements are first carried out with the

VGA_{VCC} mode. The current consumption is 32 mA from 2 V supply. An Agilent E8361C VNA equipped with VDI WR6.5-VNAX frequency extension modules is connected through Infinity Waveguide GSG probes. S-parameter curves are acquired by an automated routine sweeping all the I and Q VGA states with a resolution of 6 bits, corresponding to an acquired space map of 2^6 x 2^6 for each frequency point between 130 GHz and 175 GHz.

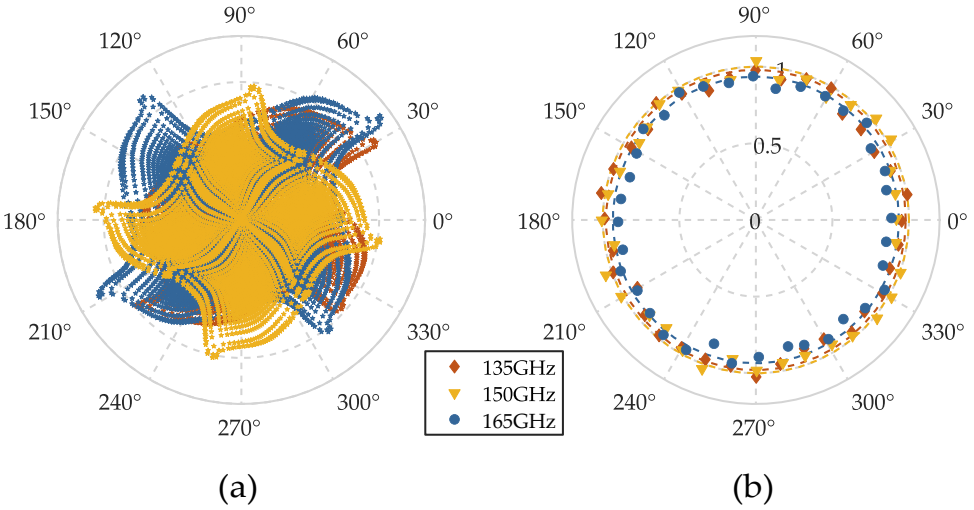


Figure 3.16: Measured output polar map (a) and calibrated constant gain circles (b) at the calibration frequencies.

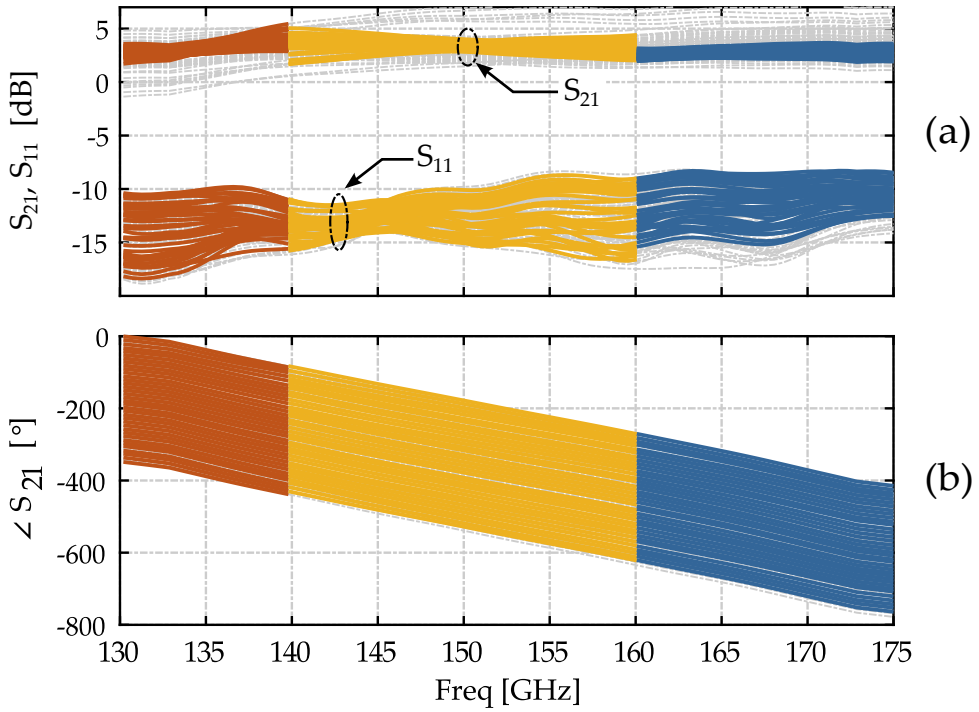


Figure 3.17: Measured S_{21} and S_{11} (a) and phase response (b) of the interpolated states in the three calibration ranges.

Fig. 3.16a reports the output polar map at three frequencies, 135 GHz, 150 GHz

and 165 GHz. Notably, the maps are well centered and present a uniform distribution of the points in the four quadrants. This confirms the high enough CMRR within the phase shifter core and the output balun. With respect to the ideal squared shape, the output vector space appears distorted along the edges. This behavior is explained by the variation of the VGAs phase when the gain is changed. The collected dataset is post-processed in MATLAB to extract the control codes that best fit the constant gain circles with a phase step of 10° at the three frequencies. The points extracted after calibration are shown in the

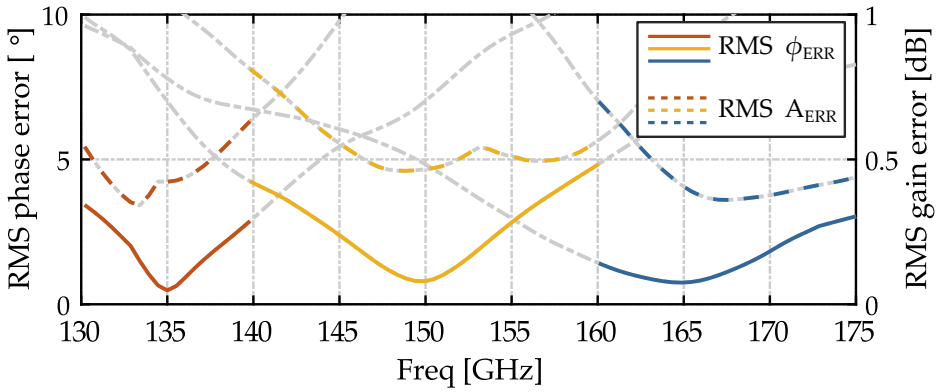


Figure 3.18: RMS phase and amplitude errors across frequency.

polar plot of Fig. 3.16b, where the circles radii are normalized to the magnitude at 150 GHz.
Fig. 3.17a reports the magnitude of the forward gain and input reflection coefficients (S_{21}, S_{11}) of the phase shifter across frequency, while Fig. 3.17b plots the transmission phase. The control codes extracted at the calibration frequencies are applied for the sub-bands (1) 130 - 140 GHz, (2) 140 - 160 GHz, (3) 160 - 175 GHz highlighted in red, yellow and blue, respectively. The average forward gain is 3.5 dB with less than -1 dB variation across the 130 - 175 GHz range.
From the calibrated settings it is possible to derive the RMS errors, defined as the phase variation from the ideal phase setting, $\phi_{set,i}$, and the amplitude variation from the average gain, $G_{T,avg}$, [62]:

$$\text{RMS } \phi_{err} = \sqrt{\frac{1}{N-1} \cdot \sum_{i=2}^{N} (\phi_{o,i} - \phi_{set,i})^2} \quad [^\circ] \tag{3.25}$$

$$\text{RMS } G_{T,err} = \sqrt{\frac{1}{N} \cdot \sum_{i=1}^{N} \left(G_{T,i\,[dB]} - G_{T,avg\,[dB]}\right)^2} \quad [dB] \tag{3.26}$$

The calculated RMS gain and phase error [62] across frequency in the three sub-bands are plotted in Fig. 3.18. The amplitude and phase errors are minimized at the calibration points but remain below 0.8 dB and 5° over the entire frequency range. From simulation results, the calibrated settings maintain validity over the temperature range [-10 – 85]°C with little to no impact on the

RMS phase and amplitude errors.
It is worth mentioning that the phase shifter may be set to operate also on different constant gain circle radii, thus allowing gain control. By using MATLAB post processing on the collected dataset, the phase shifter operated in the VGA_{VCC} mode can provide 10 dB gain regulation without penalties in the RMS phase and amplitude errors.
Fig. 3.19 shows the phase shifter NF measured at $\phi_o = 0°$ and $\phi_o = 45°$, corresponding to the best and worst case, respectively. At 150 GHz center frequency, the NF ranges from 14 to 16 dB and rises by 2 dB at the band edges. The same small-signal measurements were conducted also using the phase shifter with the VGA_{CB} and VGA_{DIFF} operating modes, giving similar results in terms of polar map, gain and RMS errors. Similar noise figure is measured for the VGA_{CB}, while for VGA_{DIFF} it is degraded by ≈3.5 dB in agreement with what discussed at the end of Sec. 3.1.2.

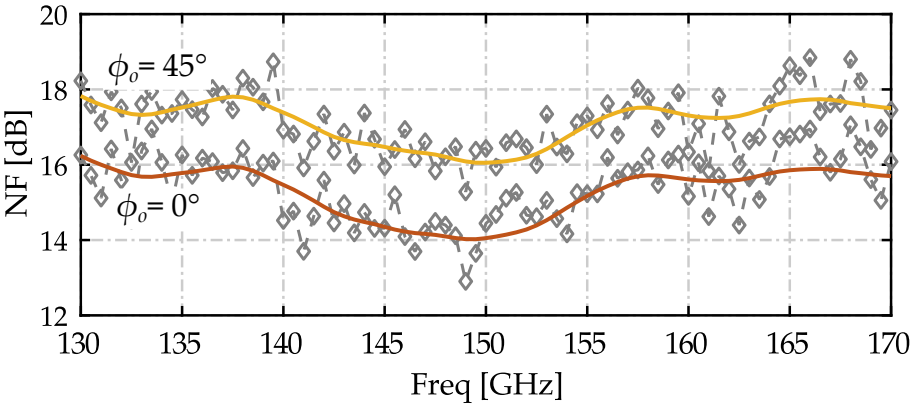


Figure 3.19: Measured noise figure of the phase shifter in the VGA_{VCC} mode.

Large signal tests are performed for all three VGA operating modes and they are obtained using ELVA-1 DPM-06 power meter for the OP_{1dB}, and the VNA along with frequency extension modules for the AM-PM. Results are shown in Fig. 3.20, reporting the OP_{1dB} and AM-PM at the center frequency of 150 GHz, for ϕ_o in the 0°- 90° range. For the VGA_{VCC} the OP_{1dB} is always greater than 1.8 dBm and the AM-PM with the phase shifter driven at the 1 dB gain compression point is maintained $< 10°$ across the full quadrant. Although VGA_{CB} shows similar OP_{1dB}, the AM-PM distortion is more than double the one demonstrated by VGA_{VCC}. On the other hand, VGA_{DIFF} has contained AM-PM distortion, at the expense of a 4 dB penalty in OP_{1dB}.
Experimental results confirm the analysis in Sec. 3.1.2 and are consistent with the simulations in Sec. 3.1.3. VGA_{VCC} is the preferable VGA topology, giving high OP_{1dB}, the same of VGA_{CB}, and low $AM\text{-}PM_{PS}$, comparable to the VGA_{DIFF}

Finally, the experimental results in the VGA_{VCC} mode are summarized in

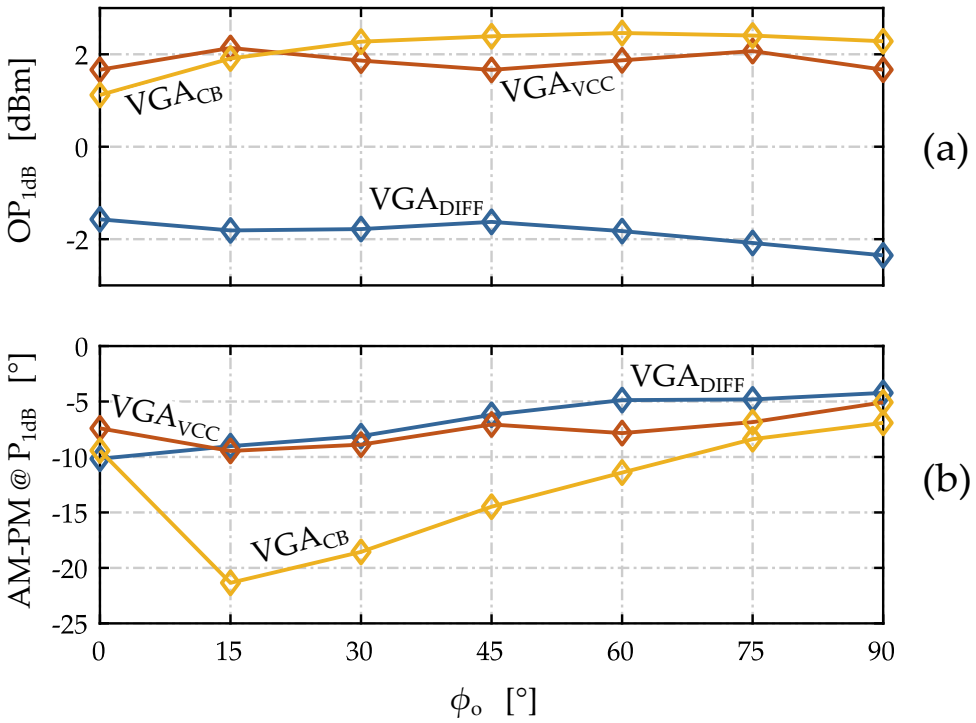


Figure 3.20: Comparison of the measured OP_{1dB} (a) and AM-PM@P_{1dB} (b) of the phase shifter at 150 GHz in the different VGAs operating modes.

Table 3.3 and compared with state-of-the-art active phase shifters operating in a similar frequency range. The proposed phase shifter achieves high gain, low RMS phase and amplitude errors and state-of-the-art fractional bandwidth, wider only in [63] at the expense of high insertion loss and 2 bit only phase resolution. At the same time, the phase shifter achieves the highest reported OP_{1dB} and collector efficiency, only comparable to [49]. The AM-PM, seldom reported in other works, is aligned with [52], which achieves a much lower gain, compression point and power efficiency.
On the right side of Table III, two state of the art passive phase shifters operating in the same frequency range are reported. [46] demonstrates a calibration free phase shifter with moderate insertion loss at the expense of narrow bandwidth. On contrary, [47] supports a wide bandwidth with with severe losses and area. Although, both passive and active phase shifters were successfully demonstrated to operate at D-band, the former show major performance trade-offs which may restrict their use depending on the application. On the other hand, active vector interpolation phase shifters offer a reasonable balance in terms of flexibility and performance.

Table 3.3: Performance summary and comparison.

		This Work	[49]	[50]	[63]	[51]	[52]	[64]	[53]	[54]	[46]	[47]
Topology		Vector interpolation									Passive	
Technology		55 nm SiGe	55 nm SiGe	90 nm SiGe	90 nm SiGe	130 nm SiGe	55 nm SiGe	130 nm SiGe	130 nm SiGe	130 nm SiGe	45 nm RFSOI	130 nm SiGe
f_t / f_{max}	[GHz]	320 / 370	320 / 370	310 / 375	310 / 375	- / 450	320 / 370	200 / 220	- / 450	300 / 500	-	300 / 500
f_0	[GHz]	130 - 175	130 - 175	110 - 145	140 - 220	162 - 190	140 - 160	105 - 125	160 - 200	130 - 170	135 - 145	110 - 170[§]
BW	[%]	30	30	27	46	16	13	17	22	27	7	44[§]
G_T	[dB]	3.5	-4.5	1.5	-8.7	-6.2	-4.5	4	-9.5	4	-10.7[†]	-21[†]
ϕ_{res}	[°]	10	10	22.5	90	22.5	11.25	22.5	22.5	2	11.25	[17 - 27]
RMS ϕ_{err}	[°]	5	8	8.5	16	8	7.5	9	15	-	1.6	-
RMS $G_{T,err}$	[dB]	0.8	1.2	1.2	1.5	1	1.4	2	0.9	-	0.6	1.4
OP_{1dB} @ f_0	[dBm]	1.8	-3	-6	-15.4	-27.2	-3.7	-10	-	-	1.8	-
AM-PM @ P_{1dB}	[°]	10	-	-	-	-	9	-	-	-	-	-
NF	[dB]	[14-18]	-	-	-	-	[19-20.5][*]	-	-	-	10.7[†]	21[†]
P_{DC} / V_{CC}	[mW / V]	64 / 2	19[†] / 2	20.3[†] / 1.5	5.4 / 1.85	12.6[†] / 1.8	50[†] / 3.3	44.6 / 2.2	8.6[†] / 2.4	66 / 3.3	0 / 1.2	6.2 / 0.9
η @ P_{1dB}	[%]	2.4	2.8[†]	1.2[†]	0.5	0.015[†]	0.8[†]	0.22	-	-	-	-
Core Area	[mm^2]	0.09	0.09	0.81	0.02	0.07	0.05	-	0.075	-	0.04	1.17

[†] Average value on the constant gain circle [*]Simulated value [§]Providing 360° only in [150 - 170] GHz band

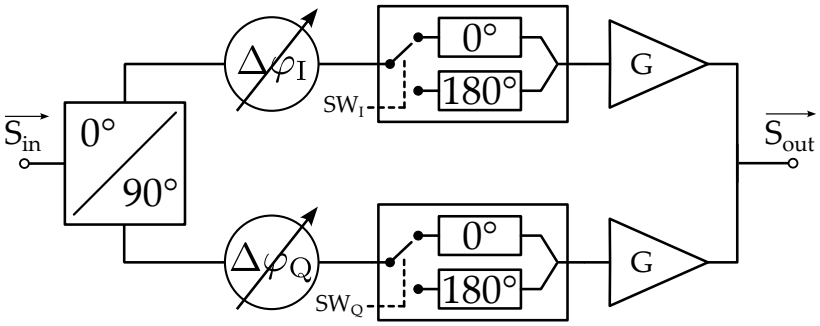


Figure 3.21: Block diagram of the proposed phase shifter.

3.2 Digital D-band phase shifter

The linearity issue in the vector interpolation phase shifters arises mainly from the need of VGAs, which must operate over a wide interval of gain control to achieve the fine phase shifting regulation. On the other hand, passive phase shifters have ideally no linearity impairment but bring other issues. [46] recently proposed a 140 GHz phase shifter based on a digitally tapped delay line, demonstrating a remarkably high $OP_{1dB} = 3.4$ dBm but with 10 dB attenuation and a narrow operation band. [45] employs two cascaded reflective-type phase shifters (RTPS) to cover 180° in fine steps and an active programmable phase inversion (0°/180°) stage, but still suffers from the same bandwidth issue, limited by the varactor-based terminations in the RTPS. [47] demonstrated broadband operation by implementing a true time-delay phase shifter, where the signal is routed to transmission lines (TLINEs) of different length through switches, but at the expense of 20 dB insertion loss, coarse phase control and large area occupation.
In [44] we investigated D-band passive networks providing a programmable phase shift in fine and coarse control steps. This paper proposes a digital phase shifter with the block diagram in Fig. 3.21, where the elementary networks presented previously are combined in a way to minimize power loss and to preserve the inherent broadband response. The input signal is split in two quadrature paths, later recombined by amplifiers to compensate for the networks losses. The amplitude of the output signal is controlled by adjusting independently the relative phase shift of the I/Q paths, similarly to the working principle of outphasing amplifiers [56], thus avoiding the need of VGAs. This choice allows the subsequent amplifiers to operate at constant-gain and at the optimal biasing condition for maximum linearity, leading to constant and high OP_{1dB}. The I/Q relative phase shift is also exploited for the correction of the quadrature and phase-inversion errors through proper calibrations. Experiments on a 55 nm SiGe BiCMOS test chip prove -2.3 dB gain and a broadband response from 125 GHz to 170 GHz. The phase-control resolution is 9° and, with calibrations applied, the RMS phase and amplitude errors are limited to

5° and 0.8 dB, respectively, across the full operation bandwidth. The OP_{1dB} is greater than 2 dBm over 0°-360° phase settings and over the entire frequency range with 31 mW power consumption from 2 V supply.

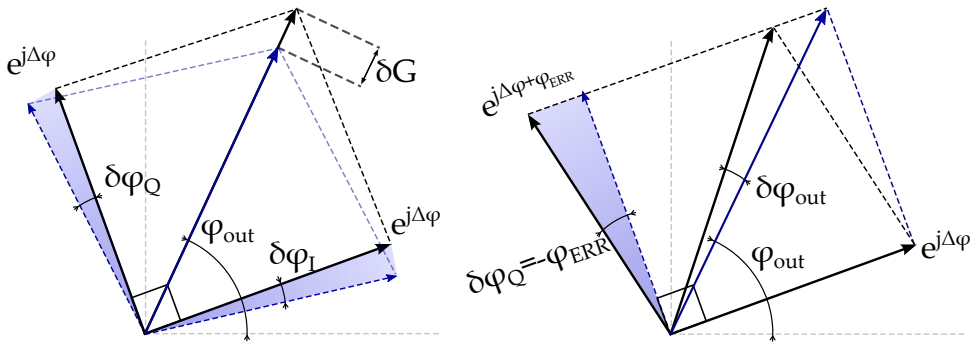
3.2.1 Operation Principle

The operation principle of the proposed phase shifter is presented in this section. Let us first assume ideal lossless networks in Fig. 3.21. The input signal S_{in} is passed through the hybrid coupler that generates I/Q components. The two quadrature signals feed a pair of blocks, referred to as $\Delta\varphi_{I,Q}$, which introduce a digitally controllable phase shift in a range exceeding 0°-90° with fine resolution. Assuming that the two phase shifters are controlled by the same digital word (thus $\Delta\varphi_I = \Delta\varphi_Q = \Delta\varphi$), the output signals on the I and Q paths are $\frac{1}{\sqrt{2}} \cdot S_{in} \cdot e^{j\Delta\varphi}$ and $j \cdot \frac{1}{\sqrt{2}} \cdot S_{in} \cdot e^{j\Delta\varphi}$, respectively. The two components are then fed to 0°/180° coarse-control phase shifters (that multiply the signals by ± 1), controlled by SW_I, SW_Q. The two quadrature vectors are finally summed at the output of two identical amplifiers with gain G. The overall phase shifter gain, $\overrightarrow{G_{PS}} = \overrightarrow{S_{out}}/\overrightarrow{S_{in}}$, and phase shift, $\angle\overrightarrow{G_{PS}}$, are summarized in the following table:

SW_I	SW_Q	$\overrightarrow{G_{PS}}$	$\angle\overrightarrow{G_{PS}}$
0	0	$\frac{G}{\sqrt{2}} \cdot (1+j) \cdot e^{j\Delta\varphi}$	[45° - 135°]
0	1	$\frac{G}{\sqrt{2}} \cdot (1-j) \cdot e^{j\Delta\varphi}$	[135° - 225°]
1	0	$\frac{G}{\sqrt{2}} \cdot (-1+j) \cdot e^{j\Delta\varphi}$	[225° - 315°]
1	1	$\frac{G}{\sqrt{2}} \cdot (-1-j) \cdot e^{j\Delta\varphi}$	[315° - 45°]

With $\Delta\varphi \in [0° - 90°]$ and a proper combination of SW_I SW_Q the input-output phase shift spans the 0°/360° range with resolution set by $\Delta\varphi$.
More realistically, the passive blocks introduce an insertion loss dependent on the phase settings, and a gain-correction functionality is needed to produce an output with variable phase but constant amplitude. To avoid the need for VGAs, which would impair the linearity, the gain regulation is performed by controlling independently the I/Q phase shifts $\Delta\varphi_I$, $\Delta\varphi_Q$. The concept, similar to the outphasing amplifier [56], is explained qualitatively in Fig. 3.22a. The two quadrature signals, $\frac{1}{\sqrt{2}} \cdot S_{in} \cdot e^{j\Delta\varphi}$, $j \cdot \frac{1}{\sqrt{2}} \cdot S_{in} \cdot e^{j\Delta\varphi}$ produce a vector with phase φ_{out}. By changing the relative phase between the quadrature components ($\Delta\varphi_I = \Delta\varphi - \delta\varphi_I$, $\Delta\varphi_Q = \Delta\varphi + \delta\varphi_Q$), it is possible to change the amplitude by δG while preserving the phase φ_{out}.
The independent control of $\Delta\varphi_I$, $\Delta\varphi_Q$ is also exploited to correct for a quadrature phase error of the two vectors being summed, due to a possible error introduced by the hybrid coupler or, more importantly, deviations from the 0°/180°

shift of the phase-inversion blocks. The situation is depicted in Fig. 3.22b. A quadrature error $\delta\varphi_{err}$ leads to an error $\delta\varphi$ on φ_{out}, which can be nulled by setting $\Delta\varphi_I = \Delta\varphi$, $\Delta\varphi_Q = \Delta\varphi$ - $\delta\varphi_{err}$.



(a) (b)

Figure 3.22: Outphasing principle for (a) gain control and (b) phase error correction.

3.2.2 Circuit Design

The detailed schematic of the phase shifter is drawn in Fig. 3.23. The 3-dB 90° coupler follows the design presented in [49], realized with 245 µm-long coupled-lines, corresponding to $\lambda/4$ at 150 GHz, and has characteristic impedance $Z_0 = 40\,\Omega$. The quadrature error and amplitude mismatch are lim-

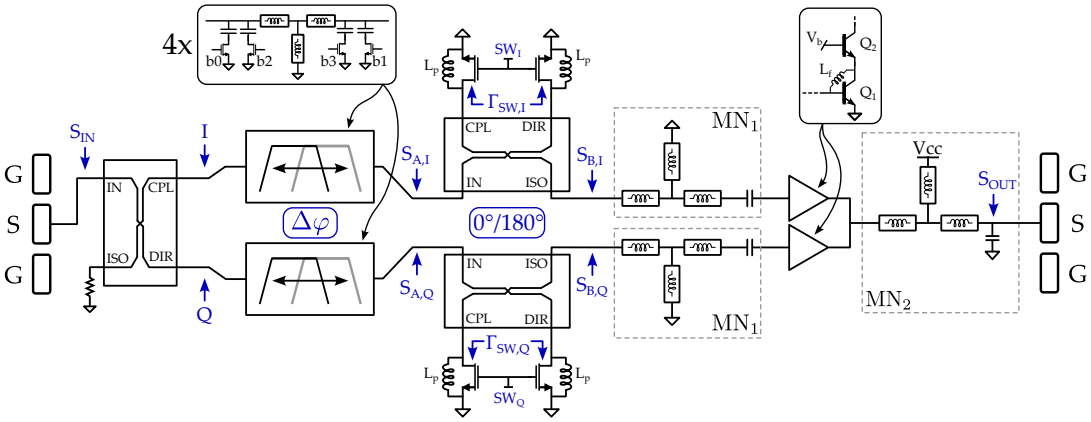


Figure 3.23: Schematic of the implemented phase shifter.

ited to 3° and 0.6 dB in the operating bandwidth, respectively. The fine-control programmable phase shifters, $\Delta\varphi_I$, $\Delta\varphi_Q$, are based on the cascade of four elementary band-pass filters with center frequency tunable by digitally switched capacitors, previously presented in [44]. The programmable phase shift is purposely selected larger than 90° in order to achieve a rotation of the output vector over one quadrant and include margin to be used for gain and phase corrections. From simulations, the input-output phase shift is programmable over a range of 130° at 125 GHz and 166° at 170 GHz. The insertion loss changes

from 4 to 7 dB at 125 GHz and from 4 to 10 dB at 170 GHz. The two phase-inversion block, 0°/180°, are realized with hybrid couplers working as RTPSs and operated with two switches. The signals $S_{A,I/Q}$ are equally split at the CLP/DIR ports. If the two ports are terminated on identical impedances with reflection coefficient $\Gamma_{SW,I/Q}$, the reflected components sum up at the ISO port, giving the signals $S_{B,I/Q}$ with a transfer function given by:

$$\left|\frac{S_{B,I/Q}}{S_{A,I/Q}}\right| = \left|\Gamma_{SW,I/Q}\right|^2 \qquad \angle\frac{S_{B,I/Q}}{S_{A,I/Q}} = -90° + \angle\Gamma_{SW,I/Q} \tag{3.27}$$

where $\Gamma_{SW,I/Q} = (Z_{SW,I/Q}\text{-}Z_0)/(Z_{SW,I/Q}+Z_0)$, being Z_0, $Z_{SW,I/Q}$ the characteristic impedance of the couplers and the impedance of the switches, respectively. Ideal switches present open or short circuit, thus, $\Gamma_{SW,I/Q} = \pm 1$. Consequently, $S_{B,I/Q}$ experience a 0°/180° relative phase shift with no attenuation. Real switches, instead, show a finite ON resistance r_{on} and a parasitic capacitance c_{sw}. According to (1), to have the same insertion loss when the phase shift is 0° and 180°, the switches must be sized to set the same magnitude of the reflection coefficient in the ON- and OFF-state: $|\Gamma_{SW,I/Q\text{-}ON}| = |\Gamma_{SW,I/Q\text{-}OFF}|$. Transistors are sized with W/L = 50 µm / 55 nm, giving $r_{on} = 7\,\Omega$. c_{sw} is resonated out by shunt inductors $L_p = 40$ pH (implemented with meandered TLINEs), giving an equivalent $r_{off} = 250\,\Omega$ and thus $|\Gamma_{SW,I/Q\text{-}ON}| \approx |\Gamma_{SW,I/Q\text{-}OFF}| \approx 0.7$. The resulting insertion loss is ≈3 dB, which sums to the 0.5-1 dB loss of the couplers. From simulations, the relative phase shift across the bandwidth changes from 150° to 200°. The relatively large phase error is nevertheless compensated in calibration by properly selecting $\Delta\varphi_I$, $\Delta\varphi_Q$, as discussed in the previous section. The signals $S_{B,I/Q}$ feed a pair of cascode amplifiers with input matching networks MN_1. All the HBTs, with 8 µm x 0.2 µm emitter area, are biased with ≈8 mA from 2 V supply. The feedback inductor $L_f = 55$ pH is added to the common-emitter transistors, Q_1, to boost the gain [65]. The collectors of the common-base devices, Q_2, are shorted to sum the I/Q paths in the current domain. The output network MN_2 performs a step-up transformation of the 50 Ω off-chip termination to rise the gain. MN_1, MN_2 absorb device parasitics and emulate the behavior of a doubly-tuned transformer [66] to extend the bandwidth, leveraging the 4^{th} order network response [61].

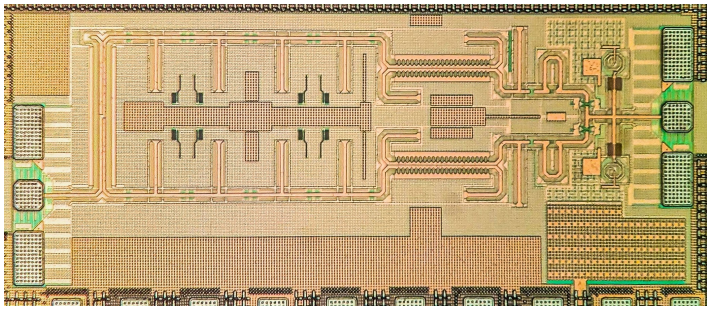


Figure 3.24: Photograph of the realized phase shifter.

3.2.3 Measurement Results

The test-chip, realized in the SiGe BiCMOS 55 nm of STMicroelectronics, is shown in Fig. 3.24, and the core size is 810 x 250 μm^2. The chip is wire-bonded onto a PCB that provides biasing, supply and the digital signals to an on-chip serial interface, used to program the phase shifter. Infinity waveguide 75 µm-pitch GSG probes are employed together with VDI WR6.5-VNAX extension modules to acquire S-Parameters by means of the Agilent E8361C vector network analyzer. A MATLAB routine is used to automate the acquisition of the forward gain (S_{21}, plotted in grey in Fig. 3.25) in all the possible phase shifter configurations. Then, an offline calibration algorithm is applied to select the traces that give the minimum RMS phase error over a target bandwidth, with maximum gain variation within ±1 dB. The procedure is applied within three

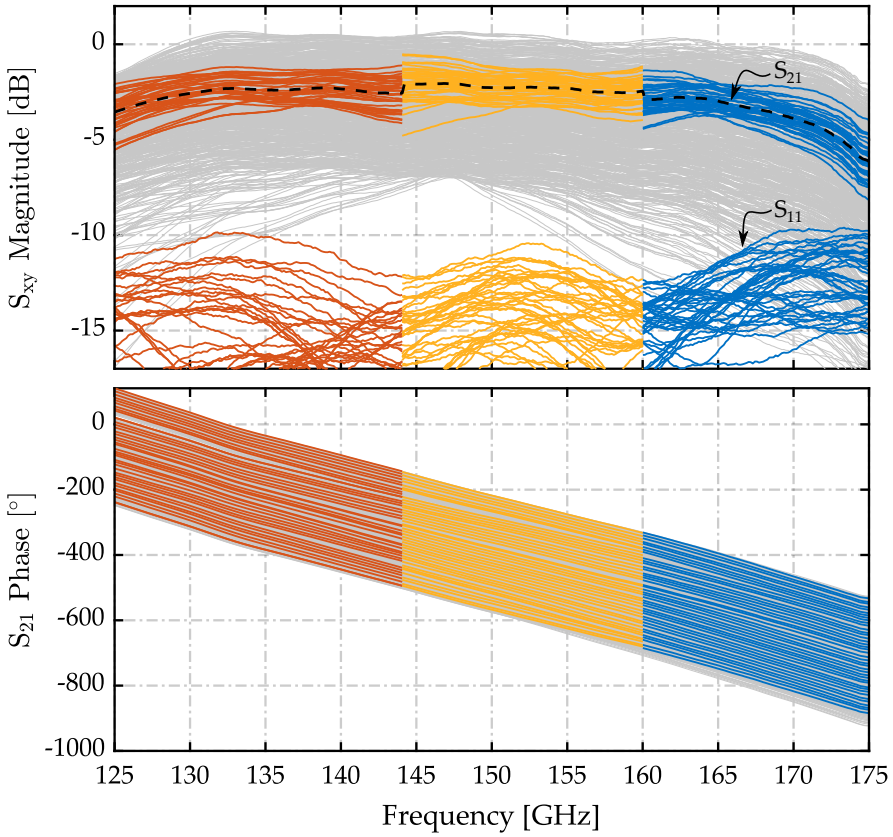


Figure 3.25: Measured S-parameters. Highlighted are the curves selected after calibration.

separate sub-bands, centered at 138 GHz, 152 GHz and 165 GHz, to reduce the RMS errors across a larger bandwidth. The selected S_{21} curves are drawn in red, yellow and blue colors in Fig. 3.25. Fig. 3.26 shows the polar plot (with magnitude expressed in linear scale and normalized to the average gain) and the corresponding point-to-point gain variation and phase steps at the three center frequencies. The RMS magnitude and phase errors across frequency are plotted in Fig. 3.27 and are within 0.8 dB and 5°, respectively, across the

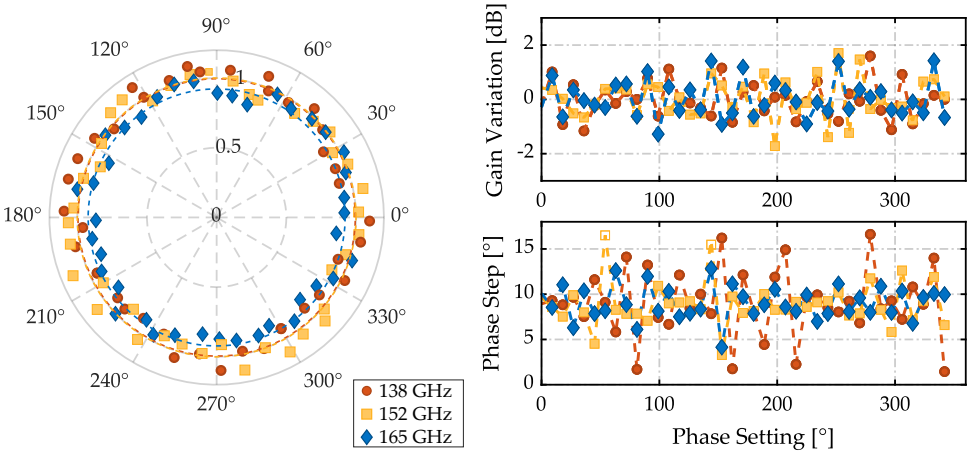


Figure 3.26: Polar plot at the calibration frequencies and corresponding point-to-point gain and phase variation.

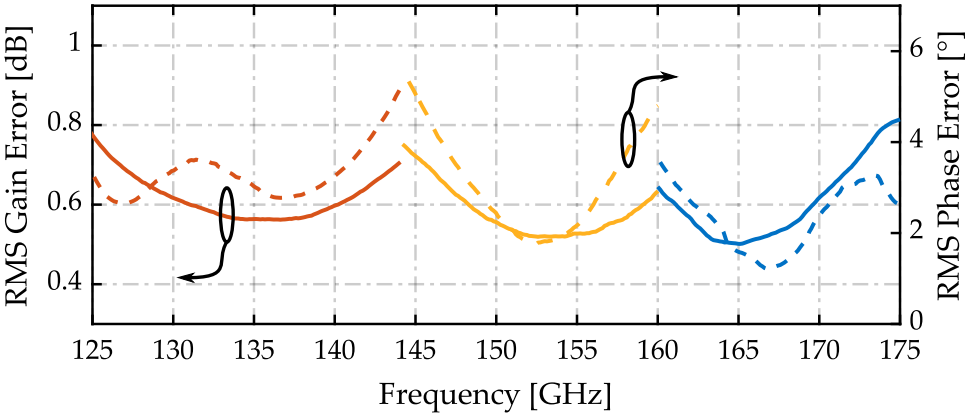


Figure 3.27: Gain (solid) and phase (dashed) RMS errors.

125-170 GHz band.

The gain compression point is measured with an ELVA-1 DPM-06 power meter at three frequency points for 0°-360° phase shift. The results, plotted in Fig. 3.28, prove OP_{1dB} always above 2 dBm. With a power consumption $P_{DC} = 31$ mW, the power efficiency, $\eta = OP_{1dB}/P_{DC}$, is higher than 5%.

Noise figure was not characterized but simulation results shows a NF = [16 - 20] dB over the 360° and frequency ranges. Although all the losses are concentrated at the input, the noise figure is only 2 dB worse than the vector interpolation solution presented before.

The measured results are summarized and compared against previous works in Table 3.4. The fully passive phase shifter in [46] has 1.4 dB higher OP_{1dB}, but with 8.2 dB higher insertion loss and only 10 GHz bandwidth. The proposed phase shifter demonstrates an excellent OP_{1dB}, remarkably higher than active

phase shifters [49]–[51], with the highest power efficiency.

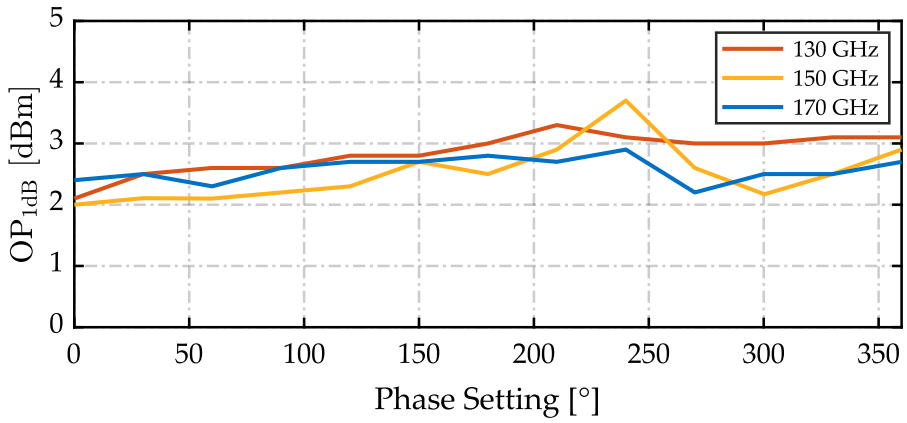


Figure 3.28: Measured OP_{1dB} at three frequencies vs. phase settings.

Table 3.4: Performance summary and comparison.

Reference		This Work	[45]	[46]	[47]	Proposed VI Sec. 3.1.3	[49]	[50]	[52]	[51]
Technology		55 nm SiGe	120 nm SiGe	45 nm RFSOI	130 nm SiGe	55 nm SiGe	55 nm SiGe	55 nm SiGe	55 nm SiGe	130 nm SiGe
Topology		Passive+Buff	RTPS+Buff.	Switched TLine	Switched TLine	Vect. Int.	Vect. Int.	Vect. Int.	Vect. Int.	Vect. Int.
f_0	[GHz]	125 - 170	116 - 128	135 - 145	110 - 170	130 - 175	130 - 175	110 - 145	140 - 160	162 - 190
Gain	[dB]	-2.3	-5.8	-10.5	-21	3.5	-4.5	1.5	-4.5	-6.2
Phase Res.	[°]	9	11.25	11.25	17 - 27	-	-	-	-	-
RMS ϕ_{err}	[°]	5	2.2	1.2	4	5	8	8.5	7.5	8
RMS $Gain_{err}$	[dB]	0.8	0.2	0.5	1	0.8	1.2	1.2	1.4	1
OP_{1dB}	[dBm]	2 - 3.5	-	3.4	-	1.8	-3	-6	-3.7	-27.2
P_{DC}	[mW]	31	30	0	6.22	64	19†	20.3†	50†	12.6†
$\eta@P_{1dB}$	[%]	5.1 - 7.2	-	-	-	2.4	2.8†	1.2†	0.8†	0.02
Core Area	[mm^2]	0.207	0.405	0.04	1.16	0.09	0.09	0.81	0.05	0.07

† Average value on the constant gain circle

3.3 Chapter Summary

This chapter presented two different approaches for building a phase shifter at D-band frequencies with focus on the linearity and efficiency. The first is based on the well known vector interpolation principle, offering high versatility, phase resolution and compact area. However the need for variable gain amplifiers may limit the linearity, thus the efficiency, of the overall phase shifter. This work studied the impact of VGAs AM-AM and AM-PM distortions. Different VGA configurations were compared, finding a preferable solution to optimize the phase shifter distortion. A D-band phase shifter test-chip was then realized in a BiCMOS technology. The issue of the common-mode signal generated by the VGAs was considered in the design and solutions implemented, including a novel current-combining balun which performs 4:1 impedance transformation and high common-mode rejection with equal primary and secondary inductors. The VGAs in the implemented phase shifter can be programmed to operate in the different ways considered in the distortion analysis, allowing to validate the theoretical results with measurements. Using the optimal VGA operation mode, the phase shifter demonstrated gain, bandwidth and phase accuracy comparable or better than state-of-the-art vector interpolation phase shifters, but with superior linearity and power efficiency.
Opposite to the vector interpolation is the phase shifters based on tunable passive networks that notoriously offer higher linearity performance. The approach is well explored at lower frequency, where compact, bidirectional and low loss solutions can be achieved. The task is more challenging at D-band where the quality factor passive components, especially for tunable capacitors, is degraded. A programmable phase shifter architecture is presented to overcome the linearity issue of the vector interpolation scheme, and both the bandwidth and high-insertion-loss limitations of fully-passive solutions. In the proposed architecture, I/Q vectors are shifted with a fine phase-control resolution, passed through 0°/180° phase inversion blocks and finally combined by a pair of amplifiers operated at constant gain for optimal linearity. The relative phase shift between the I and Q vectors is exploited for gain and phase errors corrections, avoiding the need of VGAs. Measurement results on a SiGe BiCMOS test-chip working in D-band compare favorably against previous works, demonstrating a superior OP_{1dB} with double the efficiency of the vector interpolation phase shifter presented before. This comes at the expense of double the area, which may be reduced by optimizing the layout of the passive phase shifting elements. Moreover, the proposed architecture still maintain the versatility and phase resolution of the vector interpolation approach, demonstrating to be a good candidate for high frequency phase shifter designs.

4 Conclusion

This dissertation presented the 3 years research work on building blocks for transceiver front-ends operating in D-band.
The increased free space path loss due to the antenna scaling, the limited output power available from PAs and the degraded sensitivity of receivers due to transistor operating at frequency close to the f_{max}, push the need for phased arrays, which extends the benefits of high directivity antennas, as the increased TX EIRP and RX SNR, to the over-the-air power combining and electronically controlled beam steering. In this framework, SiGe BiCMOS technology represents a good candidate, offering high speed/medium power HBTs along with CMOS logic.

The first part of the work introduced the issue of frequency synthesis at mm-Wave and sub-THz frequencies. A novel frequency doubler architecture was presented offering superior performance in terms of bandwidth, efficiency and rejection of the fundamental frequency. The operation mechanism was tested in K-band, demonstrated a remarkable bandwidth advantage with respect to a conventional mixer based frequency doubler driven by quadrature signals, as well as to the state-of-the-art. The concept was extended at D-band, where we propose a solution to compensate for the unavoidable and not negligible phase shifts introduced by parasitic components, again demonstrating performance comparable or better than state-of-the-art.

The second core activity regarded phase shifters, a fundamental block in phased-array transceivers. The vector interpolation principle was investigated with focus on the linearity performance. A solution was proposed, demonstrating wideband operation with high phase resolution along with high output power and efficiency. To further overcome the limited linearity in the vector interpolation principle, a second solution based on passive phase shifting blocks was proposed. With a low insertion loss, wide bandwidth and a remarkable efficiency $> 5\%$, proves the superior performance against state-of-the-art.

List of Publications

1. L. Piotto, G. De Filippi, D. D. Maistro, S. Erba and A. Mazzanti, “A K-band Gilbert-Cell Frequency Doubler with Self-Adjusted 25% LO Duty-Cycle in SiGe BiCMOS Technology," *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC), Milan, Italy, 2022*.

2. L. Piotto, G. De Filippi, G. Brozzetti, D. D. Maistro, S. Erba and A. Mazzanti, “A 14–32 GHz SiGe-BiCMOS Gilbert-Cell Frequency Doubler With Self-Adjusted Reduced Duty-Cycle Performance Enhancement," *in IEEE Journal of Solid-State Circuits, 2023*.

3. L. Piotto, G. De Filippi, A. Bilato and A. Mazzanti, “A 20 mW 130-175 GHz Phase Shifter with Meandered λ/2 TLINEs in BiCMOS 55 nm," *ESSCIRC 2023 - IEEE 49th European Solid State Circuits Conference (ESSCIRC), Lisbon, Portugal, 2023*.

4. L. Piotto, G. De Filippi, M. M. Pirbazari and A. Mazzanti, “Compact D-Band Passive Phase Shifters with Fine and Coarse Control Steps in BiCMOS-55nm Technology", *2024 IEEE 24nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), San Antonio, TX, USA, 2024*.

5. L. Piotto, G. De Filippi and A. Mazzanti, “110-170 GHz 25% Duty-cycle Gilbert-cell Frequency Doubler with 6.5 dBm Peak Output Power in BiCMOS 55 nm Technology," *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Washington, USA, 2024*.

6. L. Piotto, G. De Filippi, A. Bilato and A. Mazzanti, “AM-AM and AM-PM Distortion in D-Band BiCMOS Vector-Interpolation Phase Shifters," ***submitted*** *to IEEE Journal of Solid-State Circuits, 2024*.

7. G. De Filippi, L. Piotto, A. Bilato and A. Mazzanti, “A SiGe BiCMOS D-Band LNA with Gain Boosted by Local Feedback in Common-Emitter Transistors," *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Diego, CA, USA, 2023*.

8. G. De Filippi, L. Piotto, A. Bilato and A. Mazzanti, “A D-Band Low-Noise-Amplifier in SiGe BiCMOS with Broadband Multi-Resonance Matching Networks," *2023 18th European Microwave Integrated Circuits Conference (EuMIC), Berlin, Germany, 2023*.

9. G. De Filippi, L. Piotto, M. M. Pirbazari and A. Mazzanti, “D-Band RX Front-End with a 0°-360° Phase Shifter Based on Programmable Passive Networks in SiGe-BiCMOS" - *RWW Mini Special Issue of IEEE Transactions on Microwave Theory and Techniques, 2024*.

10. G. De Filippi, L. Piotto, M. Bruccoleri and A. Mazzanti, “A 170 GHz 5.5 dB NF Low-Noise-Amplifier in 55 nm SiGe BiCMOS," *19th International Conference On PhD Research in Microelectronics and Electronics (PRIME), Larnaca, Cyprus, 2024*.

11. G. De Filippi, L. Piotto and A. Mazzanti, “A D-Band LNA Exploiting Ultra-Wideband Sixth-Order Matching Networks in SiGe BiCMOS," ***accepted*** *at ESSCIRC 2024 - IEEE 50th European Solid State Circuits Conference (ESSCIRC), Bruges, France, 2024*.

12. L. Serra, G. De Filippi, L. Piotto and A. Mazzanti, “A Biasing Scheme for the Gain Compression Point Optimization of HBT Cascode D-Band LNAs", ***accepted*** *at 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Fort Lauderdale, FL, USA, 2024*.

List of Figures

Bibliography

[1] A. Devices. "E-Band Wireless Radio Links Deliver High Capacity Backhaul Solutions for 5G Networks—Part 1." (2023), [Online]. Available: https://www.analog.com/en/resources/technical-articles/e-band-wireless-radio-links.html.

[2] Huawei. "2022 Microwave Industry White Paper." (2023), [Online]. Available: https://www.huawei.com/en/huaweitech/industry-trends/microwave-industry-2022-whitepaper.

[3] B. Sadhu, X. Gu, and A. Valdes-Garcia, "The more (antennas), the merrier: A survey of silicon-based mm-wave phased arrays using multi-ic scaling," *IEEE Microwave Magazine*, vol. 20, no. 12, pp. 32–50, 2019. DOI: 10.1109/MMM.2019.2941632.

[4] R. Rotman, M. Tur, and L. Yaron, "True time delay in phased arrays," *Proceedings of the IEEE*, vol. 104, no. 3, pp. 504–518, 2016. DOI: 10.1109/JPROC.2016.2515122.

[5] H. Hashemi, T.-s. Chu, and J. Roderick, "Integrated true-time-delay-based ultra-wideband array processing," *IEEE Communications Magazine*, vol. 46, no. 9, pp. 162–172, 2008. DOI: 10.1109/MCOM.2008.4623722.

[6] S. Wang and G. M. Rebeiz, "A 32-Element 28/39 GHz Dual-Band Dual-Beam 5G Phased-Array with 40 dBm EIRP and Simultaneous 64 QAM Operation," in *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, 2022, pp. 940–942. DOI: 10.1109/IMS37962.2022.9865316.

[7] S. Mondal, R. Singh, and J. Paramesh, "A reconfigurable 28/37GHz hybrid-beamforming MIMO receiver with inter-band carrier aggregation and RF-domain LMS weight adaptation," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 72–74. DOI: 10.1109/ISSCC.2018.8310189.

[8] B. Welp, G. Briese, and N. Pohl, "Ultra-Wideband FMCW Radar with over 40 GHz Bandwidth below 60 GHz for High Spatial Resolution in SiGe BiCMOS," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 1255–1258. DOI: 10.1109/IMS30576.2020.9224087.

[9] S. Hansen, C. Bredendiek, G. Briese, and N. Pohl, "A Compact Harmonic Radar System with Active Tags at 61/122 GHz ISM Band in SiGe BiCMOS for Precise Localization," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 1, pp. 906–915, 2021. DOI: 10.1109/TMTT.2020.3026353.

[10] A. Mirbeik-Sabzevari, S. Li, E. Garay, H.-T. Nguyen, H. Wang, and N. Tavassolian, "Synthetic Ultra-High-Resolution Millimeter-Wave Imaging for Skin Cancer Detection," *IEEE Transactions on Biomedical Engineering*, vol. 66, no. 1, pp. 61–71, 2019. DOI: 10.1109/TBME.2018.2837102.

[11] J. Nehring, M. Schütz, M. Dietz, *et al.*, "Highly Integrated 4–32-GHz Two-Port Vector Network Analyzers for Instrumentation and Biomedical Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 229–244, 2017. DOI: 10.1109/TMTT.2016.2616873.

[12] A. Franceschin, F. Padovan, R. Nonis, and A. Bevilacqua, "On the Optimal Operation Frequency to Minimize Phase Noise in Integrated Harmonic Oscillators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 5, pp. 657–661, 2018. DOI: 10.1109/TCSII.2018.2822483.

[13] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, "Injection-Locked CMOS Frequency Doublers for μ-Wave and mm-Wave Applications," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, 2010. DOI: 10.1109/JSSC.2010.2049780.

[14] M. M. Pirbazari and A. Mazzanti, "High Gain 130-GHz Frequency Doubler with Colpitts Output Buffer Delivering Pout up to 8 dBm with 6% PAE in 55-nm SiGe BiCMOS," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 36–39, 2021. DOI: 10.1109/LSSC.2021.3053314.

[15] S. Hara, T. Sato, R. Murakami, K. Okada, and A. Matsuzawa, "60 GHz injection locked frequency quadrupler with quadrature outputs in 65 nm CMOS process," in *2009 Asia Pacific Microwave Conference*, 2009, pp. 2268–2271. DOI: 10.1109/APMC.2009.5385434.

[16] J.-J. Hung, T. Hancock, and G. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 2, pp. 754–761, 2005. DOI: 10.1109/TMTT.2004.840615.

[17] I. Ju, C. D. Cheon, and J. D. Cressler, "A Compact Highly Efficient High-Power Ka-band SiGe HBT Cascode Frequency Doubler with Four-Way Input Transformer Balun," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 6, pp. 2879–2887, 2018. DOI: 10.1109/TMTT.2018.2811494.

[18] S. Vehring and G. Boeck, "Truly Balanced K-Band Push-Push Frequency Doubler," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2018, pp. 348–351. DOI: 10.1109/RFIC.2018.8428966.

[19] P.-H. Tsai, Y.-H. Lin, J.-L. Kuo, Z.-M. Tsai, and H. Wang, "Broadband Balanced Frequency Doublers with Fundamental Rejection Enhancement Using a Novel Compensated Marchand Balun," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 1913–1923, 2013. DOI: 10.1109/TMTT.2013.2255618.

[20] S. Li, T. Chi, T.-Y. Huang, M.-Y. Huang, D. Jung, and H. Wang, "A Buffer-Less Wideband Frequency Doubler in 45-nm CMOS-SOI with Transistor Multiport Waveform Shaping Achieving 25% Drain Efficiency and 46–89 GHz Instantaneous Bandwidth," *IEEE Solid-State Circuits Letters*, vol. 2, no. 4, pp. 25–28, 2019. DOI: 10.1109/LSSC.2019.2918943.

[21] M. M. Pirbazari and A. Mazzanti, "E-Band Frequency Sextupler with >35 dB Harmonics Rejection Over 20 GHz Bandwidth in 55 nm BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 7, pp. 2155–2166, 2022. DOI: 10.1109/JSSC.2022.3146730.

[22] V. Puyal, A. Konczykowska, P. Nouet, *et al.*, "DC-100-GHz frequency doublers in InP DHBT technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 4, pp. 1338–1344, 2005. DOI: 10.1109/TMTT.2005.845766.

[23] L. Vera and J. R. Long, "A DC-100 GHz Active Frequency Doubler with a Low-Voltage Multiplier Core," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 1963–1973, 2015. DOI: 10.1109/JSSC.2015.2443372.

[24] J. Kaukovuori, K. Stadius, J. Ryynanen, and K. A. I. Halonen, "Analysis and Design of Passive Polyphase Filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3023–3037, 2008. DOI: 10.1109/TCSI.2008.917990.

[25] J. Wan, Z. Chen, Q. An, and X. Wang, "A Truly Balanced Q-Band CMOS Frequency Doubler Based on Hybrid Quadrature Coupler," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 2, pp. 165–167, 2017. DOI: 10.1109/LMWC.2016.2646909.

[26] L. Piotto, G. De Filippi, D. D. Maistro, S. Erba, and A. Mazzanti, "A K-band Gilbert-Cell Frequency Doubler with Self-Adjusted 25% LO Duty-Cycle in SiGe BiCMOS Technology," in *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, 2022, pp. 389–392. DOI: 10.1109/ESSCIRC55480.2022.9911526.

[27] L. Piotto, G. De Filippi, G. Brozzetti, D. D. Maistro, S. Erba, and A. Mazzanti, "A 14–32 GHz SiGe-BiCMOS Gilbert-Cell Frequency Doubler With Self-Adjusted Reduced Duty-Cycle Performance Enhancement," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 3, pp. 878–888, 2024. DOI: 10.1109/JSSC.2023.3313501.

[28] L. Piotto, G. De Filippi, and A. Mazzanti, "110-170GHz 25% Duty-cycle Gilbert-cell Frequency Doubler with 6.5dBm Peak Output Power in BiCMOS 55nm Technology," *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2024.

[29] F. Starzer, H. P. Forstner, L. Maurer, and A. Stelzer, "77 GHz Radar Transmitter with PLL Based on a Sub-Harmonic Gilbert Frequency Doubler," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 8, pp. 539–541, 2014. DOI: 10.1109/LMWC.2014.2321227.

[30] M. Frounchi, S. G. Rao, and J. D. Cressler, "A Kα-Band SiGe Bootstrapped Gilbert Frequency Doubler with 26.2% PAE," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 12, pp. 1122–1124, 2018. DOI: 10.1109/LMWC.2018.2877198.

[31] J. Li, Y.-Z. Xiong, W. L. Goh, and W. Wu, "A 27–41 GHz Frequency Doubler with Conversion Gain of 12 dB and PAE of 16.9%," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 8, pp. 427–429, 2012. DOI: 10.1109/LMWC.2012.2205228.

[32] Y. Gong, J. Chen, L. Du, *et al.*, "An Ultra-Low Power K band Balanced Frequency Doubler with a Novel Current-reused Structure," in *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 2021, pp. 443–446. DOI: 10.1109/ESSCIRC53450.2021.9567776.

[33] K.-H. Lu, J.-J. Huang, W.-C. Chen, H.-Y. Chang, and Y.-C. Wang, "A K-Band Frequency Doubler in 0.15 − µm GaAs pHEMT with an Autonomous Circuit for Stability Analysis," in *2018 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2018, pp. 1–3. DOI: 10.1109/RFIT.2018.8524108.

[34] G.-Y. Chen, Y.-L. Yeh, H.-Y. Chang, and Y.-M. Hsin, "A ka-band broadband active frequency doubler using CB-CE balanced configuration in 0.18 µm SiGe BiCMOS process," in *2012 IEEE/MTT-S International Microwave Symposium Digest*, 2012, pp. 1–3. DOI: 10.1109/MWSYM.2012.6258269.

[35] Z. Wang, K. Ma, Z. Ma, H. Fu, and J. Xu, "A 20.7–43.8-Ghz Low Power Reconfigurable ×2/× 3 Frequency Multiplier for Multiple 5G-mm-Wave Bands," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 8, pp. 2348–2361, 2022. DOI: 10.1109/JSSC.2022.3166636.

[36] U. J. Lewark, S. Diebold, S. Wagner, *et al.*, "A Miniaturized Unit Cell for Ultra-Broadband Active Millimeter-Wave Frequency Multiplication," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1343–1351, 2014. DOI: 10.1109/TMTT.2014.2318272.

[37] C. Coen, S. Zeinolabedinzadeh, M. Kaynak, B. Tillack, and J. D. Cressler, "A highly-efficient 138–170 GHz SiGe HBT frequency doubler for power-constrained applications," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2016, pp. 23–26. DOI: 10.1109/RFIC.2016.7508241.

[38] S. G. Rao, M. Frounchi, and J. D. Cressler, "Triaxial Balun With Inherent Harmonic Reflection for Millimeter-Wave Frequency Doublers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2822–2831, 2021. DOI: 10.1109/TMTT.2021.3061092.

[39] Y. Li, W. L. Goh, and Y.-Z. Xiong, "A Frequency Doubler/Modulator With 4.5 dBm Output Power at 170 GHz Using SiGe HBTs," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 3, pp. 181–183, 2015. DOI: 10.1109/LMWC.2015.2390534.

[40] M. Mock, I. K. Aksoyak, and A. C. Ulusoy, "A High-Efficiency D-Band Frequency Doubler in 22-nm FDSOI CMOS," in *2022 17th European Microwave Integrated Circuits Conference (EuMIC)*, 2022, pp. 272–275. DOI: 10.23919/EuMIC54520.2022.9923533.

[41] Z. Yang, K. Ma, F. Meng, and B. Liu, "A 120-GHz Class-F Frequency Doubler With 7.8-dBm Pout in 55-nm Bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 8, pp. 2173–2188, 2023. DOI: 10.1109/JSSC.2023.3253287.

[42] M. Abbasi, R. Kozhuharov, C. Karnfelt, *et al.*, "Single-Chip Frequency Multiplier Chains for Millimeter-Wave Signal Generation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3134–3142, 2009. DOI: 10.1109/TMTT.2009.2034344.

[43] T. Maiwald, T. Li, G.-R. Hotopan, *et al.*, "A Review of Integrated Systems and Components for 6G Wireless Communication in the D-Band," *Proceedings of the IEEE*, vol. 111, no. 3, pp. 220–256, 2023. DOI: 10.1109/JPROC.2023.3240127.

[44] L. Piotto, G. D. Filippi, M. M. Pirbazari, and A. Mazzanti, "Compact D-Band Passive Phase Shifters with Fine and Coarse Control Steps in BiCMOS-55nm," in *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2024, pp. 25–28. DOI: 10.1109/SiRF59913.2024.10438529.

[45] R. B. Yishay and D. Elad, "D-Band 360° Phase Shifter with Uniform Insertion Loss," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 868–870. DOI: 10.1109/MWSYM.2018.8439838.

[46] M. Abbasi and W. Lee, "A Low-Loss Passive D-Band Phase Shifter for Calibration-Free, Precise Phase Control," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 5, pp. 1371–1380, 2024. DOI: 10.1109/JSSC.2024.3357738.

[47] A. Karakuzulu, M. H. Eissa, D. Kissinger, and A. Malignaggi, "Broadband 110 - 170 GHz True Time Delay Circuit in a 130-nm SiGe BiCMOS Technology," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 775–778. DOI: 10.1109/IMS30576.2020.9223843.

[48] Y. Kim, S. Kim, I. Lee, M. Urteaga, and S. Jeon, "A 220–320-GHz Vector-Sum Phase Shifter Using Single Gilbert-Cell Structure With Lossy Output Matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 1, pp. 256–265, 2015. DOI: 10.1109/TMTT.2014.2376515.

[49] L. Piotto, G. D. Filippi, A. Bilato, and A. Mazzanti, "A 20mW 130-175GHz Phase Shifter with Meandered λ/2 TLINEs in BiCMOS 55nm," in *ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, 2023, pp. 65–68. DOI: 10.1109/ESSCIRC59616.2023.10268727.

[50] A. Moradinia, Y. A. Mensah, W. Lim, S. Lee, and J. D. Cressler, "A 110–145-GHz SiGe HBT D-Band Vector Modulator Phase Shifter Utilizing Differential Quadrature Delay Lines," *IEEE Solid-State Circuits Letters*, vol. 6, pp. 117–120, 2023. DOI: 10.1109/LSSC.2023.3267715.

[51] P. V. Testa, C. Carta, and F. Ellinger, "A 160–190-GHz Vector-Modulator Phase Shifter for Low-Power Applications," *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 1, pp. 86–89, 2020. DOI: 10.1109/LMWC.2019.2952766.

[52] D. d. Rio, I. Gurutzeaga, R. Berenguer, I. Huhtinen, and J. F. Sevillano, "A Compact and High-Linearity 140–160 GHz Active Phase Shifter in 55 nm BiCMOS," *IEEE Microwave and Wireless Components Letters*, vol. 31, no. 2, pp. 157–160, 2021. DOI: 10.1109/LMWC.2020.3037162.

[53] P. V. Testa, C. Carta, and F. Ellinger, "A 140–210 GHz Low-Power Vector-Modulator Phase Shifter in 130nm SiGe BiCMOS Technology," in *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 530–532. DOI: 10.23919/APMC.2018.8617631.

[54] M. Elkhouly, M. J. Holyoak, D. Hendry, *et al.*, "D-band Phased-Array TX and RX Front Ends Utilizing Radio-on-Glass Technology," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 91–94. DOI: 10.1109/RFIC49505.2020.9218409.

[55] T. Maiwald, K. Kolb, J. Potschka, M. Dietz, and R. Weigel, "Towards Broadband D-Band Wireless Communication Systems using Beam Steering in SiGe BiCMOS Technology," in *2021 13th Global Symposium on Millimeter-Waves and Terahertz (GSMM)*, 2021, pp. 1–3. DOI: 10.1109/GSMM53250.2021.9512012.

[56] H. Chireix, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, 1935.

[57] E. Rahimi, J. Zhao, F. Svelto, and A. Mazzanti, "High-Efficiency SiGe-BiCMOS E -Band Power Amplifiers Exploiting Current Clamping in the Common-Base Stage," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2175–2185, 2019. DOI: 10.1109/JSSC.2019.2909475.

[58] D. Ozis, J. Paramesh, and D. J. Allstot, "Integrated Quadrature Couplers and Their Application in Image-Reject Receivers," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1464–1476, 2009. DOI: 10.1109/JSSC.2009.2016705.

[59] P. Stärke, V. Rieß, C. Carta, and F. Ellinger, "Continuous 360° Vector Modulator with Passive Phase Generation for 140 GHz to 200 GHz G-Band," in *2019 12th German Microwave Conference (GeMiC)*, 2019, pp. 240–243. DOI: 10.23919/GEMIC.2019.8698129.

[60] E. Ozturk, H. J. Ng, W. Winkler, and D. Kissinger, "0.1mm^2 SiGe BiCMOS RX / TX channel front-ends for 120 GHz phased array radar systems," in *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2017, pp. 50–53. DOI: 10.1109/SIRF.2017.7874368.

[61] A. Mazzanti and A. Bevilacqua, "Second-Order Equivalent Circuits for the Design of Doubly-Tuned Transformer Matching Networks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4157–4168, 2018. DOI: 10.1109/TCSI.2018.2846029.

[62] K.-J. Koh and G. M. Rebeiz, "0.13-µm CMOS Phase Shifters for X-, Ku-, and K-Band Phased Arrays," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2535–2546, 2007. DOI: 10.1109/JSSC.2007.907225.

[63] W. Lee, J. Tao, J. S.-C. Chien, and J. F. Buckwalter, "A 5.4 mW G-Band Phase Shifter in 90-nm SiGe HBT With One-Hot Encoding," *IEEE Solid-State Circuits Letters*, vol. 6, pp. 189–192, 2023. DOI: 10.1109/LSSC.2023.3294172.

[64] S. Afroz and K.-J. Koh, "A D -Band Two-Element Phased-Array Receiver Front End With Quadrature-Hybrid-Based Vector Modulator," *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 2, pp. 180–182, 2018. DOI: 10.1109/LMWC.2018.2792150.

[65] G. De Filippi, L. Piotto, A. Bilato, and A. Mazzanti, "A SiGe BiCMOS D-Band LNA with Gain Boosted by Local Feedback in Common-Emitter Transistors," in *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2023, pp. 133–136.

[66] G. De Filippi, L. Piotto, A. Bilato, and A. Mazzanti, "A D-Band Low-Noise-Amplifier in SiGe BiCMOS with Broadband Multi-Resonance Matching Networks," in *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, 2023, pp. 382–385.