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Intentional and Unintentional Light Emission Diode in Power Electronics applications

DOCTORAL THESIS

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Introduction

The phenomenon of light emission in a P-N junction is due to the recombination of electrons and holes in the junction. This light emission phenomenon has been widely used in power electronics applications. Among them, it is worth remembering the use of the light-emitting diode (LED) as a source of light in lighting system applications. In this perspective, LEDs technology has been widely studied as an “Intentional” source of light in Power Electronics.

In such a context, a LED light bulb can be assumed as a combination of LED semiconductor materials and a ballast circuit, where the LED driver circuit plays a fundamental role from a power quality point of view. In fact, the driver controls the input current of the LED light bulb that must be compliant with the standards and regulations concerning currents harmonic. Furthermore, the whole lighting system must meet the standards. In this perspective, a sufficient power factor (PF) must be guarantee thanks to a proper design of the lighting system, especially when a very huge number of lamps are used. Hence, the electrical model of each light bulb is fundamental to foresee the effects of different design configurations.

In this perspective, my research activity has been firstly focused on providing such a generic circuit model of LED light bulbs which is useful at the design stage of the lighting system to guarantee a high power factor. The proposed circuit model is able to emulate the current drawn of any LED light bulbs, whatever lamp driver is used. The procedure and equations to obtain the components of the equivalent circuit of the LED light bulbs have been provided. It is worth highlighting that such a procedure enables to obtain the model of any LED light bulbs available on the market without the knowledge of its inner components (driver, LED package, and so on). The components in the model of a generic lamp can be obtained by a few simple current measurements to be performed at the lamp terminals. These parameters are the coefficients of the functions obtained by linear or polynomial interpolation of the *rms* of the current harmonics. The model validation has confirmed the effectiveness and robustness of the proposed solution.

In the context of LED light bulbs, my research activity has also focused on the study of the LED drivers topologies. Among the various LED drivers available on the market for integrated lighting applications, the single-stage discontinuous current conduction mode

flyback PFC converter has been revealed as the preferred choice in order to achieve a high PF with a good cost-performance ratio. Notwithstanding the use of a suitable control method that enables a high PF, different inherent causes of distortion in the input current, due to the power processing mechanism of the High PF QR flyback converter, have been found. Hence, the different issues due to the correlation of these causes, which are the ringing current, the crossover distortion due to transformer leakage inductance, and crossover distortion due to the input storage capacitor have been widely studied. It is worth noting that the problem of the input current distortion caused by the ringing current has been studied for the first time in a QR flyback. Moreover, the crossover distortion due to the input storage capacitor in the case of a Hi-PF flyback LED driver has never been treated in literature. Finally, some practical design guidelines for mitigating the inherent causes of distortion of the input current in a Hi-PF QR flyback driver for LED applications have been provided.

An emerging application of the light emission in a P-N junction is the use of light emission from the body diode of a SiC device for condition monitoring (CM). In this perspective, the LED is an “unintentional” source of light in Power Electronics.

More specifically, the reliability of power electronics devices is raising a great interest, especially, in some critical applications. In this perspective, several condition monitoring methods have been widely proposed so far. Among them, the light emission phenomenon from the body diode of a SiC device has been gained more interest in the last decade. In detail, the electroluminescence phenomenon refers to the photoemission from a SiC material and it is related to its intrinsic body diode. The light brightness in the SiC intrinsic body diode depends on the junction temperature, where the light intensity decrease at high temperature. Thus, the electroluminescence phenomenon can be a suitable indicator of the temperature of the SiC MOSFET chip during a general power converter application.

In this perspective, my research activity has been firstly focused on the description of several CM methods adopted for power devices. Moreover, the intrusiveness of these condition monitoring methods has been also deeply investigated for the first time. More specifically, three intrusiveness criteria have been considered at the device level, converter operation level, and conversion system level. Then, three figures of merit (FOM) have been accordingly considered and assigned to all the condition monitoring methods by means of a mark based rule. Finally, a unique single-value figure of merit has been obtained from the product of the three figures of merit. An application-based FOM that accounts for the importance of the different intrusiveness criteria in a given application has been also proposed. The use of a single value to compare the different CM methods is the main strength of these overall FOMs but they do not provide a fixed value due to the subjective of the marks. On the other hand, the rank of the CM methods according to an intrusiveness criterion is almost unbiased. Therefore, a strategy to compare the CM methods according to the rank instead of the mark is proposed by borrowing some reasoning from the Pareto optimality. Such an approach has revealed that the CM

methods adopting, respectively, Integrated photodiode, IR Camera, Acoustic, and two thermo-sensitive electrical parameters (turn on-off delay time and peak gate current) are the best ones in terms of intrusiveness, and they are equivalent each other from the Pareto optimality point of view. Finally, the Integrated photodiode and the IR Camera CM methods are the less intrusive according to the overall FOM.

Therefore, these results have highlighted that the use of the Integrated photodiode is one of the best choices, and considering the SiC MOSFET intrinsic diode as an unintentional diode, a new CM method adopting the Integrated photodiode in a SiC MOSFET module has been devised. More specifically, a non-invasive temperature sensing method for high-voltage SiC MOSFET chips based on the measurement of light emission during reverse conduction has been proposed. The method is based on a compact sensing circuit that can be easily embedded in the package, allowing online temperature estimation. The effectiveness of the circuit has been confirmed by the analysis of a commercial SiC power module. It is worth noting that the proposed temperature sensing strategy is fast, inexpensive, accurate, and of course, non-invasive.

By summing up, this work has been focused on the application of “intentional” and “unintentional” light emission diode in Power Electronics. The first, second, and third chapters have been focused on the use of commercial LED light bulbs. More specifically, Chapter 1 describes the power quality issues and the drivers adopted to mitigate them. Chapter 2 reports the analysis of the intrinsic causes of current distortion in high power factor Quasi-Resonant flyback and proposes some mitigation guidelines. Then, in Chapter 3, a circuit model of a generic LED light bulb has been proposed with the aim to emulate the current drawn from a generic LED light bulb. Chapter 4 focuses on the advantages (in terms of intrusiveness) of using unintentional light emission diode for condition monitoring of power devices. Finally, Chapter 5 describes the proposed innovative condition monitoring method based on the integration of a photodiode to correlate the “unintentional” light emission of a SiC material to the temperature of the device.

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Chapter 1
Current harmonics due to LED light bulbs: mitigation and modeling

1.1 Introduction

The lighting systems, both in-home and business environments, may take up over 15% of overall electrical consumption [1-3]. Hence, the lighting system designers always search for applying new technologies to obtain savings, thus reducing the waste of electrical energy and the bill. Nowadays, a huge quantity of lighting systems is widespread in the marketplace, where different types of lamps are used. Light bulbs may be divided in incandescent, compact fluorescent lamp (CFL), high-intensity discharge, halogen, LED, and so on [4-5]. Among them, the LED light bulbs technology is today in a good stage of trade-off for cost, lifetime, and efficiency in the case of lighting applications. Moreover, LED light bulbs are expected to provide in future more lumens per watt in comparison to today technology [6]. The LED technology presents the additional advantage of being free from the toxic substances contained in some CFL, which may cause pollution issues [7].

Generally speaking, a LED light bulb can be thought of as a combination of LED semiconductor materials and a driver circuit. The choice of the LED driver circuit plays a fundamental role from a power quality point of view. In fact, the driver controls its own input current and the LED output current. Consequently, it must guarantee a high power factor (PF), which means a displacement power factor next to one and an input current with low total harmonic distortion (THD) [8-9]. Actually, the LED light bulbs must comply with the national and international standards and regulations concerning harmonic currents, such as the standard IEEE-Std-519 and the IEC 61000-3-2.

The needed to ensure a high power factor is further significant in the case of the design of a lighting system, especially when a very huge number of lamps are used. In this perspective, the electrical model of each light bulb is fundamental to foresee the effects of different design configurations. An incandescent lamp typically consists of a glass enclosure containing a tungsten filament that produces light at a given temperature reached

due to the flowing of the current and, consequently, it can be simply modeled by a resistor. Differently, the equivalent electrical model of a LED light bulb is not easy to define, due to the converters inside the lamp as well as due to the control technique used to obtain constant current on the diode light engine [10].

The following chapter has been organized into two main parts: firstly, various topologies of passive and switching LED drivers have been described and classified. More specifically, the passive drivers are simpler and more reliable and they operate at the line frequency. They do not provide any active control, so a significant current ripple can occur. The switching drivers can strongly reduce the current distortion and improve the PF with the additional advantage of being suitable for high-frequency operations, thus enabling reduced size. On the other hand, switching LED drivers are less reliable than passive ones. The second part of the chapter has been focused on the current state of the art of the harmonic pollution produced by a LED light bulb. More specifically, it has been widely discussed several key aspects of the optimal lighting system design, and the power quality degradation due to the employment of the LED light bulbs, and more in general, for different kinds of energy-saving lamps (ESLs). From the perspective of an optimal and efficient design, the distorted current drawn by a large number of LED light bulbs and the prediction of the amount of current harmonic that the lamps inject into the power grid have been discussed.

1.2 Brief Overview of LED Driver Topologies

In this section, various topologies of passive and switching LED drivers have been described and classified. The main drawback of passive LED drivers is the low PF that often cannot comply with the standard limit. Instead, switching LED drivers can realize a better output current regulation and higher power density, and they are more capable of satisfying the standard limits. Generally, there is a wide variety of LED driver topologies depending on the different power ranges. Furthermore, the topology of the driver can also be selected according to other requirements, including cost, galvanic isolation, and efficiency.

1.2.1 Passive LED Drivers

Passive LED drivers are characterized by the exclusive use of passive components (e.g., resistors, capacitors, magnetic components). The insertion of an impedance between the ac line and the LED light bulb load to limit the current is mandatory. One of the main drawbacks of these topologies is the low PF and high THD, sometimes not enough to meet the standards [11].

Passive LED drivers can be classified into lossy and lossless impedance driver. The strength and simplicity of the lossy impedance is due to the use of a resistor RL or a linear regulator on the dc side, as depicted in Figure 1:1. In many practical applications, it is widespread the use of a bulky step-down transformer from high to low voltage. It has a two-fold benefit: it reduces the voltage drop on the resistor with an increase of the overall system efficiency and, at the same time, guarantees galvanic isolation. A large electrolytic capacitor C_S is typically used in order to avoid flickering.

A passive driver with a lossless impedance (an inductor, capacitor, or their combinations), usually placed in the ac side to limit the LED output current, is shown in the example of Figure 1:2. An inductor L_{in} is usually adopted with the aim to replace the less efficient and low-frequency transformer. L_{in} usually behaves as an additional input filter (by means of C_{in}) that smooths the input current and leads to advantages such as reducing the input current distortion [12-14]. Instead of using a bulky electrolytic capacitor (E-CAP) that ensures a constant output current, it is often used as a non-E-CAP on the dc side, still achieving a higher PF with respect to the lossy counterpart. This solution can ensure a longer lifetime and small size of the overall system, although there is a small output current ripple in the LED load. Notwithstanding, lossless passive drivers can reach high efficiency, above 90% [13].

They can be easily employed in outdoor applications and they are very cost-effective especially for low-power applications. The main drawbacks of passive LED drivers are their lack of a proper output current control and, an input current THD that does not always meet the standards target.

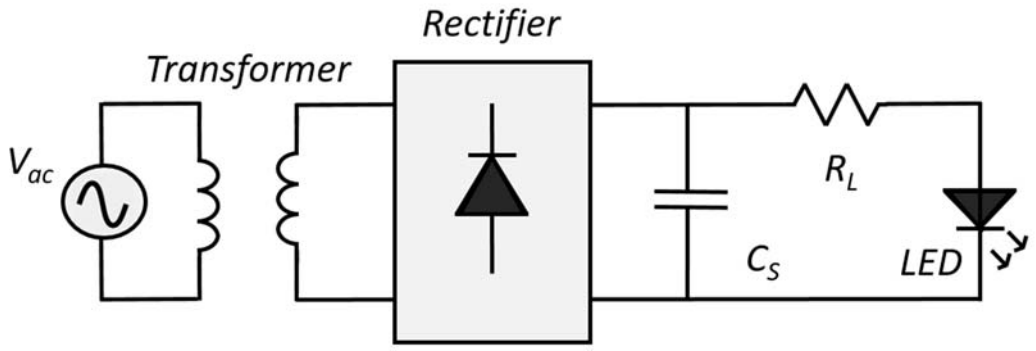


Figure 1:1 Typical application of a passive “lossy” LED driver.

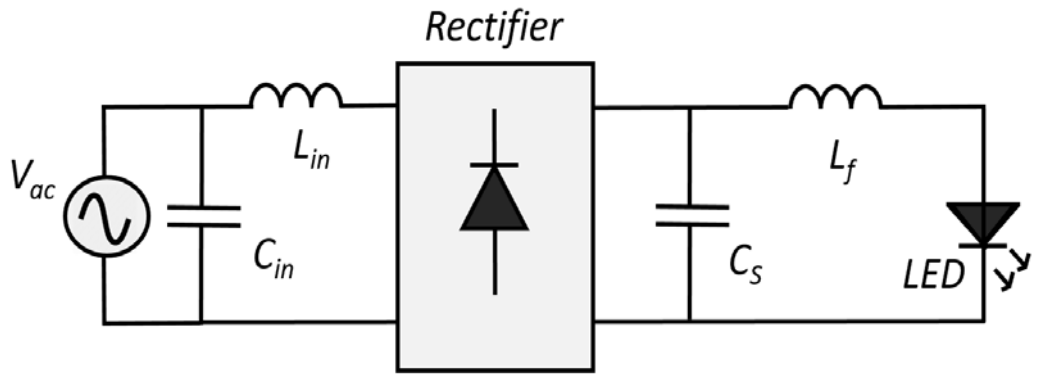
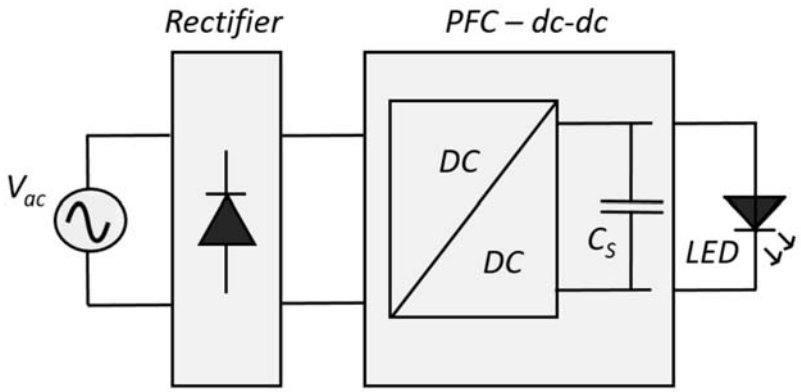


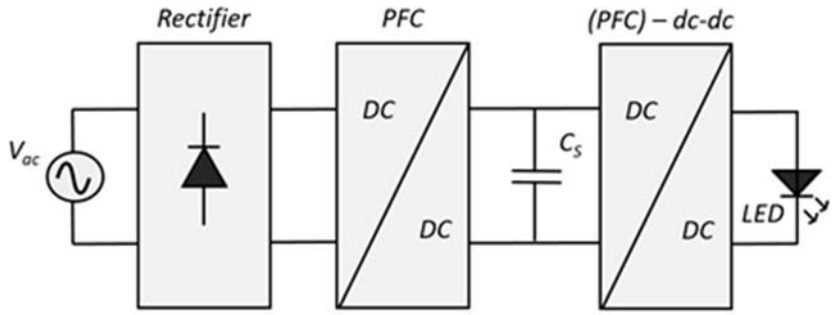
Figure 1:2 Typical application of a passive “lossless” LED driver.

1.2.2 Switching LED driver

Switching LED drivers bring various advantages arising from the use of the switching devices. Moreover, switching LED drivers can embed into a single electronic ballast various functionalities such as circuit fault protection, active and high PFC [15]. They are especially employed in indoor applications since the whole circuit control is compact, reliable, effective with a low and controllable ripple output current. Another strength point of switching LED drivers is their higher efficiency in comparison to the passive ones. Switching LED driver topologies can be classified into two main categories, SS and TS (see Figure 1:3). The SS drivers consist of a single power stage that acts as both a dc-dc regulator and PFC (Figure 1:3(a)) with a storage capacitor C_s. On the other hand, the TS drivers are used for high power applications. The aforementioned drivers comprise two power conversion stages that can perform different functions. In general, the first stage acts as a PFC and the second one as a dc-dc regulator and filter [16], as depicted in Figure 1:3(b).



(a)



(b)

Figure 1:3 (a) SS switching LED driver topology. (b) TS switching LED driver topology.

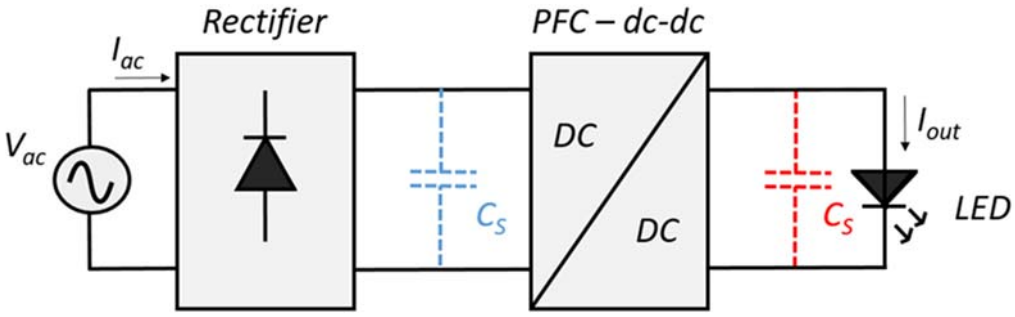


Figure 1:4 Switching -mode single-stage driver: depending on the position of the capacitor Cs the single dc-dc converter can provide both PFC and output current regulation.

In the following, a brief focus on the SS LED drivers with the main advantages of different topologies adopted in the literature.

SS drivers usually have low component count and among them a power switch that controls a power conversion stage. However, it is often difficult for a SS driver to simultaneously ensure good performance in many respects, such as high efficiency, high PF, constant current output, and so on. SS drivers are suitable for low and medium power class applications (below 70 W) where size and cost are usually more critical than PF and efficiency. The storage capacitor is usually placed downstream from the dc-dc converter, which is on the high-frequency side (red capacitor Figure 1:4) to obtain a high PF. Notwithstanding, another approach can be found in some embedded LED drivers where the capacitor is placed on the low-frequency side (blue capacitor Figure 1:4). More specifically, such an approach has been sometimes used in very low power applications (below 5 W) [17]. Indeed, nowadays, in this power range, passive LED drivers are adopted to guarantee an inexpensive cost. Figure 1:5 shows the waveforms of the current drawn by LED light bulbs when the capacitor is placed on the low and high-frequency side. The waveforms confirm that only when the storage capacitor is placed downstream from the dc-dc converter it guarantees PFC. Although the input current drawn by the LED light

bulbs has a better THD when the capacitor is placed at the high-frequency side, a higher output current ripple occurs in comparison with the previous solution (as shown in Figure 1:5(b)). However, the required storage capacitance is not always able to handle both the low and the high-frequency ripple [18].

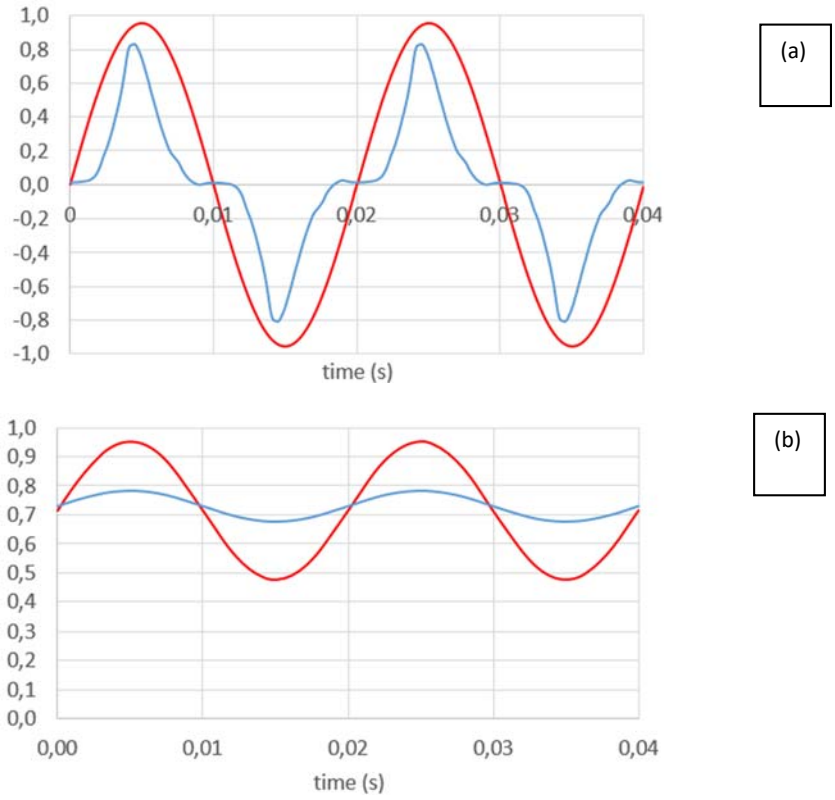


Figure 1:5 Simulation of the current drawn I_{ac} by the LED light bulb (a) and the output LED load current ILED (b). The blue one represents the case when the storage capacitor is directly connected on the low-frequency side and the red one on the high-frequency side.

The SS LED drivers can be roughly classified on the bandwidth of the feedback control systems. In case of a narrow bandwidth (e.g. boost, buck-boost, flyback) the storage capacitor must be located at the output of the converter. Instead, in case of a wide bandwidth systems (e.g. quadratic or S4ICS topologies), the storage capacitor is placed between the two semi-stages. In the following, it has been analyzed the narrow bandwidth systems. In detail, a huge number of conventional LED drivers are widely discussed in literature, such as buck [19-21], buck-boost [22], SEPIC [23-24], flyback [25-26], half-bridge [27-29], push-pull converters [30-31]. Furthermore, PFC can be achieved with valley-fill circuits [32]. Other approaches, as coupled-inductor modified converters [33-36] and valley-fill modified converters [37] show a simple solution to the step-down ratio requirement without compromising the efficiency and system complexity.

The flyback converter has been widely adopted in LED driver lamps because of its simple structure and high PF. One of the strengths is its efficiency that can be improved by using the leakage energy or using soft-switching techniques [38]. In spite of the flyback LED driver has various advantages, in many practical applications, the QR mode operation has become one of the most familiar methods in LED driver applications. It is noteworthy the decrease of switching losses with respect to a flyback converter operated with a fixed frequency. Moreover, the QR driver has an enhanced transient response in DCM operation [39-40] and it may have a smaller EMI filter [41]. In fact, in applications operated from the mains, the switching frequency is modulated at twice the mains frequency due to the voltage ripple appearing across the input capacitance. The switching frequency span depends on the amplitude of this input voltage ripple. This causes the spectrum to be spread over some frequency bands, rather than being concentrated on single frequency values.

In addition, the QR driver has a higher safety degree under short circuit conditions: since the switch is not enabled until the primary windings are fully demagnetized, both the flux runaway and the transformer saturation are not possible. On the other hand, the QR flyback LED driver may have a high ripple output current and high conduction losses in comparison to the fixed frequency one.

It is important to point out that the difference between a DCM flyback and a QR flyback is in the turn-on mechanism. In a DCM flyback converter, the gate driver provides a constant switching frequency, while in a QR flyback it is used a variable frequency where the off-time depends on the resonant valley detection of the drain to source voltage ringing that follows transformer's demagnetization. Figure 1:6 depicts the drain to source voltage waveforms in case of a DCM flyback (Figure 1:6(a)) and a QR flyback (Figure 1:6(b)), thus highlighting the benefit in terms of reduced switching losses.

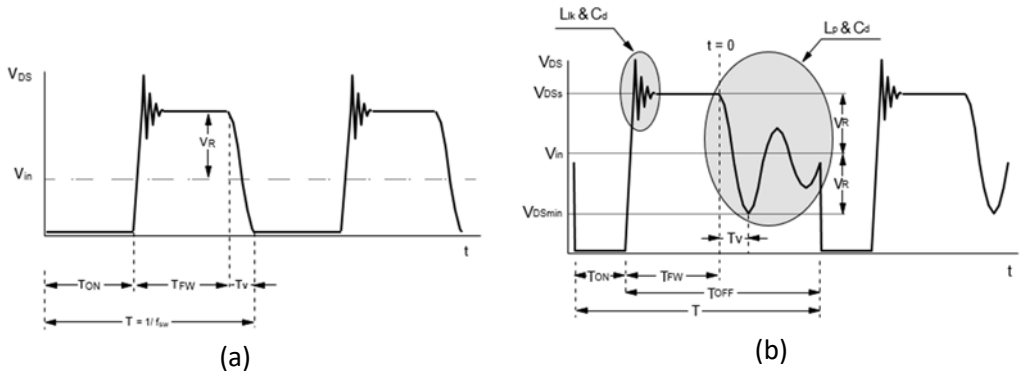


Figure 1:6 Drain to source voltage waveforms for a DCM flyback (a) and a QR flyback (b).

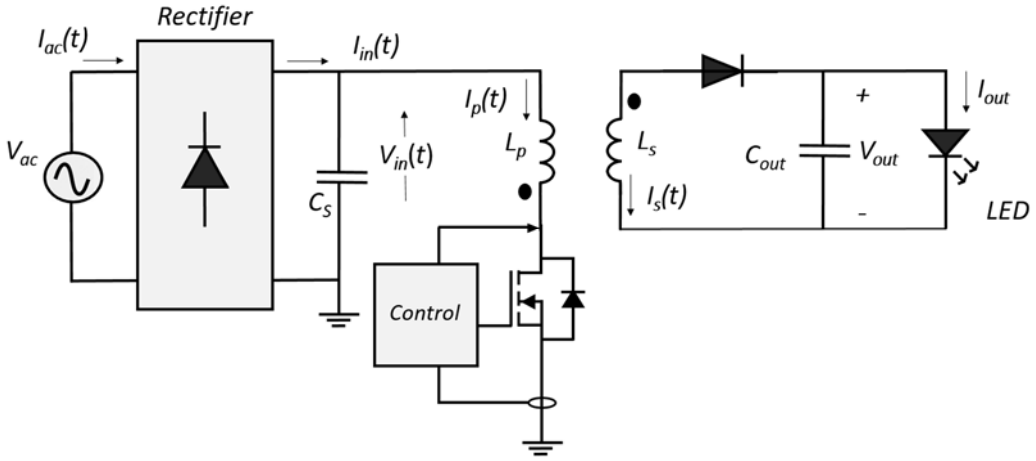


Figure 1:7 QR resonant flyback valley-switching.

A simplified schematic of a QR flyback LED driver (not for Hi-PF applications) is shown in Figure 1:7. The primary current I_p starts to flow into L_p when the power switch is turned on. The voltage at the secondary is such that the diode is reverse biased, hence the capacitance C_{out} supplies the LED string. Once the switch is turned off, the current I_p goes to zero and the voltage across both windings reverses, so that the output diode is forward-biased, the current starts flowing in the secondary winding and C_{out} can be charged by the energy stored in the transformer. It is worth noting that while the current flows on the secondary side, the drain-source voltage is equal to the rectified input $V_{in}(t)$ plus the reflected output voltage V_R at the primary windings. The transformer takes a time T_{FW} to demagnetize, and as soon as the energy transfer is completed, the drain-source voltage starts ringing. The main reason for this energy exchange phenomenon is due to a resonant tank between the inductance L_{pp} and the capacitance C_{pp}. The inductance L_{pp} is the sum between the leakage inductance of the copper paths and the primary winding L_p. The latter is the prevalent contribution, hence L_{pp} can be simply approximated as L_p. The capacitance C_{pp} can be expressed as the sum of the parasitic capacitances on the primary circuit and the capacitances of the secondary circuit referred to as the primary one. The latter is due to the parasitic capacitances of the secondary circuit and the output capacitance C_{out}. The primary circuit capacitance includes various contributions as the output parasitic capacitance (C_{oss}) of the MOSFET, the junction capacitance of the diode, and the package capacitance of the intrawinding capacitance of the transformer plus other stray contributors together and so on [42-45]. C_{oss} is a strongly nonlinear capacitance and, especially in the latest MOSFET generations, it increases dramatically (a hundred times or more) when the drain-source voltage, v_{DS}, falls below few ten volts, i.e. C_{pp} is a function of v_{DS}: C_{pp} (v_{DS}). In the following, this capacitance will be considered constant or, at least, not significantly impacting the overall C_{DS}. Hence, the resonant frequency f_r can be represented as:

$$f_r = \frac{1}{2\pi\sqrt{L_{pp}C_{pp}(v_{DS})}} \approx \frac{1}{2\pi\sqrt{L_pC_{DS}}} \quad (1)$$

In applications, the inductance L_p is measured with an impedance meter or by measuring the *di/dt* when a voltage square wave is applied. While C_{DS} is estimated by (1) from the measurement of the drain-source voltage ringing.

Bearing in mind that in a conventional QR topology is used a feedback loop voltage that controls the average value of the secondary current I_s, the switching frequency is continuously adjusted depending on the output current load. In this way, the switching device turns on when necessary provided that the inner controller is able to detect a valley in the ringing drain-source voltage. The switching period *T* can be expressed as:

$$\begin{cases} T = T_{on} + T_{FW} + T_{ring} \\ T_{ring} = \frac{1}{2}[1 + 2(k-1)]T_r \end{cases} \quad (2)$$

where T_{on} is the ON time of the power switch, T_{FW} is the time interval where the current flows on the secondary side and T_{ring} is the time interval during which the drain-source voltage rings. T_{on} is reduced as the load reduces, hence at very light load the frequency is high. Therefore, the maximum switching frequency imposes a minimum T_{on}. In this case, a further load reduction involves an increment of T_{ring}. In detail, Tring strictly depends on the load level and it is imposed by keeping off the switch for some valley points in the drain-source voltage. In other terms, it depends on the number of the valley points k "skipped" by the controller. More specifically, k increases as the load level decreases. Until T_{on} is greater its minimum value k=1, that is the switch turned on at the first valley on the drain to source voltage waveform (one-half of the resonant period). In the following, the QR mode operation of the converter is defined when k=1.

The reason behind the turn-on during a valley point of the drain-source voltage is the achievement of a lower capacitive switching losses:

$$E_s = \frac{1}{2}C_{DS}{V_{DS}}^2 \quad (3)$$

This mechanism is able to minimize in a significant way the switching losses. It is worth noting that the bill of material of a QR driver contains only a few simple components which implies an inexpensive solution [45-46].

Finally, Figure 1:8 compares the performance between a QR flyback, a buck-boost, and a hybrid solution [31-43] in terms of some key factors. The high step down ability (HSDA)[31-33], efficiency (EFF) [33-36], compact capacitor volume (CAP) [37], cost (COST)[38 -41], and low power range applications (LP) [42] have been taken into account

for the three converters. The comparison highlights the superior performance of the QR flyback converter, which makes it the preferred choice for LED driver applications.

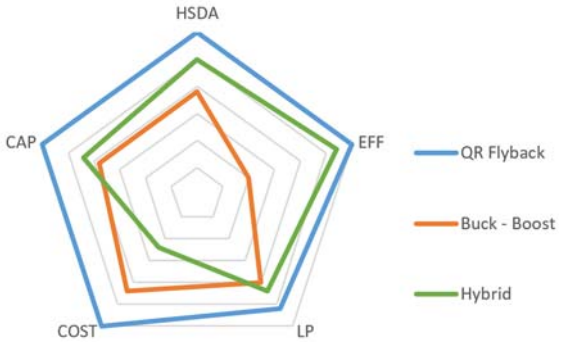


Figure 1:8 Performance of three main SS LED driver topology. High step down ability (HSDA), Efficiency (EFF), reduced capacitor (CAP), Cost (COST), and Low power applications (LP).

1.3 LED light bulbs harmonics in lighting system design

Different analyses of LED light bulbs related to their behavior and efficiency as well as to the driver design have been widely treated [47-49]. The lighting design considers several variables for both indoor and outdoor applications [50]. More specifically the design accounts for the light level and the uniformity of the light pattern, the aesthetic appearance, the economic benefit, the safety, and appropriate equipment [51-52]. Nowadays, with the large use of the energy-saving lamps, that are non-linear loads, the amount of distorted current drawn by the lighting system has to be considered looking to the power quality issues [53]. Such issues have been not considered for many years as each lamp injection is very small but the problem will increase considerably in the next future with the massive use of LED light bulbs. In the past, only the distortion due to the single large harmonic source has been of concern, and the solution was the design of the dedicated filter, or any other harmonic mitigation option, able at meeting the system requirements, and installed across the device terminal [54-55]. The widespread adoption of LED light bulbs can be more deleterious than such a source since a large lighting system with LED light bulbs acts as a large distortion source but it is composed of many distributed harmonic sources with a difficult compensation [56]. The general adoption of the power factor corrector inside the lamps mitigates the problem but it leads to increasing the lamp cost [57]. In literature, the impact on the distribution network of the current harmonic distortion due to the LED light bulbs has already been explored [58-60]. Some works have analyzed the harmonic emissions before and after replacing the existing lamps with the LED ones [61-62]. In [63] the harmonic current from the domestic appliances with the use at the same time of LED light bulbs has been investigated. A comparison of different commercial LED light bulbs, in terms of harmonics and their negative impact on the distribution network, has been presented in [64]. Advanced studies re-

garding the injection of the harmonics have been performed in [65] by means of a simulator that emulates different LED light bulbs, where each lamp has been represented as a simple independent current generator.

Moreover, the harmonic content of a LED light bulbs changes with the variation of the voltage supply. Such a variation is very frequently due to many factors, such as the load profile variation in the nodes of the network, the presence of distributed generators based on intermittent or variable renewable energy sources, the wider use of electric vehicles, the network reconfigurations, the voltage regulation and so on [66-71].

Therefore, a proper design of the lighting system needs to foresee the distortion level due to the whole lighting system for different network voltage. For this purpose, it is necessary to estimate the harmonics due to different LED light bulbs configurations. Conventionally, the fixed current injection method sums the harmonic current magnitudes of each load, but it may significantly overestimate the cumulative harmonic currents produced by the LED light bulbs [72]. It is more appropriate to consider the diversity and attenuation factors because they can predict the behavior of distributed single-phase loads more accurately [73-76].

In this perspective, the PSpice implementation of the LED light bulb model can be adopted to predict the distortion levels at the design stage of the lighting system. Considering that the current harmonic usually significantly increases when LED light bulbs are used, the effect of different configurations can be easily forecasted in view of an optimal design of the lighting system. Figure 1:9 shows the voltage THD level before and after a large LED lighting system turn-on. Before the turn-on, it is expected the voltage THD is under the 8% limit imposed by IEEE-Std-519. More specifically, it is expected that any countermeasures have been realized at the load/generation points along the distribution network to avoid exceeding the limit. The impact of a few lamps on the voltage THD is negligible even when their current is highly distorted, this is due to the low current draw. When a large number of LED light bulbs are adopted, the whole current is not negligible and, consequently, the current drawn from the LED light system may negatively affect the voltage THD. In this context, the optimal design task is finding the combinations of LED light bulbs which led to the minimum overall distorted current even when the single LED light bulb drawn a very distorted current. Such results can be obtained by optimally exploiting the operating principle of the diversity and attenuation factors [72].

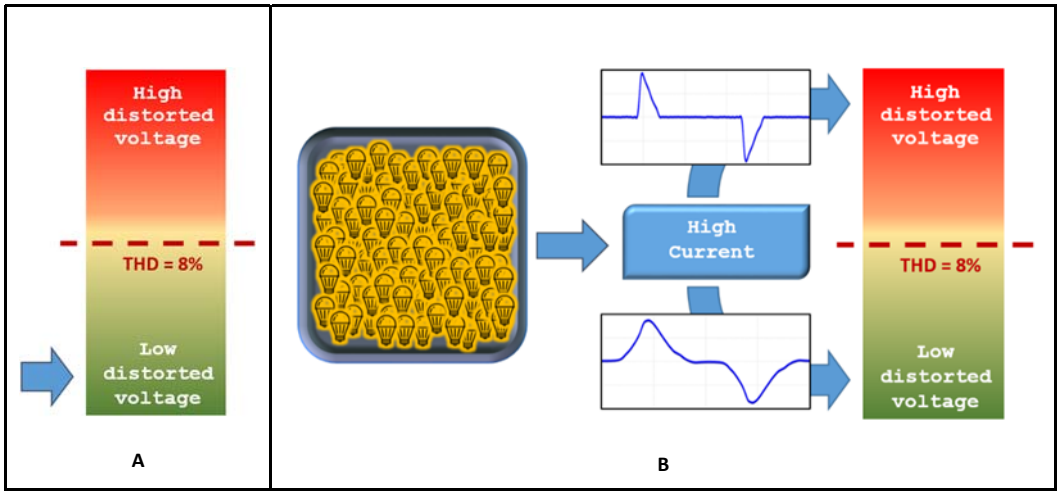


Figure 1:9 Impact of a large LED lighting system on a distribution network complaint with the THD limit of IEEE-Std-519.

Some models devised for CFL could be adopted for LED. More specifically, some researchers have been worked out the behavior of the CFL using an equivalent electrical circuit [77-83]. A common and general model is depicted in Figure 1:10, where the key circuit components are: a diode bridge that rectifies the main voltage, an ac equivalent resistor (R_{ac}), and a DC smoothing electrolytic capacitor (C) supplying the downstream inverter that, in turn, feeds the fluorescent tube. Both the inverter and the fluorescent tube can be modeled as a unique equivalent resistance, R_D, since they behave like a constant load for the DC busbar. In [76-77] an admittance model that depends on some internal parameters (firing and extinction angles) that, in turn, depend on the voltage waveform has been used instead of the general model. A method based on the measurements to obtain harmonic models of power electronic-based home appliances, among which ESLs, has been presented in [76]. In [77] a model based on harmonically coupled admittance matrix used to study harmonics in static converters of ESLs has been proposed. However, the admittance model is valid only in a specific condition of the supply voltage. In [78] a simplified version of the general model is adopted where the AC resistor has been neglected since it presents a small resistance. However, this approximation may lead to not realizable infinite slopes of the ac current rising edge.

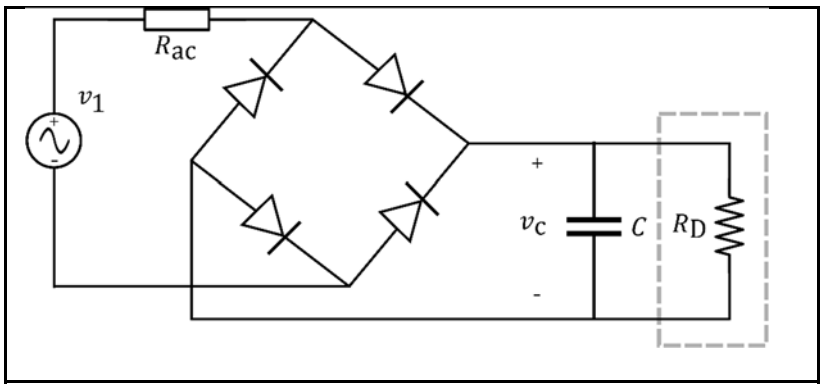


Figure 1:10 Simple equivalent circuit usually adopted in literature for modeling a CFL [76-83]

Similarly, the CFL equivalent circuit considering the AC resistance has been proposed in [79]. The model considers that the behavior of the CFL electrical circuit is similar to the one shown in Figure 1:10. The supply voltage has been modeled with the series of the fundamental and inter-harmonic voltage generators with their network equivalent impedance. In [80] the CFL parameter estimation has been obtained as a detailed analysis of the electrical model developed in [79], where the former used non-linear least-square procedures based on actual measurements. The resolution is based on the Newton method calculating the terms of the Jacobian matrix by finite difference approach. The study of CFL impact and the related model has involved the determination of the CFL equivalent circuit parameters R_{ac}, C, and R_D described previously. It is worth noting that in the literature several procedures are developed to determine the parameters from the supply voltage and ac current measurements [81-82]. Other studies deal with the estimation of other non-linear loads using least-square algorithms [82]. In [83] the parameter estimation of single-phase rectifiers by analyzing several non-linear sets of equations has been performed. More specifically, the former has proposed the two methods to esteem the electrical components in the input rectifier that there are in many electronic equipment available in the market. The latter has presented an estimation algorithm based on a rectifier model and actual measurements.

The procedures described before offers several rules that enable to obtain the circuit model of CFLs available on the market. Such an approach could be adopted for LED light bulbs, but these procedures require the knowledge of the ballast internal circuit components and not negligible computational resources, which make them unsuitable tools for optimal lighting system design. Moreover, the circuit model includes non-linear components. On the other hand, as said before, although several objectives and constraints have been considered so far in the optimal lighting system design, the harmonic mitigation target has been totally neglected. Therefore, a parametric Pspice circuit overcoming these limitations has been proposed in chapter 2. The knowledge of the ballast circuit, driver, package, and so on, is not necessary to obtain the parameters to be used in the proposed Pspice circuit. Indeed, any LED light bulb can be treated as a black box, and the components of the circuit are simply obtained with some electrical measurements, which is the amplitude and phase shift of the fundamental current and harmonics drawn by the LED light bulb. An additional advantage of the proposed circuit is that it contains only linear components and the circuit simulation is very fast and it requires few computational efforts.

Chapter 2 Analysis of the Input Current Distortion in High PF Quasi-Resonant Flyback LED Drivers

2.1 Introduction

As said before, the driver regulates its input current as well as the output current towards the LED load, thus it must guarantee a high power factor and a suitable current for the LED load. Among the various LED drivers available on the market, the quasi-resonant (QR) flyback topology shows interesting benefits. The flyback converter is the most used SS LED driver because it obtains high step-down ability and it provides a good tradeoff among the power quality, the cost, the capacitor size, and the efficiency. In integrated lighting applications, a SS discontinuous current conduction mode (DCM) flyback PFC converter is commonly used to drive the LED light bulbs in order to achieve a high PF. The task is performed by means of a simple circuit configuration used to regulate the lamp current. A flyback LED driver operating in DCM where the PFC proprieties can be easily obtained has been frequently adopted. In this context, the quasi-resonant (QR) flyback LED driver can effectively reduce the transformer size and weight thanks to the high switching frequency, which is not fixed since it increases as the load decreases. Furthermore, the switching losses can be strongly reduced by adopting zero voltage switching (ZVS).

A suitable control method enables to obtain a high power factor (Hi-PF) QR flyback LED driver. On the other hand, there are different inherent causes of distortion in the input current to be faced. It is worth noting that, these causes are due to the power processing mechanism of the Hi-PF QR flyback converter and they are not ascribable to the specific control method (although the control method may mitigate them). The first part of the proposed work aims at investigating and analyzing the different issues due to the correlation of several causes such as the ringing current, crossover distortion due to transformer leakage inductance, and crossover distortion due to the input storage capacitor. The input current distortion caused by the ringing current has been widely studied for the boost converter, while it is the first time the problem has been studied for the QR flyback. Moreover, the

crossover distortion due to the input storage capacitor in the case of a Hi-PF flyback LED driver has never been treated in literature. Furthermore, an accurate analysis has been performed in this work by considering the linear approximation of the input voltage and the related comparison with a sinusoidal waveform. Finally, some practical design guidelines for mitigating them in a Hi-PF QR flyback driver for LED applications are provided.

2.2 Generic Control Method Obtaining High Power Factor

Although the QR flyback converter topology is extremely popular since it is a very cost-effective solution with high performance, the converter features inherent distortion of the input current. Normally, this distortion is not a concern for compliance with the IEC61000-3-2, however, some input current THD targets (e.g., <10% at full power) are becoming market requirements that are very difficult to achieve, especially when working with lighting equipment over 25 W [84].

As shown in Figure 1:7, the storage capacitor of the QR flyback is placed on the low-frequency side of the dc-dc converter. With the aim to reduce the input current THD, the capacitor should be placed downstream from the converter, according to the waveform simulations in Figure 1:5 (red trace) related to the capacitor position of Figure 1:4. In this perspective, the converter can be considered as a Hi-PF QR flyback, which has a rectified voltage in input and the storage capacitor downstream of the power stage. The aforementioned solution strongly reduces the harmonics distortions of the input current drawn by the LED light bulb.

The control gear in a Hi-PF QR flyback converter has a twofold task: firstly, it is responsible for regulating the output voltage or current and, simultaneously, it has to maintain a low THD of the input current. For the sake of completeness, the characteristics and proprieties of the control method that have to be considered to achieve a Hi-PF QR flyback converter will be briefly discussed.

The control method, shown in Figure 2:1, is responsible for the turn on and turn off of the switch.

Henceforth, the quantities depending on the instantaneous line voltage will be considered as a function of the term $\theta = 2\pi f_{line} t$.

The target of the control method is to obtain an input current very similar to a sinusoid in-phase with the input voltage to achieve high-PF. Regardless of the specific control method, the previous target can be partially converted into obtaining a primary current, as shown by I_p in Figure 1:7, whose peak envelope, detailed by the green elements in Figure 2:1, leads to a sinusoid in-phase with the input voltage. To obtain such an envelope, the control method

must turn off the switch when the current on the primary side reaches one of the (green) peaks in Figure 2:1. To obtain a similar result for the secondary current, shown by the red elements in Figure 2:1, a similar control must be adopted for the switch turn on. The turn-on must occur when the transformer is fully demagnetized, thanks to a zero-current detector. In other terms, the combination of these switching rules, which result in a variable switching frequency, shown in Figure 2:1, ensures that the peaks of the primary current, in a half period of the rectified voltage $V_{in}(\theta)$, can be enveloped by a rectified sinusoid. The primary current $I_p(\theta)$ in a switching cycle is triangular shaped and flows only during the switch on-time, as sketched by the green triangles shown in Figure 2:1. During the off-time, the secondary current $I_s(\theta)$ flows and it is represented by the red triangles. Therefore, the switching frequency SW is variable, where the $T_{ON}(\theta)$ and $T_{OFF}(\theta)$ are modulated to achieve a sinusoidal current envelope.

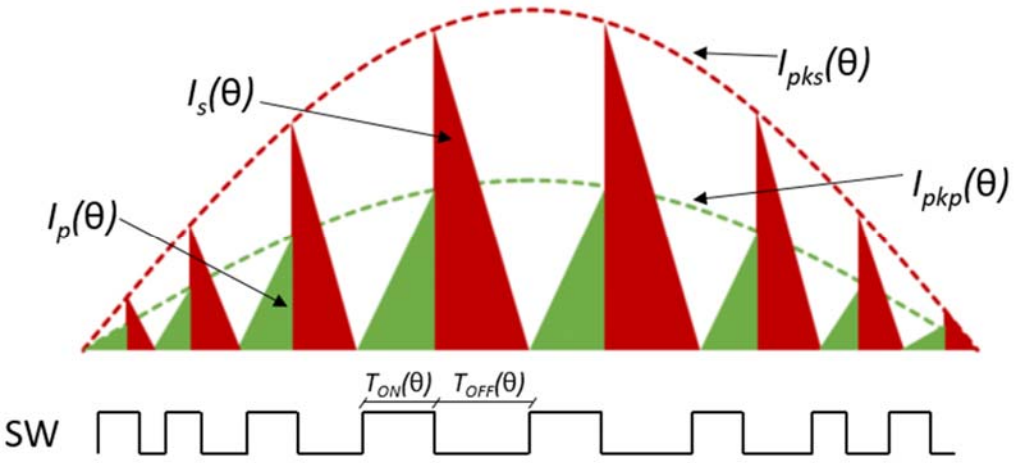


Figure 2:1 Primary and secondary currents in a QR-controlled Hi-PF flyback converter.

However, the primary current $I_p(\theta)$ flows only during the on-time of the power switch, and this means that the average value of the primary current deviates significantly from an ideal sinusoid. To ensure good performance and low THD input current for a Hi-PF driver LED, the quantity D^2T (D is the duty ratio) must be constant along each line half-cycle, thus a unity PF is obtained [85].

In the following, it is assumed that the generic control method implements the previous features. For the sake of simplicity to obtain a quantitative expression of the input current I_{in}, the following assumptions have been considered:

1. The line voltage is sinusoidal, and the input bridge rectifier is ideal, thus the voltage at the bridge output terminal is a rectified sinusoid.

2. The voltage drop across the power switch in the on-state is negligible and there is negligible energy accumulation on the dc side of the bridge.

3. The transformer windings are perfectly coupled (i.e., no leakage inductance).

4. The turn-off transient of the power switch has a negligible duration so that T_{FW} immediately follows T_{ON}.

5. The converter is operated so the power switch is turned on in each cycle after the secondary current becomes zero, therefore in either QR-mode (i.e., on the first valley of the ringing in the drain-source voltage) or DCM.

6. The output voltage is constant along a line half-cycle.

7. During the time interval elapsing from the instant when the transformer demagnetizes to the instant when the power switch is turned on, the transformer current is zero; consequently, the initial current during the on-time is zero too. This time interval is equal to $T_r/2$ in the case of the converter being used in QR mode.

It is worth generalizing the relation to D^2T when a variable switching frequency is used, in particular:

$$D^2T = \left[\frac{T_{ON}(\theta)}{T(\theta)}\right]^2 T(\theta) = \frac{T_{ON}(\theta)^2}{T(\theta)} = \text{constant} \tag{4}$$

where the dependencies of T_{ON} and T on θ point out that they are a function of the instantaneous line voltage V_{ac}. Assuming that the rectified voltage V_{in} is sinusoidal in $0 \le \theta \le \pi$, according to assumption 1, it can be written as:

$$V_{in}(\theta) = V_{in,pk}\sin(\theta) \tag{5}$$

where $V_{in,pk}$ is the amplitude of the rectified voltage.

By considering the current flowing in the primary windings during the time interval T_{ON}, and bearing in mind the inductance current-voltage differential relation, the peak value of primary current $I_{pkp}(\theta)$ can be expressed as:

$$I_{pkp}(\theta) = \frac{1}{L_p}\left(V_{in,pk}\sin(\theta)\right)T_{ON}(\theta) \tag{6}$$

The generic control method must ensure that the height of the triangles depicted in Figure 2:1 varies along a line cycle as expressed by (6). To reach this target, the control method

must properly vary the width of $T_{ON}(\theta)$ as well as $T_{OFF}(\theta)$. The input current $I_{in}(\theta)$ is the average value of each triangle over a switching cycle, hence, taking (6) into account:

$$I_{in}(\theta) = \frac{1}{2} I_{pkp}(\theta) \frac{T_{ON}(\theta)}{T(\theta)} = \frac{1}{2L_p} \left(V_{in,pk} \sin(\theta) \right) \frac{T_{ON}(\theta)^2}{T(\theta)} \tag{7}$$

It is worth noting that, if the ratio $T_{on}(\theta)^2/T(\theta)$ is maintained constant by the controller, the input current $I_{in}(\theta)$ can be assumed sinusoidal. Figure 2:2 summarizes the key current waveform in the Hi-PF driver LED.

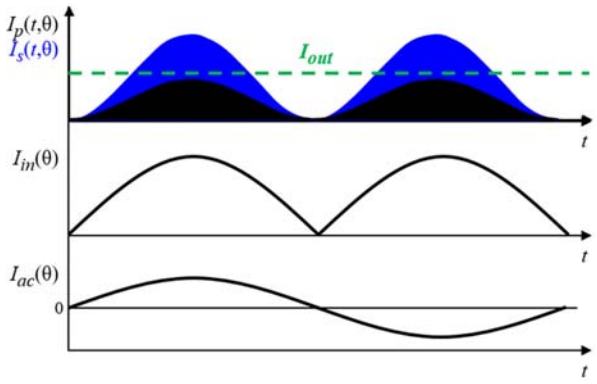


Figure 2:2 Current waveforms of the circuit in Figure 1:7: line cycle time scale of the primary current I_p, the secondary current I_s, input rectified current I_{in} and current in the ac side I_{ac}.

Despite the fact that a suitable control method leads to a Hi-PF QR flyback driver according to the previous features, there are different inherent causes of distortion in the input current to be faced. The distortion due to these causes is reported in the next section where the THD has been experimentally evaluated. After that, in the following subsections, these causes, due to the power processing mechanism of the QR flyback converter that are not ascribable to the specific control method (although the control method may mitigate them), are described.

2.3 *Experimental Verification of the Input Current Distortion in a Hi-PF QR Flyback LED Driver*

A prototype of a Hi-PF QR flyback LED driver has been set up to highlight the distortion occurring, even when a control method implementing the previous features is adopted. The main parameters of the converter are summarized in Table 2:1.

The prototype has been built and its performance has been evaluated on the bench. The PF has been result greater than 0.98 over the input voltage range at full load. At 50% load, at a low line, it was nearly equal to that at 100% load, but at the high line, it dropped to about 0.97 at 230 V_{ac}. Figure 2:3 depicts the experimental waveforms of the input current $I_{ac}(\theta)$ (blue trace), the output voltage (red trace), the drain current of the MOSFET (green trace), and the current sense voltage reference for the controller (purple trace). The measurements have been carried out at full load both 110 V_{ac} (60 Hz) and 230 V_{ac} (50 Hz). From the experimental evidence, the shape of the measured $I_{ac}(\theta)$ results very close to an ideal sinusoid waveform. It is worth noting that the harmonic contribution the prototype boards met the European norm EN61000-3-2 Class-C and Japanese norm JEITA_MITI Class-C, both of which are relevant to lighting equipment, at full load and nominal input voltage mains, as depicted in Figure 2:3.

A small distortion in the input current is apparent in Figure 2:3 (blue trace) by looking at the zero crossing of the waveform. Therefore, as previously mentioned, notwithstanding the enhanced performance of a Hi-PF QR flyback LED driver, there are still different inherent causes of distortion in the input current that are not ascribable to the specific control method. The causes are the ringing current, the crossover distortion due to transformer leakage inductance, and crossover distortion due to the input storage capacitor. Generally speaking, being the converter in a nonlinear system, the overall THD of the input current cannot be the sum of each distortion contribution. Due to the number and the complexity of the distortion causes and, above all, due to the complexity of their mutual multi-interactions, the only way to have a sensible estimate of the overall result in terms of input current THD is to resort to simulations.

It is worth noting that the distortion of the input current $I_{ac}(\theta)$ caused by the ringing effect has already been studied theoretically for boost PFC [86-88], while in the case of a Hi-PF QR flyback it has not yet been treated. Furthermore, the crossover distortion due to the input storage capacitor in the case of a Hi-PF flyback LED driver has never been studied. Finally, the crossover distortion due to transformer leakage inductance has also been theoretically analyzed in depth.

Table 2:1 Main characteristics of the Hi-PF QR flyback converter.

Parameter	Value
Input voltage range [V_{ac}]	90–265 V
Line frequency range [f_l]	47–63 Hz
Rated output voltage [V_{out}]	48 V
Regulated dc output current [I_{out}]	700 mA
Expected full-load efficiency [η]	86%
Transformer primary inductance [L_p]	500 µH
Reflected voltage [V_R]	120 V
Drain–Source capacitance [C_{DS}]	150 pF

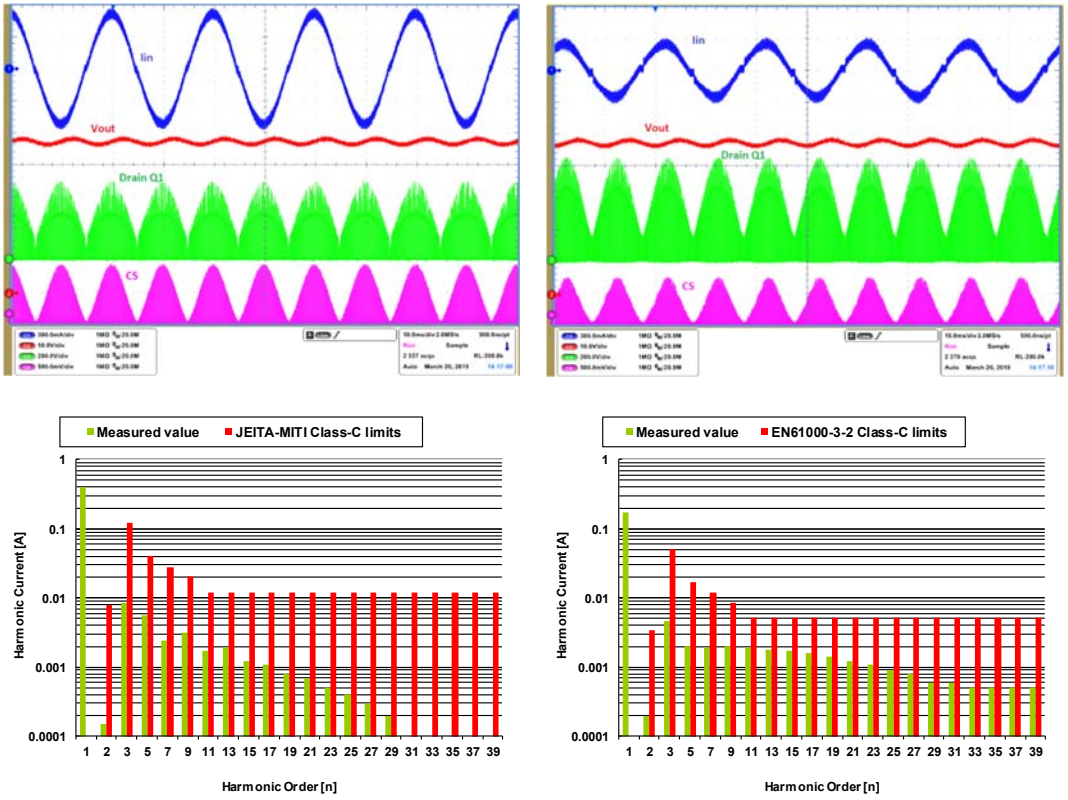


Figure 2:3 Steady-state waveforms at full-load: (a) Vin = 110 V at 60 Hz. (b) Vin = 230 V at 50 Hz. They have been overlapped by the harmonic contributions of the input current (green bars) with the Japanese norm JEITA_MITI Class-C (a), and European norm EN61000-3-2 Class-C (b) (red bars) for lighting equipment.

2.4 *Distortion Caused by the Ringing Current*

In a flyback, the drain-to-source voltage rings as soon as the secondary winding is fully demagnetized. The energy is exchanged between the total capacitance C_{DS} of the drain node and the primary inductance of the flyback transformer L_p. For the sake of simplicity, assumption 3 has been assumed, and consequentially it has been carried out an equivalent circuit of the QR flyback during the time interval T_{neg}, which is the duration of the negative portion of the primary current, I_p. The duration of the positive portion, T_{pos}, of the primary current is equal to T_{ON} when the current in the turn-on instant of the power switch is zero. The simplified circuit model and the key waveforms are depicted in Figure 2:4.

In Figure 2:4(a), the voltage across L_p is equal to the reflected output voltage V_R, which is almost constant during T_{FW}, according to the previous assumption 6. After that, the voltage

across L_p and C_{DS} and the current through them start to oscillate. More specifically, the analytical expressions of $V_{DS}(t)$ and $I_p(t)$ in the time interval T_{neg}, can be written as:

$$V_{DS}(t)=\begin{cases} V_{in}(t)+V_R\cos\left(2\pi\dfrac{t}{T_r}\right) & 0<t\le T_z \\ 0 & T_z<t\le T_{neg} \end{cases} \tag{8}$$

$$I_p(t)=\begin{cases} -Y_L V_R\sin\left(2\pi\dfrac{t}{T_r}\right) & 0<t\le T_z \\ I_p(T_z)+\dfrac{V_{in}}{L_p}t & T_z<t\le T_{neg} \end{cases} \tag{9}$$

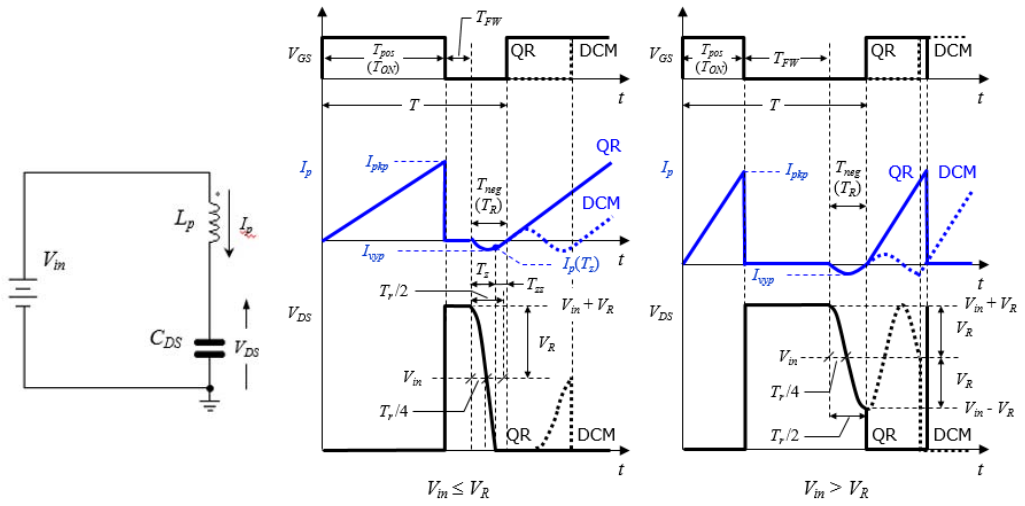
$$Y_L=\sqrt{\frac{C_{DS}}{L_p}} \tag{10}$$

where Y_L is the characteristic admittance of the C_{DS}-L_p tank circuit and T_z is the time interval needed for the V_{DS} to fall zero when $V_{in} < V_R$; that is:

$$V_R\cos\left(2\pi\frac{T_z}{T_r}\right)=-V_{in}(T_z) \tag{11}$$

When QR-mode is adopted, the device can be turned on, but according to assumption 5, the current must reach zero. T_{zz} is the time interval needed for the primary current I_p to ramp linearly until zero from the current value $I_p(T_z)$. In DCM operation, considering that I_p oscillates around zero, and that ringing is damped, after a few ringing cycles, assumption 7 can be considered exactly true; with QR operation, the negative current just after demagnetization is not compensated by subsequent positive contributions as in DCM. Considering zero the average value of I_p, as per assumption 7, is already a better approximation as compared to totally neglecting T_R (i.e., assuming the operation is exactly at the boundary between DCM and CCM). However, in this context, assumption 7 is just a simplification, whose impact on the shape of the input current, quantitatively expressed by its THD, needs to be assessed. Being the ringing current at the turn-on instant of the power switch equal to the initial current during the on-time interval, this current may or may not be zero, which has an impact on the shape of the input current and, consequently, on its THD too.

When $V_{in} > V_R$, in QR-mode, the turn-on occurs at the first valley of the ringing in the drain voltage that follows the transformer demagnetization. Therefore, in this case, T_{neg} is equal to $T_r/2$.



(a) (b)

Figure 2:4 (a) Simplified equivalent circuit during Tneg , (b) key waveforms in QR-mode, and DCM operations.

By neglecting the input capacitor C_s from the QR flyback schematic in Figure 1:7, the following considerations are valid: during T_{on} a charge Q_{pos} is provided from the input source and stored in the transformer; during T_{FW}, the energy is mostly delivered to the output; finally, in T_{neg}, a negative charge Q_{neg} is returned to the input source. The average input current during a switching cycle can, therefore, be expressed as:

$$\left\langle I_p \right\rangle = \frac{Q_{pos} - Q_{neg}}{T} \tag{12}$$

As shown in Figure 2:4, the positive charge Q_{pos} is clearly given by:

$$Q_{pos} = \frac{1}{2} I_{pkp} T_{on} \tag{13}$$

To evaluate the absolute value of the negative charge Q_{neg}, it is necessary to consider Equations (8)-(10)that describe the $V_{DS}(t)$ and $I_p(t)$ variations in the time interval T_{neg} (when QR operation is only considered) and distinguish two cases.

1. $V_{in} > V_R$. In the time interval (0, T_{neg}) $V_{DS}(t)$ is always greater than zero and the current $I_p(t)$ is sinusoidal; T_{neg} equals half the ringing period. The average value of $I_p(t)$ during T_{neg} is 2/π times the negative peak value $|I_{vyp}| = Y_L V_R$, therefore:

$$Q_{neg} = T_{neg}\frac{2}{\pi}Y_L V_R = \frac{T_r}{\pi}Y_L V_R = 2V_R C_{DS} \tag{14}$$

2. $V_{in} \le V_R$. The current $I_p(t)$ is sinusoidal in the subinterval (0, T_z). T_z can be expressed as:

$$T_z = \frac{T_r}{2}\left(1 - \frac{1}{\pi}\cos^{-1}\left(\frac{V_{in}}{V_R}\right)\right) \tag{15}$$

and the current $Ip(t)$ evaluated when $t = Tz$ is:

$$I_p(T_z) = -Y_L V_R\sqrt{1-\left(\frac{V_{in}}{V_R}\right)^2} \tag{16}$$

As depicted in Figure 2:4 (b), in the time interval T_{zz}, $I_p(t)$ ramps up linearly to zero. Hence, T_{zz} can be expressed as:

$$T_{zz} = \frac{L_p}{V_{in}}\left|I_p(T_z)\right| \tag{17}$$

Since T_{neg} is the sum of T_z and T_{zz}, it can be written:

$$T_{neg} = T_z + T_{zz} = \frac{T_r}{2}\left[1 + \frac{V_R}{V_{in}}\sqrt{1-\left(\frac{V_{in}}{V_R}\right)^2} - \cos^{-1}\left(\frac{V_{in}}{V_R}\right)\right] \tag{18}$$

which is always greater than $T_r/2$, except when $V_{in} = V_R$. Finally, Q_{neg} is given by the sum of the two contributions, Q_{neg1} during the subinterval (0, T_z) and Q_{neg2} during the subinterval (T_z, T_{neg}). After some mathematical steps, Q_{neg} can be evaluated as:

$$Q_{neg} = Q_{neg1} + Q_{neg2} = \int_0^{Tz} Y_L V_R \cos\left(2\pi\frac{t}{T_r}\right)dt + \int_{Tz}^{Tneg} I_p(T_z) + \frac{V_{in}}{L_p}t\,dt = \frac{1}{2}C_{DS}\frac{(V_{in}+V_R)^2}{V_{in}} \tag{19}$$

Considering equation (12), the overall input current $I_{in}(\theta)$ can be found by adding the contributions obtained in Equations (7)and (13), which also takes into account the ringing oscillations along each line half-cycle. Hence it can be written as:

$$I_{in}(\theta) = \begin{cases} \frac{1}{2}I_{pkp}(\theta)\frac{T_{on}(\theta)}{T(\theta)} - \frac{2}{T(\theta)}V_R C_{DS} & V_{in} > V_R \\ \frac{1}{2}I_{pkp}(\theta)\frac{T_{on}(\theta)}{T(\theta)} - \frac{1}{2T(\theta)}\frac{(V_{in}+V_R)^2}{V_{in}}C_{DS} & V_{in} \le V_R \end{cases} \tag{20}$$

It is evident that the positive term in Equation (20) does not introduce any distortion, provided that the generic control method provides $I_{pkp}(\theta)$, as in Equation (6), and satisfies equation (4). The contribution of the ringing current, related exclusively to the negative terms, takes into account the ringing contributions derived in Equations (14)-(19). They represent a twofold effect: they downwards offset the input current waveform, which produces crossover distortion, and, considering that the offset is a function of the instantaneous line voltage, they distort its shape as well. It is worth noting that the distortion contribution is not ascribable to the control method; that is, it is not due to the control but is inherent in the power processing mechanism of any Hi-PF QR flyback converter. On the other hand, the control method may compensate or mitigate it. First of all, the contribution of the ringing current can be reduced by lowering the switching frequency (i.e., a longer $T(\theta)$, obtained with a larger L_p value) and using a low reflected voltage V_R. However, a larger L_p value implies a bigger flyback transformer, and a lower V_R increases the primary *rms* current and, consequently, the conduction losses. A trade-off is therefore required. A smaller C_{DS} also helps to reduce the ringing contribution, however, it is important to underline that a tradeoff between switching losses and EMI should be found. In fact, the lower the C_{DS}, the faster the V_{DS} transient at turn-off, and this faster transient may adversely affect both the efficiency of the power switch, as well as the EMI.

LED driver applications are typically specified to accommodate a certain range of output voltages V_{out} to power different types and lengths of LED string. Thus the contribution of the ringing current is expected to be maximum at the upper end of the V_{out} range and minimum at the lower end of the V_{out} range. In fact, lowering V_{out} will simultaneously reduce V_R and increase $T(\theta)$.

2.5 Crossover Distortion Due to the Input Capacitor

The storage capacitor *Cs* placed downstream of the input bridge, as depicted in Figure 1:7, is part of the EMI filter, which is always needed in an SMPS connected to the power line to restrict the conducted emission within the limits envisaged by the relevant EMI regulations. The capacitor has a twofold effect: it contributes to the voltage-current phase-shift and worsens the THD by maintaining a residual voltage on the dc side of the input bridge rectifier. The latter causes a non-conduction zone as the line voltage approaches zero, therefore, assumption 2 is no longer valid for the following analysis. This phenomenon also occurs for systems without a PFC and is an additional source of crossover itself, which interacts with the other distortion mechanisms. A quantitative analysis of this crossover distortion can be carried out independently from the topology employed in a PFC.

In these terms, any PFC and, consequently, the Hi-PF QR flyback converter can be modeled with an equivalent resistor (R_{eq}) that can be expressed as:

$$R_{eq} = \frac{V_{PK}^{\ 2}}{2P_{in}} \tag{21}$$

where V_{PK} is the peak of the rectified line voltage $V_{in}(\theta)$ and P_{in} is the input power of the converter.

Generally speaking, the dead zone in $I_{ac}(\theta)$ increases at large C_S values, high line voltage, and low load (large R_{eq}). In quantitative terms, the dead zone starts, near the zero-crossing, when the rate of fall in the line voltage $V_{ac}(\theta)$ exceeds the rate of the voltage $V_{in}(\theta)$ across C_S, limited by the time constant $R_{eq}\,C_S$, so that from that instant on it is $V_{ac}(\theta) < V_{in}(\theta)$, as shown in Figure 2:5.

Focusing on the $V_{ac}(\theta)$ and $V_{in}(\theta)$ near the zero-crossing zone, shown in Figure 2:5(a), and neglecting the voltage drop across the input bridge rectifier, the phase angle α at which the slope of the two voltages are equal can be found with the following relation:

$$\left|\frac{dv_{ac}(\theta)}{d\theta}\right| = \left|\frac{dv_{in}(\theta)}{d\theta}\right| \quad \Rightarrow \quad 2\pi f_L V_{PK}\cos\alpha = \frac{1}{R_{eq}C_s}V_{PK}\sin\alpha \tag{22}$$

Solving for α:

$$\tan\alpha = 2\pi f_L R_{eq} C_s \tag{23}$$

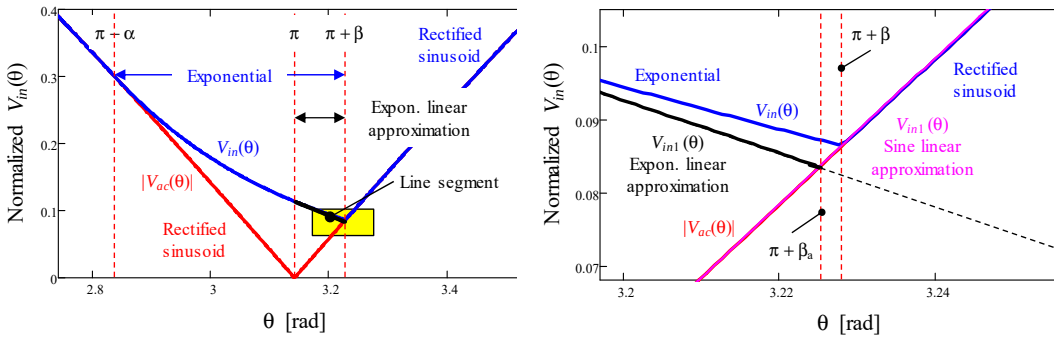


Figure 2:5 Detail of $V_{ac}(\theta)$ (red trace) and $V_{in}(\theta)$ (blue trace) near voltage zero-crossing (**a**), and zoomed view of the yellow area, the intersection of $V_{ac}(\theta)$ and $V_{in}(\theta)$ (**b**). Values are normalized to V_{PK}.

From π-α on, $V_{in}(\theta)$ follows an exponential decay until the phase θ is equal to π + β, where it is again $|V_{ac}(\theta)| \geq V_{in}(\theta)$, which marks the end of the dead zone. In this interval the expression of $V_{in}(\theta)$ can be assumed as:

$$V_{in}(\theta) = \sin\alpha e^{-\frac{\theta-(\pi-\alpha)}{\tan\alpha}} \tag{24}$$

Beyond the angle π + β, $V_{ac}(\theta)$ and $V_{in}(\theta)$ are again both sinusoidal and overlapping until they have a phase shift equal to α away from the next zero-crossing. The duration of the dead zone is clearly α + β.

The phase angle β can be found at the intersection of an exponential curve with a sinusoidal one, which results in a transcendental equation with no closed-form solution. Since β is small, it is possible to find an approximate solution β_a, substituting the last part of the exponential function (from θ = π to θ = π + β) with its expansion in Taylor series to the first order ($e^{-\theta} \approx 1-\theta$). In a similar way, it can be done for the rectified sinusoid ($sin\ \theta \approx \theta$). Therefore, the value Λ of the input voltage, evaluated when the phase angle is π, can be computed as follows*:*

$$\Lambda = V_{in}(\pi) = \sin\alpha e^{-\frac{\alpha}{\tan\alpha}} \approx \frac{\sin\alpha}{e} \tag{25}$$

As shown in Figure 2:5(b), at the intersection of the two straight lines, the phase angle is π + β_a.

$$\begin{cases} V_{in1}(\theta) = \Lambda\left(1-\dfrac{\theta-\pi}{\tan\alpha}\right) \\ V_{in2}(\theta) = \theta-\pi \end{cases} \tag{26}$$

$$\beta_a = \frac{\Lambda\tan\alpha}{\Lambda+\tan\alpha}$$

The truncation of the exponential Equation (24) to the first order introduces an underestimation, as depicted in Figure 2:5(b), hence Equation (26) provides an approximated value β_a < β. On the other hand, if Equation (24) is approximated to the second-order, which provides a better approximation of equation (24), an overestimation will result, and the approximated value β_a > β is less than 4% larger than the value provided by Equation (26), which proves that the accuracy of the first assumption is valid anyway.

The previous analysis shows that the storage capacitor C_S can be assumed as a source of crossover distortion, even if R_{eq} is a real resistor. The key point is the inability of $V_{in}(\theta)$ to keep pace with $V_{ac}(\theta)$ on the falling edge of the sinusoid, due to the maximum discharge rate of C_S through R_{eq}. However, its net impact is the result of the interaction with the other sources of distortion, previously analyzed.

In fact, it has been assumed that a resistor R_{eq} that represents the whole converter, which implicitly means that the ratio of $V_{in}(\theta)$ to $I_{in}(\theta)$ is constant in (0, π); i.e., $I_{in}(\theta)$ is pure sinusoi-

dal in (0, π). Actually, the distortion of the current shape, caused by all the previously considered sources, tends to reduce $I_{in}(\theta)$ with respect to the undistorted case. Instead, considering the same model approach, if it can be assumed that the R_{eq} changes along the sinusoid, then $R_{eq} = R_{eq}(\theta) = V_{in}(\theta)/I_{in}(\theta)$. Figure 2:6 shows $R_{eq}(\theta)$ obtained by dividing a sinusoidal input voltage and the current drawn that takes into account the distortion caused by the ringing current in Equation (20).

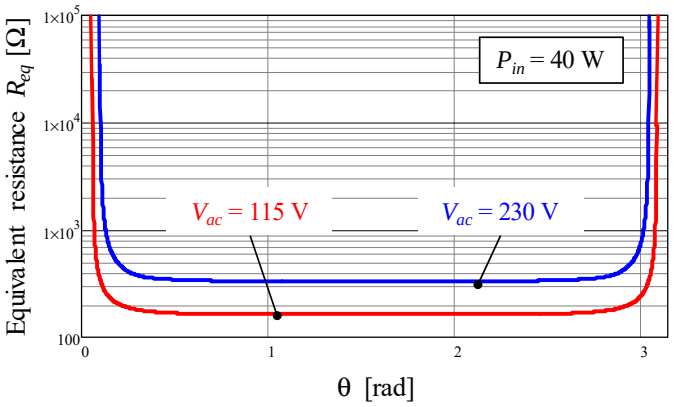


Figure 2:6 Variation of $R_{eq}(\theta)$ along the sinusoid for the prototype converter caused by the ringing current.

$R_{eq}(\theta)$ is almost flat for a wide range of the sinusoid except when the current is approaching the zero crossings. The increase in $R_{eq}(\theta)$ produces an early dead zone with respect to the case with a fixed R_{eq}. The corresponding value of α would be the solution of the equation:

$$\tan\alpha = 2\pi f_L R_{eq}(\alpha) C_s \tag{27}$$

The solution of Equation (27) must be defined in the interval (π/2, π), where *tan* α has a finite value and consequentially also $R_{eq}(\alpha)$. As a result, the dead zone caused by the input capacitor C_s starts before $R_{eq}(\theta)$ diverges, and $I_{ac}(\theta)$ must cross zero before $I_{in}(\theta)$. In other words, as long as the bridge rectifier conducts, $I_{ac}(\theta)$ is the sum of $I_{in}(\theta)$ and the current through C_S, which is essentially a sinusoid leading by 90 degrees. This causes $I_{ac}(\theta)$ to lead $I_{in}(\theta)$, whereas without C_S they would be essentially coincident.

Within the dead zone, the relation $R_{eq}(\theta) = V_{in}(\theta)/I_{in}(\theta)$ is no longer the one shown in the diagram of Figure 2:6 because of both the voltage $V_{in}(\theta)$ and the $I_{in}(\theta)$ are not sinusoidal. Besides, the voltage retained by C_s, which makes $V_{in}(\theta) > |V_{ac}(\theta)|$, and $T_{ON}(\theta)$ and $T(\theta)$ will be much smaller than those predicted during the control method design, which it has been carried out assuming a sinusoidal input voltage, as per Equation (5). The resulting switching frequency may be higher. As long as some energy is delivered to the output, C_S (which is the only source of energy, since no current comes from the reverse-biased bridge rectifier),

keeps on discharging and as long as $I_{in}(\theta) > 0$. If the peak current becomes lower than the critical peak primary current for no energy transfer, the energy is no longer transferred to the output and bounces back and forth between C_S and L_p, except for the energy dissipated during this process. As a consequence, C_S is discharged at a lower rate. Instead, if the peak current does not go below that critical value, the discharge rate of C_S has no change.

When $|V_{ac}(\theta)| \geq V_{in}(\theta)$ and the dead zone ends at $\theta = \beta$, it is possible to observe an abrupt variation in $I_{ac}(\theta)$. This is caused by the bridge rectifier that is forward-biased, as $I_{ac}(\theta)$ has to transition from zero to $I_{ac}(\beta)$, which is already greater than zero because of the leading phase of $I_{ac}(\theta)$.

It is worth mentioning that, near the zero-crossing interval, the input voltage is far from constant in a switching cycle and the switching frequency may come close to the frequency related to the resonance between C_S and L_p. So, the $V_{in}(\theta)$ has sinusoidal behavior, rather than constant. Additionally, the resonance of the inductors and capacitors in the EMI filter can also be stimulated, so that different resonance phenomena may coexist. This means that the modeling approach used throughout the present discussion is not always valid in describing the practical behavior.

2.6 Crossover Distortion Due to Transformer's Leakage Inductance

In practical cases, the real transformer's windings are not perfectly coupled. This phenomenon causes a crossover distortion that affects the input current shape and degrades the THD. Therefore, in the following subsection, the analysis of the distortion no longer takes into account assumptions 3 and 4.

In a real transformer, a portion of the energy stored in the primary winding cannot be transferred to the secondary winding because of imperfect magnetic coupling. In other words, this can be modeled by considering the primary inductance L_p split into two distinct elements: the magnetizing inductance L_M perfectly coupled to the secondary winding and the leakage inductance L_{lk} (uncoupled). In these terms, it is useful to define the coupling coefficient σ such that $L_M = \sigma L_p$ and $L_{lk} = (1- \sigma) L_p$. Typical values of σ range from 0.95 to 0.99.

The energy stored in the leakage inductance is not transferred to the output and this energy would overcharge C_{DS} well over $V_{in}(\theta) + V_R$, in most cases exceeding the voltage rating of the power switch. A typical solution is to use a clamp circuit that limits $V_{DS}(t)$ at a well-defined and properly selected value V_{CL} ($> V_R$) above $V_{in}(\theta)$. Figure 2:7 shows the equivalent circuit of the Hi-PF QR flyback converter during the off time and the current waveforms underlining the effect of L_{lk}.

When the power switch is turned off, the primary current firstly charges the capacitance C_{DS}, thus the $V_{DS}(t)$ evolves until the voltage of the magnetizing inductance L_M, V_M, equals $-V_R$. During this time interval T_{ps}, the primary current I_p is flowing through L_M and L_{lk}, so there is an inductive voltage divider. Therefore:

$$V_M = -\frac{L_M}{L_p}V_p = \frac{L_M}{L_p}\left[V_{in}(\theta) - V_{DS}(t)\right] \tag{28}$$

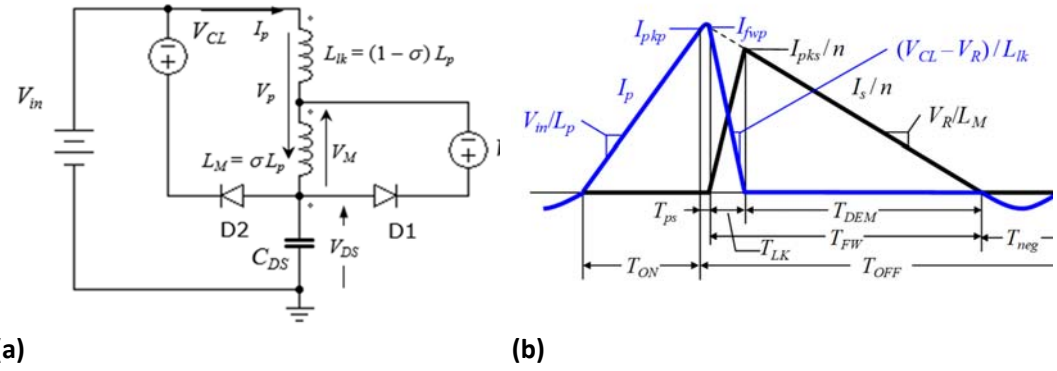


Figure 2:7 (a) Simplified equivalent circuit during off time. (b) Current in the real primary windings (blue trace) and the secondary windings (black trace).

In the instant when the voltage V_M equals $-V_R$, the voltage V_p across the primary winding can be expressed as:

$$V_p = \frac{L_p}{L_M}V_R = \frac{1}{\sigma}V_R \tag{29}$$

Immediately after the time interval T_{ps}, the current starts flowing through D1, and the energy starts being transferred to the output. $V_{DS}(t)$ keeps on ramping up until it reaches $V_{in}(\theta) + V_{CL}$ in a time T_{LK}. After that, $V_{DS}(t)$ is clamped, L_{lk} starts being demagnetized with a rate equal to $(V_R\text{-}V_{CL})/L_{lk,}$ and the current through *D1* reduces at the same rate. The portion of the primary current $I_p(t)$ of the leakage inductance varies from the peak value, $I_{pkp}(\theta)$, until zero in a time interval equal to $T_{LK}(\theta)$. Hence:

$$I_p(t) = I_{pkp}(\theta) - \frac{V_{CL} - V_R}{(1-\sigma)L_p}t \tag{30}$$

As soon as $I_p(t)$ is equal to zero, it can be written in the analytical expression of T_{LK}:

$$T_{LK}(\theta)=\frac{(1-\sigma)L_p}{V_{CL}-V_R}I_{pkp}(\theta) \tag{31}$$

Bearing in mind the current that flows in L_M can be written as:

$$I_M(t)=I_{pkp}(\theta)-\frac{V_R}{\sigma L_p}t \tag{32}$$

Meanwhile, the secondary current reaches its peak value $I_{pks}(\theta)$:

$$I_{pks}(\theta)=nI_M(T_{LK})=n\left[1-\frac{V_R}{V_{CL}-V_R}\frac{1-\sigma}{\sigma}\right]I_{pkp}(\theta) \tag{33}$$

After that, the magnetizing inductance on the secondary side starts being demagnetized at a rate V_R/L_M until it zeroes in a time T_{DEM}, as shown in Figure 2:7. The presence of L_{lk} splits the time interval T_{FW} in a first subinterval T_{LK} needed to demagnetize the leakage inductance (and magnetize the secondary winding) and a second subinterval T_{DEM} needed to demagnetize the secondary winding. It is possible to prove that the resulting T_{FW} can be expressed as:

$$T_{FW}(\theta)=\frac{L_M}{V_R}I_{pkp}(\theta)=\sigma\frac{L_p}{V_R}I_{pkp}(\theta) \tag{34}$$

(i.e., the one calculated neglecting the leakage inductance multiplied by the coupling coefficient σ).

The presence of L_{lk} clearly compromises the input-to-output transfer energy, thus the dead zone where there is no energy transfer is expected to occur over a wider phase angle range of the line voltage. In fact, the "no energy transfer" condition concerns only the portion of the primary voltage V_p across the magnetizing inductance L_M. Combining Equations (8) and (9) and (28), it is possible to find that the condition for no energy transfer, solved for $I_{pkp}(\theta)$, yields:

$$I_{pkp}(\theta)\le Y_L\sqrt{\left(\frac{V_R}{\sigma}\right)^2-V_{in}{}^2(\theta)} \tag{35}$$

The critical peak primary current for no energy transfer, expressed by Equation (35), is larger than the ideal case ($\sigma = 1$), thus confirming the forecast of a wider dead zone related to this phenomenon.

It is noteworthy to compare the critical value of $I_{pkp}(\theta)$ in Equation (35) to that determined by the ringing current after demagnetization and the relative positions of the dead zones they generate.

Bearing in mind that the on-time can be written as:

$$T_{ON} = \frac{L_p}{V_{in}} I_{pkp} \tag{36}$$

The region around zero crossings where there is no input-to-output energy transfer ($I_{in}(\theta) = 0$), can be written by considering the combination of the input current in Equation (20) in the case of $V_{in} < V_R$, and Equation (36):

$$I_{pkp} = \frac{\left(V_{in} + V_R\right)^2}{V_{in}} \frac{C_{DS}}{L_p} \frac{V_{in}}{I_{pkp}} \tag{37}$$

Combining Equations (10)-(37), the ringing current after demagnetization related to the dead zone can be expressed as:

$$I_{pkp} = \frac{\left(V_{in} + V_R\right)^2}{V_{in}} \frac{C_{DS}}{L_p} \frac{V_{in}}{I_{pkp}} \tag{38}$$

Figure 2:8 shows the ratio of the critical value of $I_{pkp}(\theta)$ for no input-to-output energy transfer, as in Equation (35), to that caused by the ringing current, as in Equation (38). The ratio is expressed as a function of the parameter K_v:

$$K_v = \frac{V_{PK}}{V_R} \tag{39}$$

where V_{PK} is the peak value of the rectified line voltage $V_{in}(\theta)$. The dashed blue line represents the ideal case. As is evident from Figure 2:8, the dead zone becomes even larger near the zero crossings. Therefore, the lack of input-to-output energy transfer may override the dead zone caused by the ringing current needed for the demagnetization of the secondary winding in a time T_{DEM}.

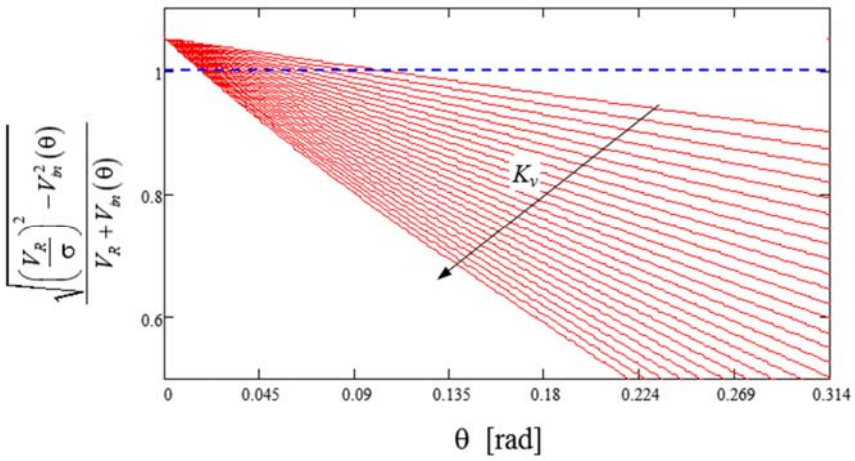


Figure 2:8 Ratio of the critical value of $I_{pkp}(\theta)$ for no input-to-output energy transfer in the dead zone, caused by leakage inductance, as in Equation (35), to that caused by ringing current, as in equation 38, as a function of *Kv* for σ = 0.95.

2.7 Guidelines for Designing High Power Factor Quasi-Resonant Flyback LED Drivers

The QR flyback shows the highest figure of merit (FOM) among the different LED driver solutions analyzed in the literature. With this aim, in the previous sections have been analyzed the different inherent causes of distortion in the input current and the power processing mechanism of the proposed QR flyback converter that are not ascribable to the control method.

Several effects, such as the distortion caused by the ringing current, crossover distortion due to transformer leakage inductance, and crossover distortion due to the input storage capacitor, have been analyzed in depth. It is important to point out that the converter is a nonlinear system and, consequentially, the overall THD of the input current cannot be evaluated as a simple sum of the THD associated to each individual contribution, where the aforementioned issues are mutually interacting or partly overlapping, such as those creating a dead zone in the line current.

Some useful design hints have been extracted and discussed in order to provide some suggestions for an optimized design of a QR flyback LED driver converter. In detail, the following list summarizes all the possible precautions to bear in mind.

1. The impact of the ringing current after transformer demagnetization can be mitigated by lowering the switching frequency, using a low reflected voltage VR or choosing a power MOSFET with a *RDS(on)* with an optimized RDS(on)/C_{oss} FOM. These criteria also help to

reduce the phenomenon of the lack of input-to-output energy transfer near the zero crossings of the line voltage.

2. The leakage inductance of the transformer should be kept as low as practically possible. This choice essentially optimizes the converter efficiency but does not impact the reduction in the dead zones near the zero crossings of the line voltage caused by other phenomena (essentially, the input capacitor C_S).

3. The input storage capacitor C_S should be minimized to reduce the dead zone near the line voltage zero crossings and the current leap occurring in the proximity of the dead zone. However, particular attention should be paid to the following points.

a. The diodes of the input bridge rectifier are usually slow-recovery ones, so the primary current at the switching frequency may require an enhanced filter on the ac side of the bridge and may cause the diodes of the bridge to overheat.

b. Close to the zero crossings, the switching frequency can be very low. If the ringing frequency related to C_S and L_p is comparable with the switching one, it may generate current spikes that would degrade the current THD.

4. Class-X capacitors are generally used along with inductors for EMI filtering, necessary for the certification of the final product. Class-X capacitors can degrade the PF, although they do not contribute to the THD. From this perspective, on the one hand, the design of the filter must make the device compliant with the standards. On the other hand, there is a degree of freedom that can be exploited to minimize PF lowering at the high line and light load. The filters should be designed with the largest inductance and the smallest capacitance practically possible.

Chapter 3 Circuit model of LED light bulb

3.1 Introduction

Nowadays, the investigation of the current harmonics prediction in the case of a lighting system generates a lot of interest. With a large use of LED light bulbs, additional issues will involve in the future smart grids that use network control and management techniques based on measurements that may be affected by the harmonics. The problem is exacerbated by the LEDs since dealing with the large distorted current due to a very great number of dispersed LEDs is more complex than in the case of a single large harmonics source. Therefore, there is a noteworthy need for mitigation of the harmonics due to LED-based lighting systems. The addition of filters, power factor corrector circuits, and other devices in the ESL increases the lamp cost and consequently the economic investment for both retrofitting and new lighting systems installation. On the other hand, although a single compensation circuit for the whole lighting system may be less expensive, it has to be revised each time a new lighting system retrofit is performed.

The best choice from cost and flexibility point of view is the harmonic mitigation at the lighting system design stage. The optimal lighting system design aiming at mitigation of the distorted current drawn from the whole lighting system requires a tool for estimating such a current when different lamps configurations are adopted (number, type, nominal parameter, and so on). In such a case the best configuration is the one with the greatest harmonic cancellation and lowest THD.

In this perspective, the proposed parametric Pspice circuit is suitable to perform this task. This chapter describes the proposed equivalent circuit which is able to model the current drawn of any LED light bulb, whatever is the lamp driver, provided that the voltage THD does not exceed the limit of IEEE-Std-519. The measurements of the current drawn from several LED light bulbs from different manufacturers have confirmed the presence of odd harmonics while even harmonics, subharmonics, and inter-harmonics are almost negligible. Moreover, the measurements have also confirmed a low voltage total-harmonic-distortion,

which is less than 4%. Therefore, in the following, firstly, the key equations of non-sinusoidal periodical, instantaneous electric quantities in the absence of subharmonics and inter-harmonics have been discussed.

After that, the rules and equations to obtain the components of the equivalent circuit of the LED light bulbs have been provided. The procedure to obtain the quantities to be used in the equations have been also described. Such a procedure with the aforesaid rules and equations enable to obtain the model of any LED light bulbs available on the market without the knowledge of its inner components (driver, LED package, and so on). Therefore, any researcher and practitioner can treat any LED light bulbs in the market as a black-box, and the components of the equivalent circuit model have been simply obtained by some electrical measurements. It is worth noting that the parameters of a generic LED light bulb can be obtained by a few simple current measurements to be performed at the lamp terminals (such as the active and reactive power, and some current harmonics that are measured on the line at different values of the voltage on the mains). These parameters are the coefficients of the functions obtained by linear or polynomial interpolation of the *rms* of the current harmonics.

Finally, the proposed parametric Pspice circuit that is able in emulating the current drawn by the lamps under variable voltage on the mains has been widely discussed. Then, the validation has been performed by comparing the waveforms and harmonics of the measured currents with the simulated ones for several LED light bulbs. The validation has confirmed the effectiveness and robustness of the proposed model.

3.2 Non-sinusoidal periodical electric quantities

Considering a circuit operating at steady-state conditions, the non-sinusoidal periodical instantaneous electric quantities, that is the voltage *v(t)* and the current *i(t)*, can be represented by means of the Fourier series in the absence of subharmonics and inter-harmonics [11]:

$$v(t) = V_0 + \sqrt{2}\sum_{k\in\mathbb{N}} V_h \sin(h\omega t + \alpha_k)$$
$$i(t) = I_0 + \sqrt{2}\sum_{k\in\mathbb{N}} I_h \sin(h\omega t + \beta_k) \quad (40)$$

Key terms are the power system fundamental frequency of the voltage, $v_1(t)$, and current, $i_1(t)$ [11]:

$$v_1(t) = \sqrt{2}V_1 \sin(\omega t + \alpha_1)$$
$$i_1(t) = \sqrt{2}I_1 \sin(\omega t + \beta_1) \tag{41}$$

Grouping the constant term with the harmonics [11]:

$$v_H(t) = V_0 + \sqrt{2}\sum_{k\in\mathbb{N}} V_k \sin(k\omega t + \alpha_k)$$
$$i_H(t) = I_0 + \sqrt{2}\sum_{k\in\mathbb{N}} I_k \sin(k\omega t + \beta_k) \tag{42}$$

any non-sinusoidal periodical instantaneous electric quantity can be summarized according to the IEEE Std-1459 [11]:

$$v(t) = v_1(t) + v_H(t)$$
$$i(t) = i_1(t) + i_H(t) \tag{43}$$

Without loss of generality, it can be set:

$$\alpha_k = \delta_k + \frac{\pi}{2}$$
$$\beta_k = \gamma_k + \frac{\pi}{2} \tag{44}$$

and also $\delta_1 = 0$. Therefore:

$$v_1(t) = \sqrt{2}V_1 \cos(\omega t)$$
$$v_k(t) = \sqrt{2}V_k \cos(k\omega t + \delta_k)$$
$$i_1(t) = \sqrt{2}I_1 \cos(\omega t + \gamma_1)$$
$$i_k(t) = \sqrt{2}I_k \cos(k\omega t + \gamma_k) \tag{45}$$

The instantaneous power related to the fundamental frequency deriving from these equations is:

$$p_1(t) = v_1(t)i_1(t) = V_1 I_1 \cos(\gamma_1)\,[1 + \cos(2\omega t)] - V_1 I_1 \sin(\gamma_1)\sin(2\omega t) = \\ = P_1[1 + \cos(2\omega t)] - Q_1 \sin(2\omega t) \tag{46}$$

and the fundamental apparent power, S_1, is then obtained from the fundamental active power, P_1, and the fundamental reactive power, Q_1, through the following equation [11]:

$$S_1^2 = P_1^2 + Q_1^2 \tag{47}$$

that, in turn, is part of the overall apparent power, *S*, that includes the harmonics contribution (that is the non-fundamental apparent power) [11]:

$$S^2 = S_1^2 + D_I^2 + D_V^2 + S_H^2 \tag{48}$$

where, the current distortion power, D_I, the voltage distortion power, D_V, and the harmonic apparent power, S_H, are obtained from the evaluation of the *rms* value of $v_H(t)$, that is V_H, and $i_H(t)$, that is I_H [11]:

$$\begin{aligned} D_I^2 &= V_1^2 I_H^2 \\ D_V^2 &= I_1^2 V_H^2 \\ S_H^2 &= V_H^2 I_H^2 \end{aligned} \tag{49}$$

The harmonics related to the voltage on the mains are negligible in comparison with the current harmonics, it is also confirmed by the measurements. Consequently, the term $v_H(t)$ in (43) can be neglected, then the apparent power is approximated to:

$$S^2 = P_1^2 + Q_1^2 + D_I^2 \tag{50}$$

Therefore, the modeling of the current harmonics enables to estimate the non-active powers *Q1* and D_I that involve undesired power losses in the line. It is worth noting that, while the current harmonics pertain to the undesired term D_I, the fundamental current affects the active power as well as the useless power Q_1. Therefore, it is useful to consider the fundamental current divided into two components [89-90]:

$$\begin{aligned} i_1(t) &= i_{P1}(t) + i_{Q1}(t) \\ i_{P1}(t) &= \sqrt{2} I_{P1} \cos(\omega t) = \sqrt{2} I_1 \cos(\gamma_1) \cos(\omega t) \\ i_{Q1}(t) &= \sqrt{2} I_{Q1} \cos\left(\omega t + \frac{\pi}{2}\right) = \sqrt{2} I_1 \sin(\gamma_1) \cos\left(\omega t + \frac{\pi}{2}\right) \end{aligned} \tag{51}$$

It is easy to prove that:

$$\begin{aligned} v_1(t) i_{P1}(t) &= V_1 I_1 \cos(\gamma_1) \left[1 + \cos(2\omega t)\right] = P_1 [1 + \cos(2\omega t)] \\ v_1(t) i_{Q1}(t) &= V_1 I_1 \sin(\gamma_1) \left[-\sin(2\omega t)\right] = -Q_1 \sin(2\omega t) \end{aligned} \tag{52}$$

Therefore, the term $i_{P1}(t)$ affects only the active power, then in the following, it is called "active current". The term $i_{Q1}(t)$, affects only the reactive power, that it is called "reactive current". Finally, as expected, in all performed tests for all the lamps, the phase shift of the

fundamental frequency current drawn has been always $-\pi/2 < \gamma_1 < \pi/2$: (with respect to the voltage on the mains), which implies a positive value of $\cos(\gamma_1)$ in (51).

3.3 Linear model for emulating the current drawn from LED light bulb

3.3.1 Description of the linear model

The measurements of the amplitude and phase shift of the fundamental and harmonic currents have to be performed in order to obtain the components of the proposed Pspice circuit. For a given LED light bulb, these measurements have to be performed by setting five voltage levels at the lamp terminals: $0.9V_{nom}$, $0.95V_{nom}$, V_{nom}, $1.05V_{nom}$, and $1.1V_{nom}$. For each current harmonic, a polynomial function has to be obtained by measurement interpolation. Similarly, polynomial functions have to be obtained for, respectively, the active and reactive current. The coefficients of these polynomial functions have to be used to select the components of the Pspice circuit according to the rules that are described in the next section. Moreover, the quantities related to these components are also related to these coefficients as described in the following. With this in mind, this section describes the test rig used to set the desired voltage levels across the lamp terminals and to perform the aforesaid measurements.

Figure 3:1 depicts the measurements of the fundamental current and the odd current harmonic amplitudes up to the 13th for a LED light bulbs. The measurements highlighted that a linear interpolation of the current harmonics turns out to be enough accurate:

$$\begin{aligned} I_{P1} &\stackrel{\text{def}}{=} I_{P1}(V_1) = a_{P1} + b_{P1}V_1 \\ I_{Q1} &\stackrel{\text{def}}{=} I_{Q1}(V_1) = a_{Q1} + b_{Q1}V_1 \\ I_k &\stackrel{\text{def}}{=} I_k(V_1) = a_k + b_kV_1 \\ k &= 2, 3, \dots K \end{aligned} \tag{53}$$

with *K* the number of harmonics considered for emulating the waveform of the current drawn from the lamp.

Remark 1 - I_{P1} is always positive regardless of its trend in (53) *because it is obtained by multiplying I_1 with $\cos(\gamma_1)$, where the former is positive by definition while the latter has been previously proved to be positive since $-\pi/2 < \gamma_1 < \pi/2$. Similar considerations are valid for I_k as well as for the terms in the related interpolation functions. On the other hand, although I_1 is positive by definition, I_{Q1} may be positive or negative, it depends on γ_1.*

Remark 2 - Considering the previous remark and that V_1 is positive by definition, at least one between a_{P1} and b_{P1} in the interpolation function have to be positive. Similar considerations are always valid for a_k and b_k, while are valid for a_{Q1} and b_{Q1} only when I_{Q1} is positive. On the other hand, when I_{Q1} is negative, a dual behavior occurs, that is at least one between a_{Q1} and b_{Q1} in the interpolation function have to be negative.

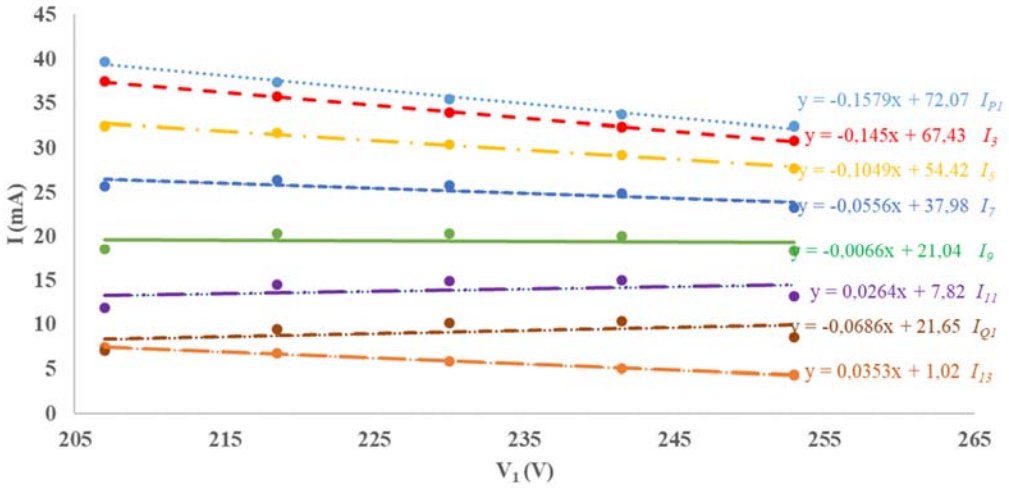


Figure 3:1 Measured amplitude of the fundamental current and greatest harmonics for a LED. The linear interpolation functions are reported on the right with the related current symbol.

In the test rig (Figure 3:2), a transformer with a continuous variable transform ratio (variac) has been connected to the mains voltage with the aim of emulating the variable voltage on the mains. In other words, each time a measurement has to be performed at a given voltage level, the variac has been properly tuned to emulate such a voltage level across the lamp terminals. The variac feeds the LED light bulb through a power analyzer used to measure the voltage across the lamp terminals as well as to measure the fundamental and harmonic currents (in terms of amplitude and phase shift) drawn. Moreover, to simultaneously observe the current harmonics amplitude and the waveforms of the voltage and current at LED light bulb terminals, an oscilloscope has been also used. More specifically, the current drawn from the LED light bulb has been displayed through the oscilloscope. The power analyzer has a 1 A shunt probe that offers a high resolution and accuracy for testing currents as low as 80 µA. This enables the meter to measure standby power as low as 20 mW at 240 V. The maximum voltage peak can reach 2kV, with an accuracy of 20mV. The power analyzer has a bandwidth of 1 MHz.

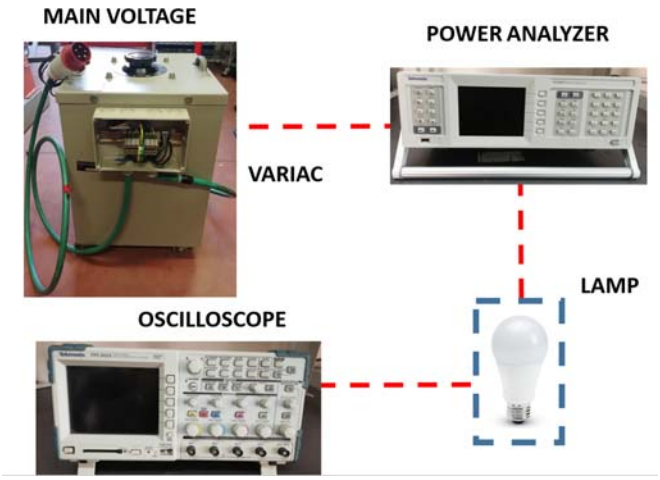


Figure 3:2 Experimental setup. A variac, connected to the mains, feeds the LED light bulb through a power analyzer that acquires the measurements. The oscilloscope displays the waveforms.

The measurements have been performed in the range of ±10% of the rated voltage due to the voltage variation that is allowed for the utility [91]. Throughout the day, the rated voltage could suffer from some variations due to the distributed renewable generators into the network, the load variations, the network configurations, and so on, without the possibility for the users to do anything about it [92].

Figure 3:3 shows the amplitude of the current harmonics normalized with respect to the fundamental one, in the case of a LED light bulb with 212V (*rms*) at its terminals. The normalized harmonic amplitudes, in blue, are sorted in ascending order and the abscissa reports the related harmonic. The figure also reports, in red, the THD error in percentage when some current harmonics are neglected, assuming as THD reference, $THD_{I,TOT}$, the one computed considering the harmonics until the 50th. More specifically, for a given harmonic, *n*, the THD error, $Error_{I,n}$, is obtained when a set of *m* harmonics are neglected. Harmonic *n* and those on its left in the figure belong to this set. The current THD reference is:

$$THD_{I,TOT} \stackrel{\text{def}}{=} \sqrt{\frac{\sum_{k=2}^{K} {I_k}^2}{{I_1}^2}} \tag{54}$$

while the THD referred to a given current harmonic *n*, $THD_{I,n}$, is computed subtracting the aforesaid *m* current harmonic amplitudes:

$$THD_{I,n} = \sqrt{\frac{\sum_{p=m+1}^{K} {\widehat{I}_p}^2}{{I_1}^2}} \tag{55}$$

with $\hat{I}$ an array where the amplitudes of the current harmonics have been ascending sorted and *p* indicates the position in the sequence. Consequentially the percentage error referred to the $THD_{I,n}$ is equal to:

$$Error_{I,n}(\%) = 100\frac{THD_{I,TOT} - THD_{I,n}}{THD_{I,TOT}} \tag{56}$$

In the THD error diagram, the first red point on the left has been calculated by removing from the total current the harmonic that has the smallest amplitude (that is the 50th), the second point is calculated neglecting the two smallest current amplitude (that is the 50 th and 48 th) and so on until it is removed the 3-rd current harmonic.

Figure 3:3 depicts the normalized current harmonics and the THD percentage error for a generic LED light bulb. It is less to 1% by removing the smallest *m*=41 (that is *n*=15) current harmonics (that is considering only the 3rd, 5th, 7th, 9th, 11th, 13th, 17th, and 19th harmonic). On the other hand, by removing *m*=46 harmonics, n=9 (considering only the 3rd, 5^{th,} and 7th), the percentage error is less than 10%. Figure 3:4 reports the quantities for the LED when the voltage is 237V.

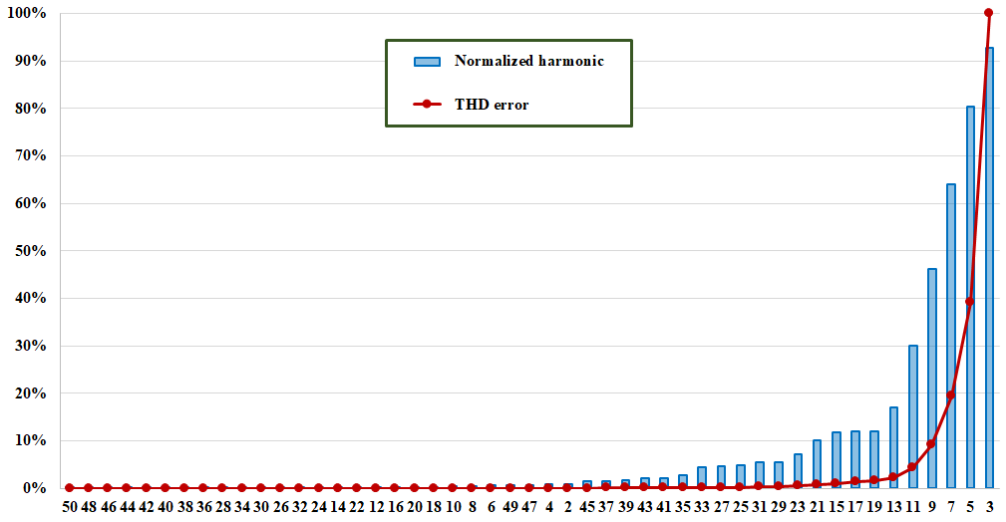


Figure 3:3 Normalized current harmonics and THD error, when the LED light bulb is feed with 212V.

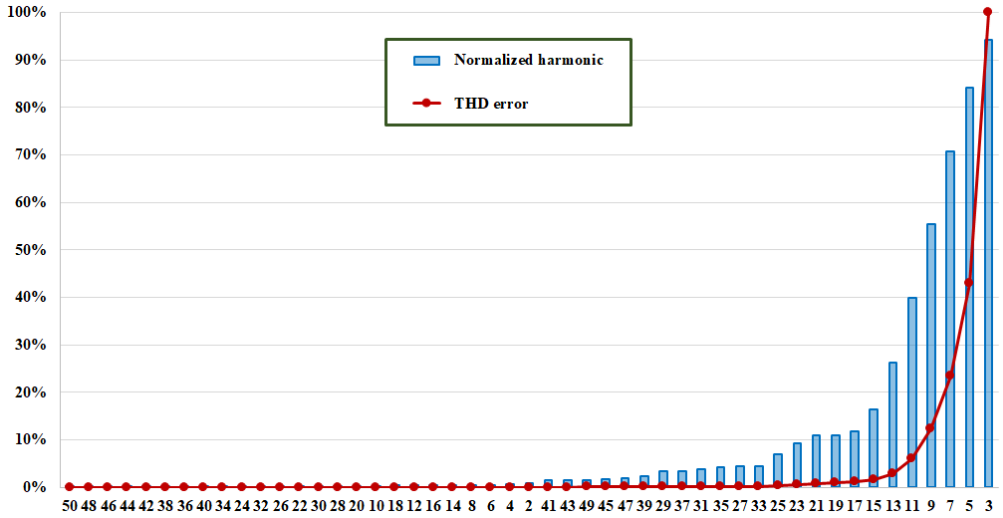


Figure 3:4 Normalized current harmonics and THD error, when the LED light bulb is feed with 237V.

The proposed circuit model accounts for the change of the current drawn from a LED light bulb when the *rms* voltage, V_1, on the mains varies within the range allowed by the regulation (±10% of V_{nom}). More specifically, the model emulates the variation of the value of the *rms*, I_1, and the change in the phase shift, γ_1, of the fundamental frequency current, $i_1(t)$. The model also emulates the variation of the *rms* of any other current harmonic, I_k, while it neglects any variation of the phase offset, γ_k (that is the phase offset at nominal voltage is considered). A graphical representation of the proposed circuit that accounts for the previous interpolation functions is reported in Figure 3:5.

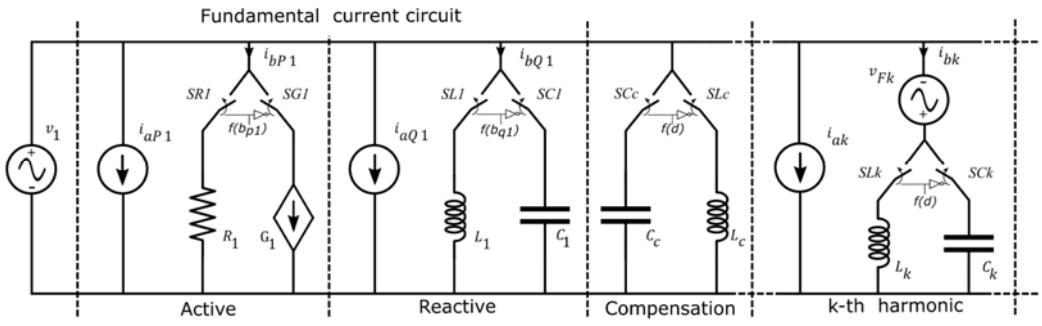


Figure 3:5 Proposed linear equivalent circuit of a generic LED light bulb.

The components in the subcircuits called “Active”, “Reactive” and “k-th harmonic” emulate the behavior of, respectively, I_{P1}, I_{Q1} and I_k in (53). According to the circuit model in the figure and the equations in (53), the following equations are valid:

$$\overbrace{i_{aP1}(t) + i_{bP1}(t)}^{circuit} = i_{P1}(t) = \sqrt{2} I_{P1} \cos(\omega t) = \sqrt{2}\overbrace{[a_{P1} + b_{P1} V_1]}^{interpolation} \cos(\omega t)$$

$$i_{aQ1}(t) + i_{bQ1}(t) = i_{Q1}(t) = \sqrt{2} I_{Q1} \cos\left(\omega t + \frac{\pi}{2}\right) = \sqrt{2}\left[a_{Q1} + b_{Q1} V_1\right] \cos\left(\omega t + \frac{\pi}{2}\right) \quad (57)$$

$$i_{ak}(t) + i_{bk}(t) = i_k(t) = \sqrt{2} I_k \cos(k\omega t + \gamma_k) = \sqrt{2}[a_k + b_k V_1] \cos(k\omega t + \gamma_k)$$
$$k = 2, 3, \ldots K$$

Then $i_{aP1}(t)$ accounts for the constant term a_{P1}, $i_{bP1}(t)$ accounts for the linear term b_{P1} and so on:

$$\begin{gathered} i_{aP1}(t) = \sqrt{2} a_{P1} \cos(\omega t) \\ i_{bP1}(t) = \sqrt{2} b_{P1} V_1 \cos(\omega t) \\ i_{aQ1}(t) = \sqrt{2} a_{Q1} \cos\left(\omega t + \frac{\pi}{2}\right) \\ i_{bQ1}(t) = \sqrt{2} b_{Q1} V_1 \cos\left(\omega t + \frac{\pi}{2}\right) \\ i_{ak}(t) = \sqrt{2} a_k \cos(k\omega t + \gamma_k) \\ i_{bk}(t) = \sqrt{2} b_k V_1 \cos(k\omega t + \gamma_k) \end{gathered} \quad (58)$$

In the previous equations, the currents $i_{aP1}(t)$, $i_{aQ1}(t)$ and $i_{ak}(t)$ are independent from V_1 since they arise from the constant terms in (53). Therefore, their waveforms are emulated by means of independent current generators in the equivalent circuit (Figure 3:5).

It is useful to recall that when a constant term is negative (for example $a_k < 0$) the related generator ($i_{ak}(t)$ in such an example) is in antiphase with the overall current it belongs to ($i_k(t)$ in such an example). Consequently, according to *Remark 2*, the other term (b_k in such an example) is definitively positive because the related current ($i_{bk}(t)$ in such an example) has to be in phase with the overall current. Moreover, the amplitude of the “in-phase” current ($i_{bk}(t)$) is greater than the amplitude of the “antiphase” current ($i_{ak}(t)$) according to *Remark 1*.

The voltage-independent generator, v_{Fk}, with an element in the series, is responsible for emulating the current $i_{bk}(t)$. The voltage-independent generator has an angular frequency *k* times greater than the mains voltage and the same amplitude:

$$v_{Fk}(t) = \sqrt{2}V_1 \cos\left(k\omega t + \gamma_k + sign(b_k)d\frac{\pi}{2}\right) \quad (59)$$

where γ_k is the phase offset of the *k*-th harmonic current according to the equations in (45); *d* can assume only two values +1 or -1, it depends on the component selected by the switches.

When the circuit component adopted is an inductor then *d*=1, otherwise, when it is chosen a capacitor *d*=-1. It is worth noting that this voltage generator does not emulate the *k*-th voltage harmonic on the mains but it is a fictitious generator belonging to the lamp model.

By using the superposition theorem, it can be noted that such a fictitious voltage-independent generator supplies only the aforesaid component, e.g. the inductor when *d*=1 (see Figure 3:6). Therefore, at steady-state, when an inductor L_k is adopted, the steady-state current through it due to v_{Fk} is:

$$i_{Lk}(t) = \frac{\sqrt{2}V_1}{k\omega L_k}\cos\left(k\omega t + \gamma_k + sign(b_k)\frac{\pi}{2} - \frac{\pi}{2}\right) \quad (60)$$

When b_k is positive, the phase of $i_{bk}(t)$ is $k\omega t + \gamma_k$ and the previous equation becomes:

$$i_{Lk}(t) = \frac{\sqrt{2}V_1}{k\omega L_k}\cos(k\omega t + \gamma_k) \quad (61)$$

that is $i_{Lk}(t)$ presents the same phase of $i_{bk}(t)$. These currents can present also the same amplitude by properly choosing L_k:

$$L_k = \frac{1}{k\omega b_k} \quad \xrightarrow{yields} \quad i_{Lk}(t) = i_{bk}(t)\ when\ b_k > 0 \quad (62)$$

When b_k is negative, the phase of $i_{bk}(t)$ is $k\omega t + \gamma_k - \pi$ since this current is in antiphase with $i_k(t)$, moreover (60) becomes:

$$i_{Lk}(t) = \frac{\sqrt{2}V_1}{k\omega L_k}\cos(k\omega t + \gamma_k - \pi) \quad (63)$$

Once again $i_{Lk}(t)$ presents the same phase offset of $i_{bk}(t)$ thanks to the adopted waveform of the fictitious voltage generator. These currents can present also the same amplitude by properly choosing L_k:

$$L_k = \frac{1}{k\omega(-b_k)} \quad \xrightarrow{yields} \quad i_{Lk}(t) = i_{bk}(t)\ when\ b_k < 0 \quad (64)$$

Therefore, by using a fictitious voltage generator with the waveform reported in (59) and an inductor is always possible to emulate the linear term b_k:

$$L_k = \frac{1}{k\omega|b_k|} \quad \xrightarrow{yields} \quad i_{Lk}(t) = i_{bk}(t) \; \forall \; b_k \neq 0 \tag{65}$$

When b_k is equal to 0, the amplitude of I_k is independent from the voltage on the mains, then only the independent current generator is considered while the fictitious independent voltage generator and the inductor are removed.

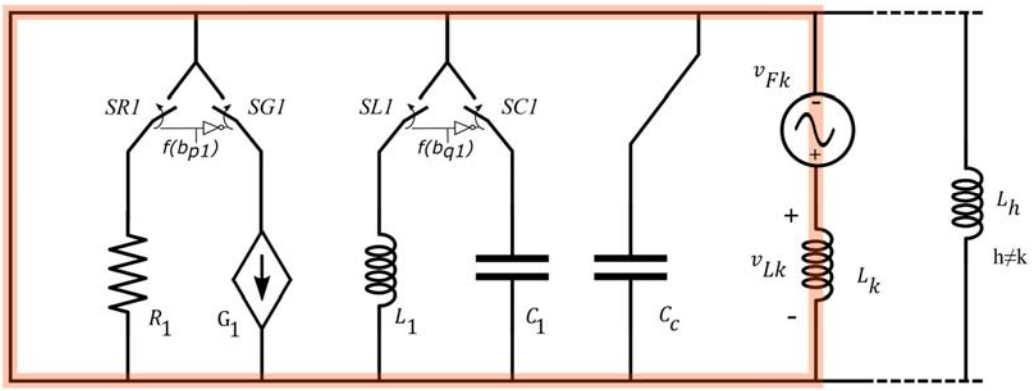


Figure 3:6 Equivalent circuit when only vFk works while the other independent generators are turned off. It is apparent that this generator supplies only Lk.

When a capacitor C_k is adopted (then d=-1) the steady-state current through it due to v_{Fk} is:

$$i_{Ck}(t) = k\omega C_k \sqrt{2} V_1 \cos\left(k\omega t + \gamma_k - sign(b_k)\frac{\pi}{2} + \frac{\pi}{2}\right) \tag{66}$$

When b_k is positive the previous equation becomes:

$$i_{Ck}(t) = k\omega C_k \sqrt{2} V_1 \cos(k\omega t + \gamma_k) \tag{67}$$

that is $i_{Ck}(t)$ presents the same phase of $i_{bk}(t)$ like the previous case where an inductor has been considered. These currents can present also the same amplitude by properly choosing C_k:

$$C_k = \frac{b_k}{k\omega} \quad \xrightarrow{yields} \quad i_{Ck}(t) = i_{bk}(t) \; when \; b_k > 0 \tag{68}$$

and more in general, also using the fictitious voltage (59) and a capacitor is always possible to emulate the linear term b_k:

$$C_k = \frac{|b_k|}{k\omega} \quad \xrightarrow{yields} \quad i_{Ck}(t) = i_{bk}(t) \; \forall \; b_k \neq 0 \tag{69}$$

In [89] and [90] have been presented, respectively, a circuit model (called “fundamental current circuit”, Figure 3:5) of the active and reactive current as well as the related Pspice model. The model of the fundamental current has been slightly modified in this work and for the sake of completeness, the main considerations and relations are reported in the following.

The active current has to be in phase with the mains voltage since the lamp is a load. Notwithstanding, when the constant term, a_{P1}, is negative the independent current generator is in antiphase with the mains voltage. On the other hand, in such a case, the term b_{P1} has to be positive according to Remark 2, that is the current i_{bP1} must be in phase with the mains voltage. Moreover, its amplitude has to exceed the other in the voltage range of application (±10% of V_{nom}). Similarly, when the linear term, b_{P1}, is negative the current i_{bP1} is in antiphase with the mains voltage, but the term a_{P1} is positive (according to Remark 2) and enough to ensure that the overall active current is in phase with the mains voltage in the range of application of the model. It is worth to note that negative values of b_{P1} highlights a reduction of the active current drawn from the lamp as the mains voltage increases. Therefore, in the Pspice circuit a resistor is adopted when i_{bP1} is positive (to emulate an increasing current in phase with the mains voltage), otherwise, a voltage-controlled current source (VCCS), *G1*, is considered:

$$R_1 = \frac{1}{b_{P1}} \quad when \quad b_{P1} > 0$$
$$VCCS\ gain = b_{P1} \quad when \quad b_{P1} < 0 \tag{70}$$

Finally, no issues arise when both terms are positive. In such a case the independent generator is in phase with the mains voltage and a resistor is adopted to emulate the increasing active current drawn by the lamp as the voltage on the mains increases.

When I_{Q1} is positive, the reactive current leads to the mains voltage. In such a case, if the constant term, a_{Q1}, is negative then the related independent current generator lags the mains voltage. Therefore, the term b_{Q1} has to be positive (according to Remark 2), that is the current i_{bQ1} must lead the mains voltage. Moreover, its amplitude has to exceed the other in the voltage range of application (±10% of V_{nom}). Similarly, when the linear term, b_{Q1}, is negative, the current i_{bQ1} lags the mains voltage, but the term a_{P1} is positive (according to Remark 2) and enough to ensure that the overall reactive current leads the mains voltage in the range of application of the model. It is worth to note that, in this specific case, negative values of b_{Q1} means a reduction of the reactive current drawn from the lamp as the mains voltage increases.

Dually, when I_{Q1} is negative, the reactive current lags the mains voltage. In such a case, if the constant term, a_{Q1}, is positive then the related independent current generator leads the

mains voltage. Therefore, the term b_{Q1} has to be negative (according to Remark 2), that is the current i_{bQ1} must lag the mains voltage. Moreover, its amplitude has to exceed the other in the voltage range of application (±10% of V_{nom}). Similarly, when the linear term, b_{Q1}, is positive, the current i_{bQ1} leads the mains voltage, but the term a_{P1} is negative (according to Remark 2) and enough to ensure that the overall reactive current lags the mains voltage in the range of application of the model. It is worth noting that, in this specific case, a positive value of b_{Q1} means a reduction of the reactive current drawn from the lamp as the mains voltage increases. Figure 3:1 represents graphically the previous cases.

Whatever I_{Q1}, a capacitor may be adopted in the model when i_{bQ1} leads the mains voltage and an inductor when i_{bQ1} lags the mains voltage:

$$C_1 = \frac{b_{Q1}}{\omega} \quad when \quad b_{Q1} > 0$$
$$L_1 = \frac{1}{\omega(-b_{Q1})} \quad when \quad b_{Q1} < 0 \tag{71}$$

It is worth to note that there is a crucial difference between these components and the others described before (L_k and C_k). More specifically, when b_{Q1} is positive a capacitor must be used in the Pspice circuit, while when b_k is positive L_k and C_k can be equally used in the Pspice model. On the other hand, once the component (L_k or C_k) is chosen the waveform of the fictitious independent voltage generator cannot be chosen arbitrarily since the value of *d* is fixed by the component choice.

By using the superposition theorem, it can be noted that the voltage-independent generator representing the mains voltage supplies the “fundamental current circuit” and also the components (L_k, C_k) adopted for emulating the current harmonics. Figure 3:7 easily makes evident such a consideration. Therefore, undesired reactive currents flow through these components. These currents have to be eliminated to ensure that the reactive current is given only by the “fundamental current circuit”. This goal is reached by adding a compensation component (L_C or C_C) which is resonant at the fundamental frequency with the equivalent component (C_{EQ} or L_{EQ}) downstream form it:

$$L_{EQ} = \frac{1}{\sum_{k=2}^{K} k\omega|b_k|} \Rightarrow C_C = \frac{1}{\omega^2 L_{EQ}} = \frac{\sum_{k=2}^{K} k|b_k|}{\omega}$$
$$C_{EQ} = \sum_{k=2}^{K} \frac{|b_k|}{k\omega} \Rightarrow L_C = \frac{1}{\omega^2 C_{EQ}} = \frac{1}{\omega \sum_{k=2}^{K} \frac{|b_k|}{k}} \tag{72}$$

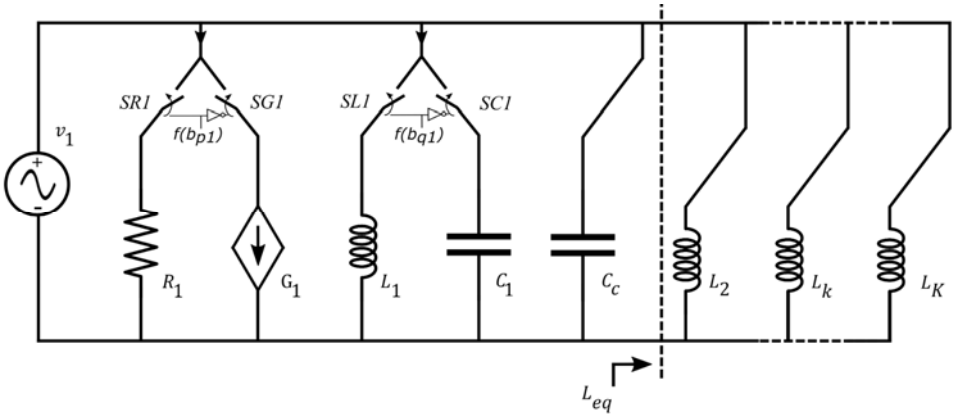


Figure 3:7 Equivalent circuit when only v1 works while the other independent generators are turned off. It is apparent that a current at the fundamental frequency flows through Leq. Cc is thus accorded to nullify the fundamental current downstream from the "fundamental current circuit".

Starting from the previous considerations and equations, the netlist (that is the circuit description file .CIR) can be obtained and simulated in Pspice. Indeed, Pspice impedes the simulation of the considered circuit "as is" when L_k is considered due to the presence of loop with only voltage sources and inductors. This obstacle can be easily overcome by adding a resistor, R_{loop}, in each loop (Figure 3:8). A small value of resistance has to be used since the resistor negatively affects the ability of the Pspice circuit in emulating the measured current.

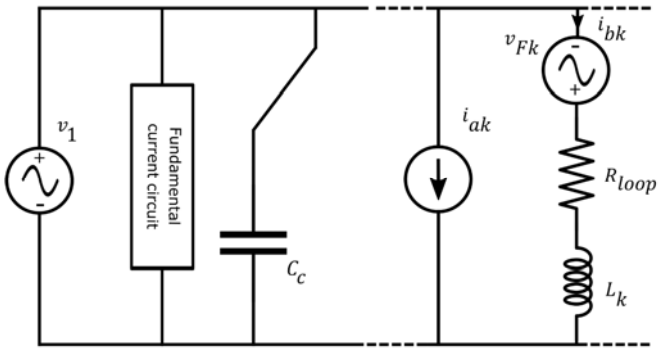


Figure 3:8 Resistance Rloop not belonging to the proposed model but necessary to enable PSpice simulation.

It is worth to underline that the proposed model enables to emulate the steady-state current drawn by the lamp while it is not able in emulating the transient (inrush current and so on [93]) at the turn on. On the other hand, the waveforms in the Pspice circuit are obtained by using a transient analysis, then the simulation period has to be enough to ensure the steady-state condition is reached.

When only capacitors are used for emulating the current harmonics, the voltage across C_k is imposed by the related loop (Figure 3:9):

$$v_{Ck}(t) = v_1(t) + v_{Fk}(t) \tag{73}$$

According to Kirchhoff's voltage law (KVL), the voltage across the capacitors is imposed, and then it is already at steady-state when the Pspice transient analysis starts.

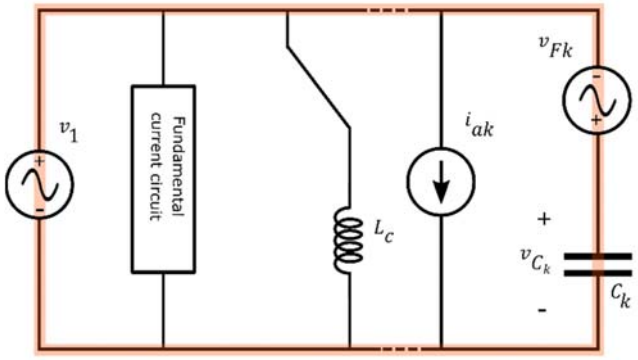


Figure 3:9 KVL for obtaining the voltage across a capacitor adopted in the k-th harmonic circuit.

The use of these capacitors asks for inserting a compensation inductor, L_C, resonant at the fundamental frequency with the equivalent capacitor C_{EQ}. As said before a resistor has to be added in series with the inductor to avoid the loop (L_C - v_1) which impedes simulation starts. Unfortunately, the current across this inductor is not yet at steady-state when the Pspice transient analysis starts and recalling the standard expression of the current in a resistor–inductor circuit:

$$i_{L_C}(t) = \left[i_{L_C}(0) - i_{L_CSS}(0)\right]e^{-\frac{R}{L_C}t} + i_{L_CSS}(t) \tag{74}$$

it is evident that the smaller the resistance the greater the time required to reach a steady-state condition. In other words, the use of small resistance provides more accurate results but at the cost of long simulation time. To solve this problem, the initial condition value has to nullify the transient current across the compensation inductor, L_C, that is:

$$i_{L_C}(0) = i_{L_CSS}(0) \implies i_{L_C}(t) = i_{L_CSS}(t) \tag{75}$$

Given the expression of the current across the inductor at steady-state when $R \to 0$, that implies $v_{Lc}(t) \longrightarrow v_1(t)$:

$$i_{L_C}(t) = i_{L_CSS}(t) \approx \frac{\sqrt{2}V_1}{\omega L_C}\cos\left(\omega t - \frac{\pi}{2}\right) \tag{76}$$

the initial condition to be set is easily obtained:

$$i_{L_C}(0) = 0 \tag{77}$$

To nullify the effect of R_{loop} (which is not present in the proposed model), a voltage-controlled voltage source (VCVS) is placed in series with the resistor. More specifically, it is controlled by the voltage across the resistor with a gain equal to -1, thus obtaining that the following relation is valid for any resistance value Figure 3:10:

$$v_{L_C}(t) = v_1(t) \tag{78}$$

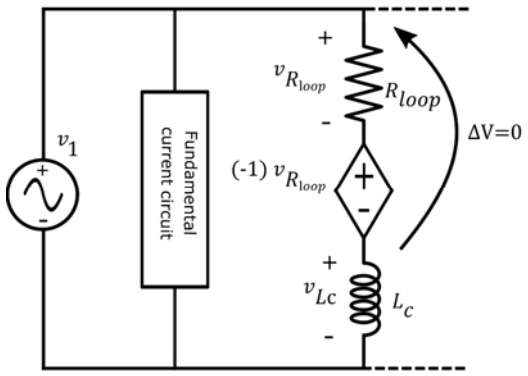


Figure 3:10 VCCS that nullifies the effect of R_{loop}, thus obtaining a Pspice circuit that actually implements the proposed model.

Therefore, setting the initial condition equal to zero enables a steady-state current through the inductor when the Pspice transient analysis starts, regardless of the value of R_{loop}. Moreover, nullifying the effect of the resistor enables to obtain a Pspice circuit that actually implements the proposed model. It is worth noting that the use of the VCVS without properly setting the initial condition enables to start the simulation but it does not address the underlining issues that lead Pspice to impede the simulation of the circuit where a loop with only voltage sources and inductors is present. Finally, it is worth recalling that the steady-state current across the inductor has the same amplitude of the fundamental current flowing through the equivalent capacitor but these currents are in the antiphase between them. Then the resulting fundamental current is zero which means, in turn, that the fundamental current flows only in the "fundamental current circuit".

As said before, whether b_{q1} is positive a capacitor is used in the "fundamental current circuit", then the voltage across it is equal to v_1 according to the related KVL, then the voltage is also already at steady-state when the Pspice transient analysis starts. On the other hand, when b_{q1} is negative an inductor has to be adopted and, consequently, a resistor R_{loop} with

the related VCVS has to be adopted and the initial condition has to be properly set (once again it has to be set equal to zero).

The mechanism adopted for these inductors can be readapted when L_k is used instead of C_k. At steady-state the voltage across the inductor is (Figure 3:9):

$$v_{Lk}(t) = v_1(t) + v_{Fk}(t) = \sqrt{2}V_1\left[\cos(\omega t) + \cos\left(k\omega t + \gamma_k + sign(b_k)\frac{\pi}{2}\right)\right] \tag{79}$$

Then the steady-state current is:

$$i_{LkSS}(t) = \sqrt{2}V_1\left[\frac{\cos\left(\omega t - \frac{\pi}{2}\right)}{\omega L_k} + \frac{\cos\left(k\omega t + \gamma_k + sign(b_k)\frac{\pi}{2} - \frac{\pi}{2}\right)}{k\omega L_k}\right] \tag{80}$$

Consequently, the initial condition to set in order to obtain a zero transient time for the current through the inductor is:

$$i_{Lk}(0) = i_{LkSS}(0) = \frac{\sqrt{2}V_1}{k\omega L_k}\cos\left(\gamma_k + sign(b_k)\frac{\pi}{2} - \frac{\pi}{2}\right) \tag{81}$$

The switches in the model (Figure 3:5) have been emulated in Pspice with "Voltage-Controlled Switch" (VCS) components. On the other hand, the VCS is not an ideal switch as the ones considered in the model. More specifically, a VCS is a resistor with a high resistance, R_{OFF}, when it emulates the open-status while the closed-status is obtained by considering a low resistance, R_{ON}. The VCS resistance is set according to the voltage value of the controlling nodes. It is worth noting that, the switch SR1 and SG1 (Figure 3:5) have to be controlled by the same voltage but with opposite logic since when the former is open the latter is closed and vice versa. Therefore, to drive these switches, a fictitious constant voltage generator has been considered:

$$V_{bp1} = sign(b_{P1}) \tag{82}$$

and

$$R_{SR1} = \begin{cases} R_{ON} & when\ V_{bp1} = 1 \\ R_{OFF} & when\ V_{bp1} = -1 \end{cases} \tag{83}$$

$$R_{SG1} = \begin{cases} R_{ON} & when\ V_{bp1} = -1 \\ R_{OFF} & when\ V_{bp1} = 1 \end{cases} \tag{84}$$

A similar mechanism can be adopted for the couple of switches *SL1-SC1*, *SCc-SLc,* and *SLk-SCk*.

Regardless of the status of a switch, the related resistance does not belong to the proposed model. Hence, similarly to R_{loop}, their effect should be nullified. It is worth to note, that the switch should ideally be a short-circuit when it is closed (that is R_{ON} should be ideally zero). Therefore, the insertion of a VCVS that nullifies the effect of R_{ON} indeed enables to emulate a short circuit (as shown in Figure 3:11), thus, once again, the Pspice circuit actually implements the proposed model. On the other hand, R_{OFF} emulates an open-circuit and, consequently, the addition of the VCVS is undesired in such a case. Notwithstanding, as the VCVS nullifies the effect of R_{ON}, dually a current-controlled current source (CCCS) placed in parallel with R_{OFF} enables to nullify its effect, that is it enables to obtain the desired open circuit. More specifically, it is controlled by the current through the resistor with a gain equal to -1, thus obtaining that the circuit element downstream from the switch have not any effect on the current drawn from the lamp circuit model.

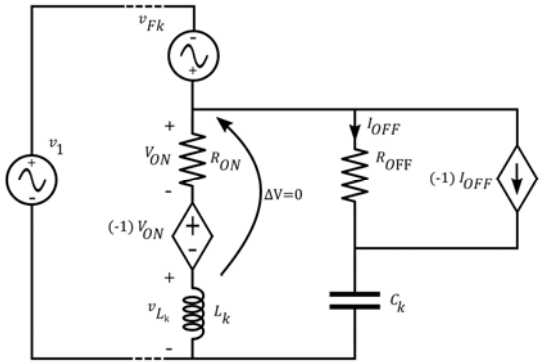


Figure 3:11 A VCCS and a CCCS used to emulate, respectively, a short circuit and an open circuit when L_k is selected (that is d=1, then L_k is connected in the lamp model while C_k is disconnected).

The parametric Pspice circuits of the generic model of an ESL are reported in Figure 3:12. It is worth noting that all voltage and current waveforms have been previously defined in terms of the "cosine" function while Pspice adopts the "sine" function; hence π/2 has been added in all the independent generators used in the Pspice netlist. The phase shift of the harmonics has been accordingly modified accounting for the related frequency.

Figure 3:12 is the main Pspice circuit of a generic ESL, where "freq" is the fundamental frequency, *V1* is the *rms* of the voltage on the main assumed to be purely sinusoidal and d is the aforesaid parameter used for considering an inductor (d=1) or a capacitor (d=-1) in each harmonic subcircuit. The switches models "swpos" and "swneg" are used to emulate the complementary operated switches. They are used in combination with the fictitious independent generators *Vbp1*, *Vbq1,* and *Vd* to drive the couple of switches *SR1-SG1*, *SL1-SC1* and *SL-SC*. Finally, *Xp1*, *Xq1,* and *Xksim* are the instances of, respectively, the active, reactive, and harmonics currents, while *X1* is the instance of the compensation subcircuit. The

parameters *ap1, bp1, aq1, bq1, ls, cs, gamma2, a2, b2,* and so on until *gamma50, a50, b50* can be reported in an external file for each lamp and then used with a ".INC" statement. The parameters *ls* and *cs* refer to the series in equations (72).

Figure 3:13 reports the netlist related to the active current, where the nodes 1 and 2 are the local numbering of the lamp terminals (which are node 1 and 0 of the Pspice lamp model as evident from the instance *Xp1* in Figure 3:12); the nodes 3 and 4 are the local numbering of the terminals (which are node 2 and 0 of the Pspice lamp model) of the voltage controlling the switches status; "freq" is the fundamental frequency (50 Hz is the default value); *a* and *b* are a_{P1} and b_{P1}. Then, the actual nodes numbering as well as the parameter values depend on the calling instance *Xp1*. *SR1* and *SG1* are the switches complementary operated to ensure that only one between the resistor, *R1*, and the VCCS are connected. The following explanation refers to the local numbering.

When b_{p1} is a positive number the voltage across terminals 3-4 is 1 V, consequently *SR1* and *SG1* are equivalent to resistors with resistance equal to, respectively, 1μΩ (that is *ron*) and 1GΩ (that is *roff*). Moreover, the expression in the curly brackets of the VCVS *ER1* is equal to -1, while is 0 for the CCCS *FR1* (it is an open circuit). Consequently, the voltage between nodes 1-6 is equal to 0, which implies a voltage across the resistor equal to the voltage on the mains (nodes 1-2) being also 0 the voltage between nodes 6-7. At the same time, the expression in the curly brackets of the VCCS *G1* is equal to 0.

The behavior of *SR1* and *SG1* is dual to the previous one when b_{q1} is a negative number because, in such a case, the voltage across the terminals 3-4 is -1 V. Moreover, the expression in the curly brackets of the CCCS *FR1* is equal to -1, while is 0 for the VCVS *ER1*. Consequently, no current flows through *R1* according to Kirchhoff's Current Law (KCL) at node 7. At the same time, the expression in the curly brackets of the VCCS *G1* is equal to the value of b_{p1}. Therefore, only *G1* is actually connected to the lamp circuit.

Similar considerations are valid for the other sub-circuits. When a switch is closed, the VCVS in series with it presents a gain -1 that ensures the switch is equivalent to a short circuit (in this case the CCCS has a gain equal to 0, then it has not any effect). The complementary switch is open, hence its VCVS presents a gain equal to 0, having no effect, while the CCCS has a gain equal to -1 to ensure the switch behaves like an open circuit.

```
.param freq      50
.param V1        212
.param d         1
.param ron       1u
.param roff      1g
.model swpos     VSWITCH (RON={ron} ROFF={roff} VON= 1 VOFF=-1)
.model swneg     VSWITCH (RON={ron} ROFF={roff} VON=-1 VOFF= 1)
.tran  0  40m  1n  10u
.probe
Vsim   1 0          sin(0 {sqrt(2)*V1} {freq} 0 0 90)
Xp1    1 0 2 0      Ip1 PARAMS: freq={freq} a={ap1} b={bp1}
Xq1    1 0 3 0      Iq1 PARAMS: freq={freq} a={aq1} b={bq1}
X1     1 0 4 0      Comp PARAMS: freq={freq} lp={ls} cp={cs} d={d}
X2sim  1 0 4 0      Ik PARAMS: freq={freq} V1={V1} k={2} gammak={gamma2} ak={a2} bk={b2} d={d}
* other current harmonics
X50sim 1 0 4 0      Ik PARAMS: freq={freq} V1={V1} k={50} gammak={gamma50} ak={a50} bk={b50} d={d}
Vbp1   2 0          {sgn(bp1)}
Vbq1   3 0          {sgn(bq1)}
Vd     4 0          {d}
```

Figure 3:12 Netlist of the overall lamp circuit.

```
.SUBCKT  Ip1  1  2  3  4  PARAMS:  freq=50  a=0  b=0
Iap1     1 2          sin(0 {sqrt(2)*a} {freq} 0 0 {0+90})
SR1      1 5 3 4      swpos
ER1      5 6 1 5      {-(sgn(b)+1)/2}
VR0      6 7          0
FR1      1 7          VR0{-(-sgn(b)+1)/2}
R1       7 2          {1/abs(b)}
SG1      1 8 3 4      swneg
G1       8 2 1 2      {b*(-sgn(b)+1)/2}
.ENDS
```

Figure 3:13 Netlist of the active current circuit.

```
.SUBCKT  Iq1  1  2  3  4  PARAMS:  freq=50  a=0  b=0
Iaq1     1 2          sin(0 {sqrt(2)*a} {freq} 0 0 {90+90})
SL1      1 5 3 4      swneg
EL1      5 6 1 5      {-(-sgn(b)+1)/2}
VL0      6 7          0
FL1      1 7          VL0 {-(sgn(b)+1)/2}
L1       7 2          {1/(2*pi*freq*abs(b))} IC=0
SC1      1 8 3 4      swpos
EC1      8 9 1 8      {-(sgn(b)+1)/2}
VC0      9 10         0
FC1      1 10         VC0 {-(-sgn(b)+1)/2}
C1       10 2         {abs(b)/(2*pi*freq)}
.ENDS
```

Figure 3:14 Netlist of the reactive current circuit.

```
.SUBCKT  Comp  1  2  3  4  PARAMS:  freq=50  lp=0  cp=0  d=0
SL       1 5 3 4      swneg
EL       5 6 1 5      {-(-d+1)/2}
VL0      6 7          0
FL       1 7          VL0 {-(d+1)/2}
Lc       7 2          {1/(2*pi*freq*lp)} IC=0
SC       1 8 3 4      swpos
EC       8 9 1 8      {-(d+1)/2}
VC0      9 10         0
FC       1 10         VC0 {-(-d+1)/2}
Cc       10 2         {cp/(2*pi*freq)}
.ENDS
```

Figure 3:15 Netlist of the compensation circuit.

```
.SUBCKT  Ik  1  2  3  4  PARAMS:  freq=50  V1=230  k=0  gammak=0  ak=0  bk=0  d=0
Iak      1 2          sin(0 {sqrt(2)*ak} {k*freq} 0 0 {gammak+90})
VFk      5 1          sin(0 {sqrt(2)*V1} {k*freq} 0 0 {gammak+sgn(bk)*d*90+90})
SL       5 6 3 4      swpos
ERL      6 7 5 6      {-(d+1)/2}
VL0      7 8          0
FRL      5 8          VL0 {-(-d+1)/2}
Lk       8 2          {1/(2*pi*k*freq*abs(bk))}
+IC={sqrt(2)*V1*abs(bk)*cos({(gammak+sgn(bk)*d*90-90)*pi/180})}
SC       5 9 3 4      swneg
ERC      9 10 5 9     {-(-d+1)/2}
VC0      10 11        0
FRC      5 11         VC0 {-(d+1)/2}
Ck       11 2         {abs(bk)/(2*pi*k*freq)}
.ENDS
```

Figure 3:16 Netlist of the generic harmonic circuit.

3.3.2 Linear model validation

In the following, the comparison between the measured and simulated current waveforms of different LED light bulbs have been carried out. The results have highlighted the high fidelity level of the proposed linear model in emulating the current drawn by the LED light bulbs under variable voltage on the mains.

Figure 3:17 and Figure 3:18 report the measured voltage on the mains (blue waveform), the measured current (green waveform), and the simulated current (red waveform) for the two LED light bulbs when the *rms* voltage on the mains is, respectively, 212V and 237V. These two voltage levels have not been used for obtaining the parameters of the interpolation function, since these measurements have been performed only for model validation. They have been set by means of the variac similarly to the voltage level used for the interpolation functions as described before. The simulated currents that are reported in the figures have been obtained using the inductors in the harmonic subcircuits (i.e. d=1). The results confirm that the current is already at steady-state when the transient analysis starts, then the method adopted for the Pspice implementation of the current lamp model is effective. By analyzing the figures, it is also evident the goodness of the proposed Pspice model. It is worth noting that the predicted current is accurate for the LED light bulb in case of voltage on the mains exceeding the nominal value. As expected, there has been not any difference be-

tween the voltage THD during the current measurement (lamp on) and without any load (lamp off). The THD of the voltage on the mains has been measured in the interval 2%-4% during the measurements.

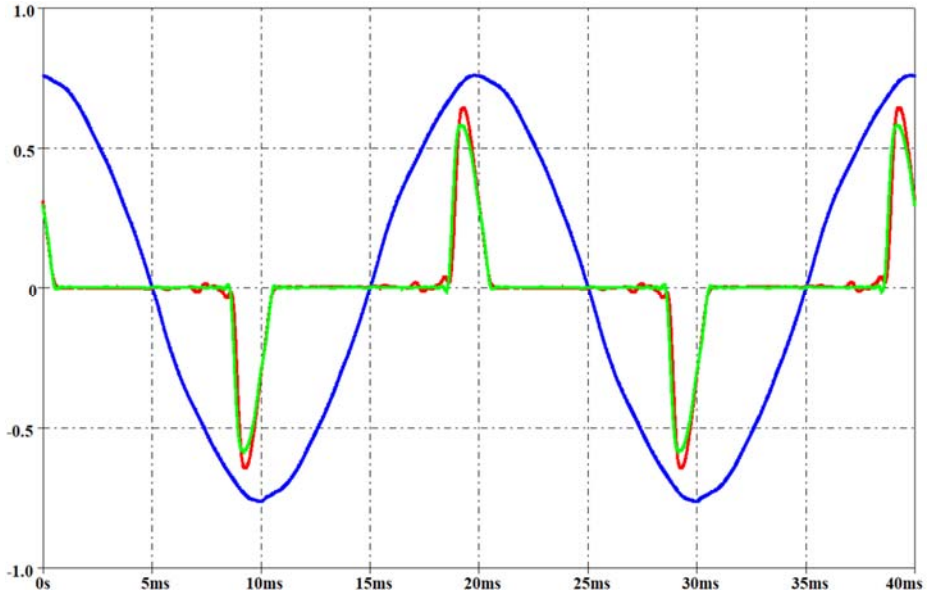


Figure 3:17 Measured voltage on the mains (blue waveform, *rms* 212V), measured current (green waveform), and simulated current (red waveform) for a LED. Per-unit system: base voltage 400V, base current 300mA.

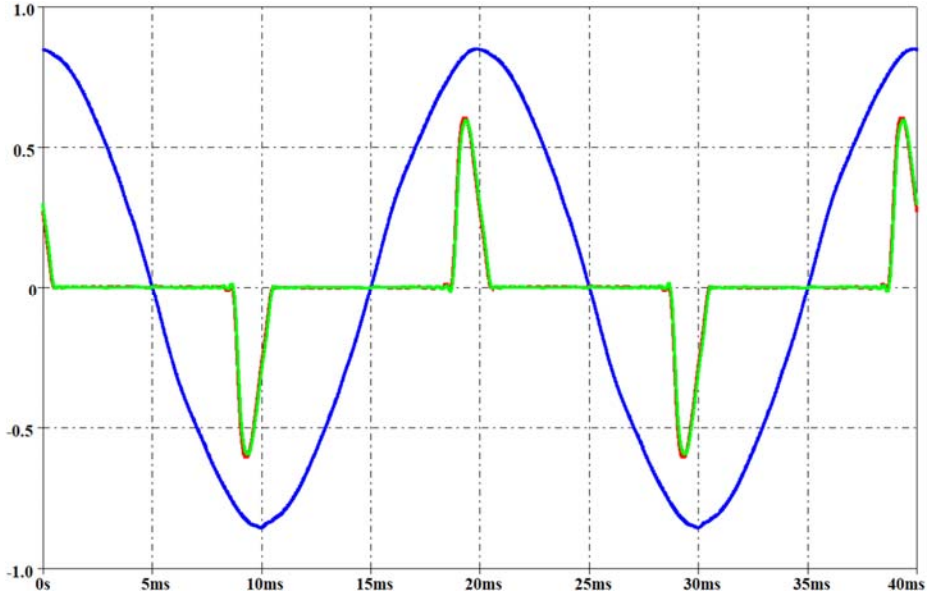


Figure 3:18 Measured voltage on the mains (blue waveform, *rms* 237V), measured current (green waveform) and simulated current (red waveform) for a LED. Per-unit system: base voltage 400V, base current 300mA.

The total number of circuit components in the active and reactive current circuit is, respectively, 8 and 11 (Figure 3:13 and Figure 3:14). The compensation circuit includes 10 components (Figure 3:15), while there are 12 components in each harmonic subcircuit (Figure 3:16). Therefore, the total number of components of the lamp Pspice circuit is 617 when the current harmonics until the 50^{th} are used. On the other hand, a reduced circuit can be obtained using a less general circuit where each switch with the related zero-voltage generator, VCVS, and CCCS are removed together with the elements to be disconnected. In such a case the number components in the active current circuit is 2. The number of components in the reactive current circuit is also 2 when the capacitor has to be considered (bq1 is positive), while is 4 when the inductor has to be considered since a resistor, R_{loop} and the related VCVS has to be considered. The adoption of only capacitors or only inductors in the harmonic subcircuit reduces its number of components to 3 in the first case, while 5 components in the second one due to the need of the resistor and VCVS. Finally, only the capacitor is adopted in the compensation circuit when the inductors are used in the harmonic subcircuits, while 3 components are necessary when an inductor has to compensate the equivalent capacitance of the harmonic subcircuits. Therefore, the smallest reduced lamp circuit has 154 components while 252 components are present in the greatest reduced circuit. It is worth noting that the reduced circuits provide the same current waveform of the one with 617 (full circuit) but each reduced circuit is related only to a given lamp.

Neglecting a current harmonic enables to remove 12 components from the full circuit (3 or 5 in the reduced ones) at cost of worsening the model accuracy. The error on the current THD described before has been used as a criterion for choosing the harmonic to be considered. Two levels of maximum THD error have been considered: 1% and 10%. It is worth noticing that each time a group of harmonics is neglected and the related components removed from the Pspice circuit the value of L_{EQ} (or C_{EQ}) changes, then the resonant (at the fundamental frequency) component in the compensation circuit have to be properly accorded. Figure 3:19 and Figure 3:20 report the measured current (green waveform) and the simulated current involving a THD error of 1% (red waveform) and 10% (blue waveform) for a LED light bulb at the two aforementioned voltage levels adopted for model validation. The harmonics neglected for achieving a given THD error refer to Figure 3:3 and Figure 3:4. It is worth noting that the reduced circuit performing a THD error of 1% contains less than 40 components.

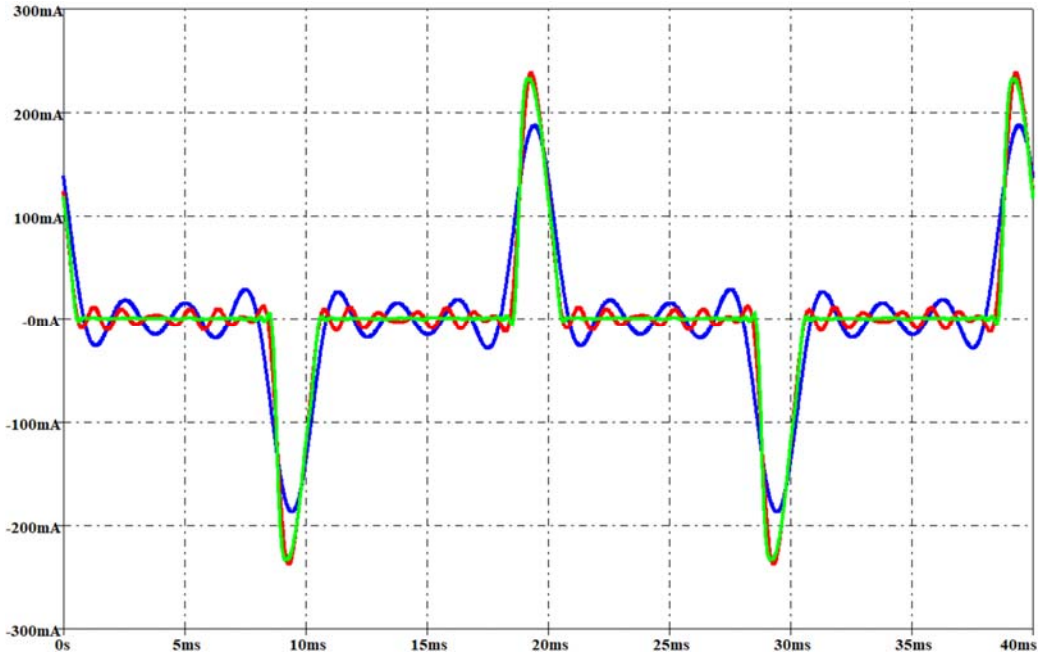


Figure 3:19 LED light bulb: measured current (green waveform) and the simulated current involving a THD error of 1% (red waveform) and 10% (blue waveform) with a rms voltage of 212V.

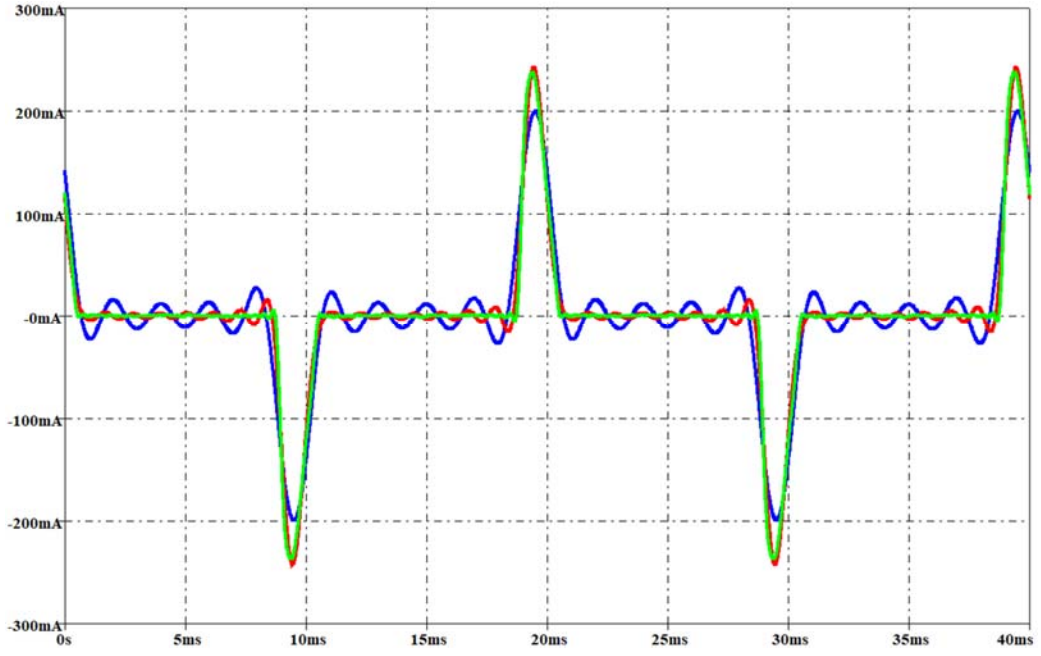


Figure 3:20 LED light bulb: measured current (green waveform) and the simulated current involving a THD error of 1% (red waveform) and 10% (blue waveform) with a *rms* voltage of 237V.

3.4 Nonlinear model for emulating the current drawn from a LED light bulb

3.4.1 Description of the nonlinear model

The next stage of the research proposal has the aim to increase the effectiveness of the previous model. In this perspective, nonlinear interpolation functions have been taken into account. More specifically, bearing in mind the relations in (53), it has been considered a polynomial function of degree *m* for each component of the fundamental current as well as for each current harmonic. All the derived components have been expressed as a function of V_1 by interpolation of the measured *rms* currents. In detail:

$$I_{P1} = a_{P1} + b_{P1}V_1 + \sum_{m=2}^{np1} c_{P,m}{V_1}^m \tag{85}$$

$$I_{Q1} = a_{Q1} + b_{Q1}V_1 + \sum_{m=2}^{nq1} c_{Q,m}{V_1}^m \tag{86}$$

$$I_k = a_k + \sum_{m=2}^{nqk} c_{k,m}{V_1}^m \tag{87}$$

where n_{p1}, $n_{q1,}$ and n_{qk} are numbers representing the maximum exponents of the polynomial expressions adopted for modeling, respectively, the active current, the fundamental nonactive current, and the *k*-th nonactive current.

The components of the proposed equivalent circuit model are obtained directly by the coefficient of the polynomial functions that, in turn, are obtained by the current measurements performed at the lamp terminals for different values of the voltage supply.

In the nonlinear model, both the active and nonactive fundamental currents are represented by means of three-term contributions:

$$i_{P1}(t) = i_{aP1}(t) + i_{bP1}(t) + i_{cP1}(t) \tag{88}$$

$$i_{Q1}(t) = i_{aQ1}(t) + i_{bQ1}(t) + i_{cQ1}(t) \tag{89}$$

In both equations, the magnitude of the first term is constant to emulate the constant coefficient in the related polynomial function, the second one represents the linear dependence on the voltage V_1, and the last one refers to the other terms of the interpolation function.

For the active current, the sum of the three contributions must present a phase offset equal to zero regardless of their amplitudes since i_{P1} is in phase with the network voltage. Considering that i_{aP1} has a constant amplitude and the amplitude of the other two currents changes as V_1 changes, the phase offset of each current must be equal to zero. At the most, some contributions could be in antiphase (i.e. phase offset equal to π) with i_{P1}, but the sum of all the contributions must present phase offset equal to zero. The contributions in phase with the active fundamental currents are associated with the positive coefficients in the related polynomial function, while the negative coefficients involve antiphase currents. In other words, a negative coefficient emulates an amplitude reduction that involves an antiphase current. Similar considerations are valid for the other polynomial functions related to the nonactive currents.

For the three current terms in (89), the phase offset has to be equal to π/2 (or -π/2), which is the phase offset of the nonactive fundamental current. Such an assumption is necessary to ensure that the phase offset of the sum of the three currents does not change when their amplitude changes.

Finally, the *k*-th current harmonic is represented as the sum of two different contributions:

$$i_{Qk}(t) = i_{ak}(t) + i_{ck}(t) \tag{90}$$

The first term emulates the constant value of the related polynomial function while the second one represents the dependence on the voltage V_1. Once again, the phase offset of these currents should be equal to φ_k although, at most, one could be in antiphase.

For the active current (see Figure 3:21), the constant and linear terms of the polynomial function are emulated by means of an independent current generator and a resistor o VCCS respectively. It is worth noting that the value of the magnitude of the independent current generator and the choice of the Resistor or the VCCS in the model circuit are both evaluated by using the (58) and (70) (See section 3.2).

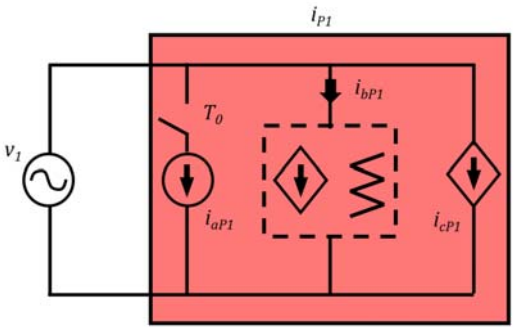


Figure 3:21 Equivalent circuit for the active current. Only one element in the dashed box has to be used (it depends on the sign of b_{P1}).

The remaining terms in (91) are emulated in Figure 3:21 by means of a VCCS as represented in (92):

$$i_{cP1}(t) = \left\{ \sum_{m=2}^{np1} c_{P,m}[pV_1]^m \right\} v_1(t) = \left\{ \sqrt{2} \sum_{m=2}^{np1} c_{P,m}[pV_1]^m \right\} \sin(\omega t) \tag{91}$$

Where *p* is a parameter used to account for the variation of the network voltage amplitude.

Figure 3:22 depicts the components related to the nonactive fundamental current. The constant term in the polynomial function related to the amplitude of the nonactive fundamental current is emulated by means of an independent current generator to keep a constant amplitude. While the linear term in the polynomial function is emulated by means of an inductor or capacitor depending on the value of the coefficient b_{Q1}. Also in this case, the value of the independent current generator and the inductor or capacitor can be derived by using the relations (58)-(65)-(69) (See section 3.2).

The second and higher-order terms in the polynomial function in (89) are emulated by means of a current-controlled current source (CCCS) i_{cQ1}. It is worth noting that a CCCS enables to obtain current with variable amplitude while their phase offset is equal to the control current when the gain of the CCCS is a positive number, otherwise the current is in antiphase with the control one. Therefore, such a control current has to present a phase offset equal to i_{Q1} to obtain currents in phase or antiphase with that current. The independent current generator, i_{aQ1}, is chosen as control current because a waveform in phase with i_{Q1} is easily obtained by dividing the current of the generator:

$$i_{cQ1}(t) = \left\{ \frac{1}{a_{q1}} \sum_{m=2}^{nq1} c_{P,m}[pV_1]^m \right\} i_{aQ1}(t) = \left\{ \sqrt{2} \sum_{m=2}^{np1} c_{Q,m}[pV_1]^m \right\} \sin(\omega t + \varphi q) \tag{92}$$

The previous considerations and rules are also adopted for modeling the nonactive currents referred to the harmonics. The circuit model is depicted in Figure 3:23, where the k-th current harmonic, i_{qk}, is represented as the sum of two different contributions as reported in (90).

The first current in (92) is referred to the constant value of the related polynomial function while the second one represents the dependence on the voltage V_1. It is worth mentioning that such a current also includes the linear term of the polynomial function (differently from the previous cases). On the other hand, the constant term of the polynomial function is modeled by means of an independent current generator (See section 3.2 and Equation (58)).

A CCCS is adopted to emulate the other terms in the polynomial function. The angular frequency of the control current waveform has to be $k\omega$, with a phase offset equal to φ_k. Therefore, i_{ck} is the control current that may be adopted (similarly to the previous cases):

$$i_{ck}(t) = \left\{ \frac{1}{a_k} \sum_{m=1}^{nqk} c_{P,m} [pV_N]^m \right\} i_{ak}(t) = \left\{ \sqrt{2} \sum_{m=1}^{nqk} c_{k,m} [pV_N]^m \right\} \sin(\omega t + \varphi_K) \tag{93}$$

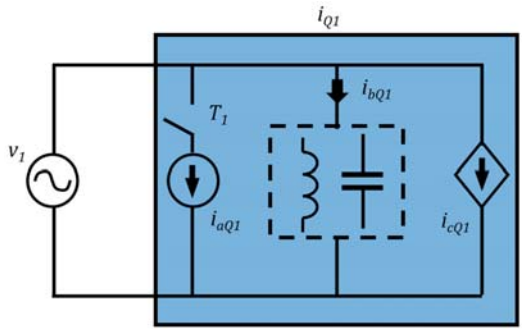


Figure 3:22 Equivalent circuit for the fundamental nonactive current. Only one element in the dashed box has to be used (it depends on the sign of b_{Q1}).

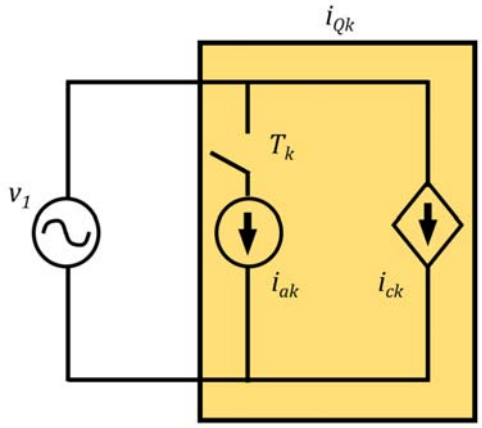


Figure 3:23 Equivalent circuit of the k-th nonactive current harmonic.

3.4.2 Nonlinear model validation

In the following, the comparison between the measured and simulated current waveforms of different LED light bulbs have been carried out. The results have highlighted the high fidelity level of the proposed nonlinear model in emulating the current drawn by the LED light bulbs under variable voltage on the mains. Furthermore, the PSpice netlist has been partially modified according to the aforementioned model.

A. Measurements

The quantities necessary for obtaining the components of the circuit model according to the rules and equations discussed before are obtained by using the coefficients of the polynomial functions that, in turn, have been obtained by the simple procedure described before.

The circuit model described in the previous section presents several components that are obtained through the acquisition of the active and nonactive power referred to the fundamental frequency and the amplitude and phase offset of 49 current harmonics, i.e. up to 2.5 kHz. The active and nonactive power and the current harmonics have been detected at the eight aforementioned voltage values from the measurements on the mains by a power analyzer. The experimental setup is the same as Figure 3:2, where the lamp in the box represents any commercial LED light bulbs. The experimental measurements and the model validation have been performed using several LED light bulbs by different manufacturers in the range 6W-12W. Each lamp type has been experienced by a five sample stock in order to verify the spread of the performances. The phase offset of each simulated current harmonic has been assumed equal to the one measured when the network voltage has been set at its

nominal value. In other words, the equivalent circuit is able to simulate only the variation of the harmonic amplitude, while the variation of both amplitude and phase offset of the fundamental current are modeled. Figure 3:24 summarizes the main steps to be executed in order to obtain the circuit model starting from the measurements performed at the terminals of LED light bulbs with the related data flow (represented by the dashed arrows). More specifically, the first box refers to the measurement procedure and the red storage silos represent the saved data. A limited number of measurements (six in the case study) is necessary to obtain the coefficients, thus this step requires low time. The second box refers to a simple modification of the data. The third box highlights the use of the data to evaluate the polynomial coefficients, which are saved in the blue silos. Finally, the last box reports the implementation (in a PSpice netlist) of the circuit model by using both previous data. Figure 3:24 highlights that the parameters extraction is performed off-line. Moreover, the computational effort to obtain the coefficients is very low because only the previous few values are necessary for each quantity to be modeled (e.g. the amplitude of the *k*-th current harmonic). According to these facts, the computational time for the extraction of the model parameters is very low.

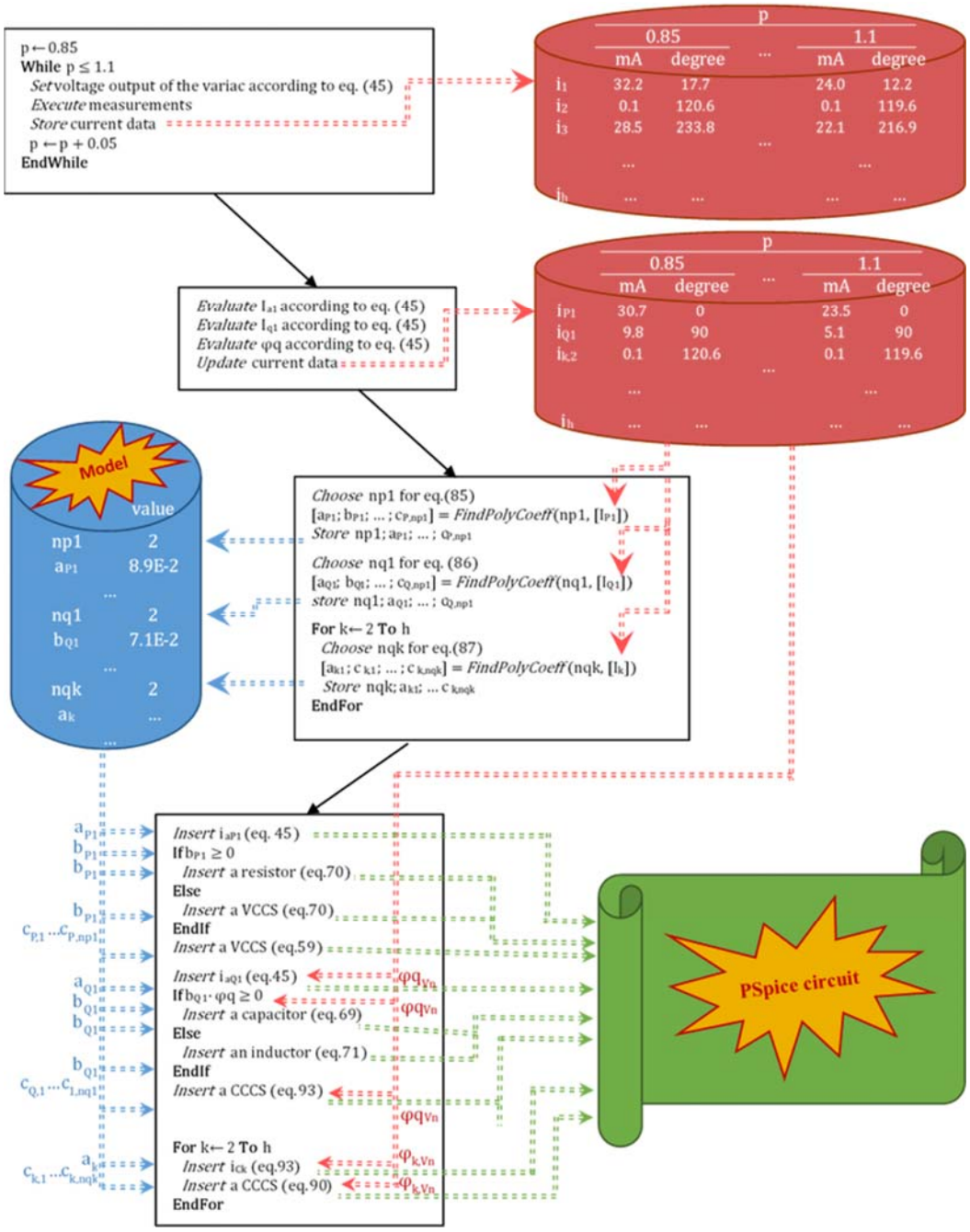


Figure 3:24 Main steps to obtain the circuit model for any LED light bulb using only measurements at its terminal (i.e. black-box model).

Similar considerations hold true for the degree of the polynomial function. Indeed, for a given lamp, there is not an optimal value for all the current harmonics (i.e. the optimal value

of *np1*, *nq1,* and *nqk* is not the same). On the other hand, the value of each exponent in (85)-(87) depends on two conflicting targets: the improvement of the model accuracy of the related current asks for higher exponent values, while the reduction of the computational burden of the circuit model asks for lower exponent values. A second-order polynomial function has been always adopted (i.e. *np1*, *nq1* and *nqk* are set to 2 for each lamp) since the tests have revealed that it has been enough to obtain good results.

B. Simulation of the equivalent circuit

The data acquired from the instruments have been processed using an interface tool used to implement the circuit model and to create a PSpice netlist. As mentioned before, the circuit model integrates the polynomial functions of each current harmonic to emulate its amplitude variation according to the variability of the network voltage, but the model does not account for the phase offset variation. Therefore, for each harmonic, a fixed phase offset, equal to the one measured at V_1, has been used in the netlist. On the other hand, the interpolation of both the active and nonactive fundamental current amplitude enables to account in the model for the phase offset variation of the fundamental frequency current. Finally, the netlist contains the parameter *p* to emulate the network voltage variation. Therefore, only one netlist file is obtained for each LED light bulb.

To evaluate the effectiveness of the proposed model, the amplitude of the fundamental (k=1) and harmonic (k=2…h) currents obtained by simulations have been compared with the measured ones. The comparison has been performed at eight voltage values (V_1 =0.85V_1 and so on) for each lamp under test and the percentage error between the current simulated, $I_{ksim}(V_1)$, and measured, $I_{kmeas}(V_1)$, has been computed:

$$E_k(V_1) = \left|\frac{I_{k,sim}(V_1) - I_{k,meas}(V_1)}{I_{k,meas}(V_1)}\right| \% \tag{94}$$

The maximum and minimum percentage error obtained at the various frequencies (fundamental and harmonics) is depicted in Figure 3:25(a).

It is worth noting that a considerable error occurs for many even harmonics and some odd harmonics at high frequency. However, this does not affect the effectiveness of the model since the amplitude of these harmonics is very small in comparison with the fundamental. To support such a consideration each error has been weighted by the normalized harmonic to evaluate the factual effect of each error in the suitability of the proposed model:

$$EN_k(V_1) = \left|\frac{I_{k,sim}(V_1) - I_{k,meas}(V_1)}{I_{k,meas}(V_1)}\right| \left|\frac{I_{k,meas}(V_1)}{I_{1,meas}(V_1)}\right| = \left|\frac{I_{k,sim}(V_1) - I_{k,meas}(V_1)}{I_{1,meas}(V_1)}\right| \tag{95}$$

Figure 3:25(b) shows the range of normalized error, *EN*, once again considering all the lamps. Figure 3:25(b) weights the error by the normalized amplitude of each harmonic to

highlight the low overall impact of the error on the current prediction ability of the model. The low impact of errors on the ability of the proposed circuit model in emulating the true current waveform (when using a second-order polynomial interpolation) has been also confirmed by visual inspection of the measured and simulated currents. In other words, a small estimation error occurs for the fundamental current and the relevant harmonics while a higher error occurs for the smallest ones (i.e. many even harmonics and some odd harmonics with k>22). Moreover, as it will be highlighted in the following, whether all the even harmonics and the odd harmonics at higher frequency (k>19) are neglected, the error on the power factor is less than 1% also when the lamp presents a low power factor. It is worth noting that, the voltage THD has been monitored during the acquisition of the currents to be modeled. The values of the voltage THD have been measured in the range 2.2%-4.7% during the measurements, which is typical THD meeting the limit of IEEE-Std-519. Therefore, the previous error has been computed comparing the measured currents (obtained with a distorted voltage within the limit) with the simulated ones obtained considering a pure sinusoidal voltage supply. In other words, a good accuracy of the model has been experienced when the voltage THD satisfies the limit.

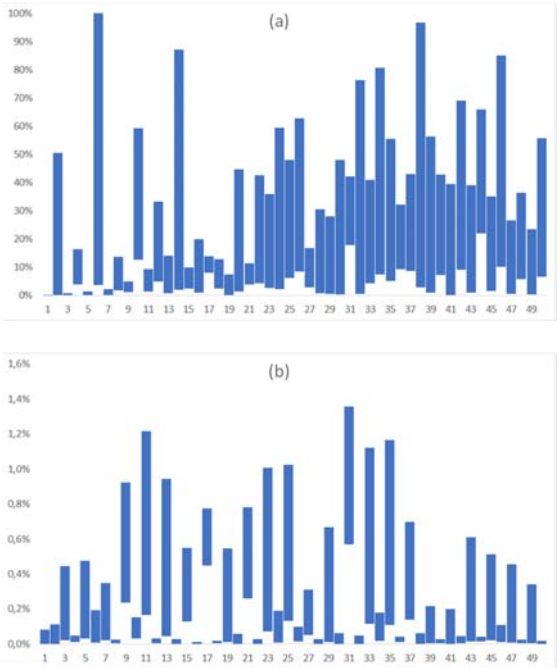
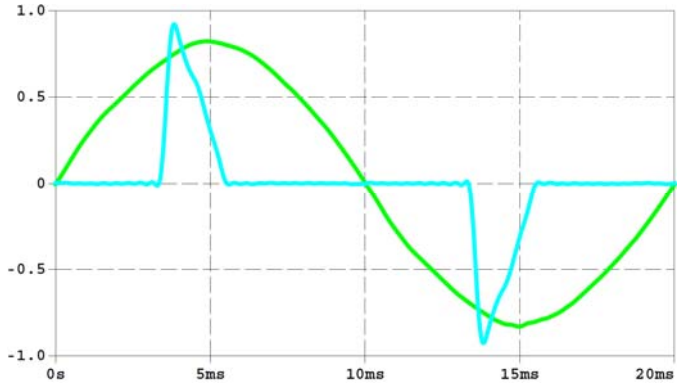
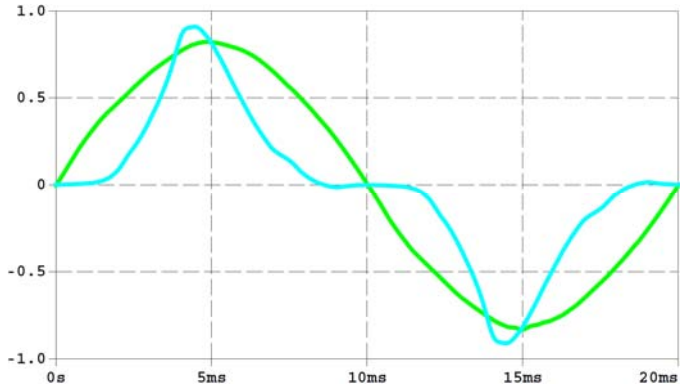


Figure 3:25 Maximum and minimum percentage error: (a) before normalization - (b) after normalization.



(a)



(b)

Figure 3:26 Measured voltage (green) on the mains at V_1 =230V and currents (light blue) drawn by the LED 1 (a) and LED 2 (b). The waveforms are in per unit: 1p.u.= 400V for the voltage, 1p.u.=180 mA for LED1 current, 1p.u.=120 mA for LED2 current.

The main data and results for the LED light bulbs, named LED1, with greater error in terms of relation (32) are given in the following. LED 1 is a lamp with a low power factor (PF): 0.55. The data and results related to a high PF LED light bulbs, LED 2, have been also reported.

Figure 3:26 shows the waveforms measured for, respectively, the voltage on the mains and for the measured current drawn by the two LED light bulbs under the nominal condition in case of a voltage THD=2.6%. Figure 3:27 reports the amplitude of the fundamental current and the harmonics until the 50th for both lamps. More specifically, the amplitude of each current measured at the six voltage values adopted for obtaining the interpolation functions are reported. Moreover, the related amplitude obtained by using these interpolation functions are also reported to reveal the estimation error due to the interpolation. A magnification of higher-order harmonics has been also reported in order to better observe the measurements and the estimated values. Finally, Table 3:1 reports the coefficients of the poly-

nomial functions related to the active and nonactive fundamental currents and for the odd harmonics until the 45th. Figure 3:28 shows the comparison between the measured and simulated currents when two generic voltage values, different from the ones used to identify the model parameters, are used. The results confirm the effectiveness and robustness of the proposed model in emulating the lamp current drawn in case of variability of the network voltage for the two different LED light bulbs. Figure 3:28(a) and Figure 3:28 (b) report the comparison for LED1. In both cases, the current waveforms have been obtained considering until the 50th harmonic, thus obtaining a power factor (PF) equal to 0.5498 in good agreement with the one provided by the manufacturer. They are indicated as “original” waveforms in the figures. In the figure are also reported two further cases where a reduced number of harmonics are considered. More specifically, the dotted waveforms are obtained when the fundamental current and the 3rd, 5^{th,} and 7th harmonic are considered for the measured and simulated waveforms, thus obtaining a PF equal to 0.5864 that implies an estimation error less than 10%. Similarly, the dashed waveforms are obtained considering other current harmonics (odd harmonics until the 19th) so that the error on the PF estimation is less than 1% (estimated PF equal to 0.5547).

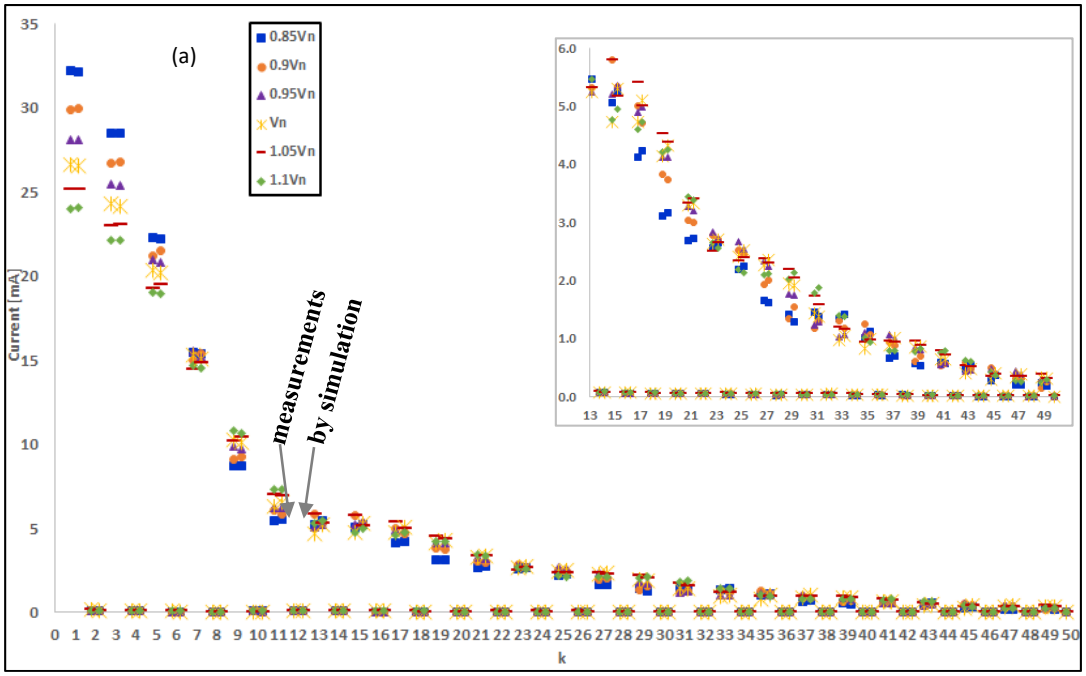
Table 3:1 Coefficients of the polynomial functions for LED light bulbs with low (LED1) and high PF (LED2)

coeff.	LED 1	LED 2	coeff.	LED 1	LED 2	coeff.	LED 1	LED 2
a_{P1}	8.93E-02	2.04E-01	$a_{13,0}$	1.99E-02	2.66E-03	a_{27}	-2.68E-02	5.22E-04
b_{P1}	-4.36E-04	-1.18E-03	$c_{13,1}$	-1.31E-04	-1.39E-05	$c_{27,1}$	2.52E-04	-3.08E-06
$c_{P,2}$	6.94E-07	2.10E-06	$c_{13,2}$	2.93E-07	2.30E-08	$c_{27,2}$	-5.42E-07	5.52E-09
a_{Q1}	7.11E-02	1.78E-02	a_{15}	-8.49E-03	9.58E-04	a_{29}	-9.60E-03	3.31E-04
b_{Q1}	-4.95E-04	-1.01E-04	$c_{15,1}$	1.28E-04	-4.97E-06	a_{31}	1.76E-02	4.18E-04
$c_{Q,2}$	9.25E-07	1.81E-07	$c_{15,2}$	-2.97E-07	8.22E-09	$c_{31,1}$	-1.54E-04	-2.49E-06
a_3	8.20E-02	1.12E-01	a_{17}	-3.24E-02	1.60E-03	$c_{31,2}$	3.63E-07	4.54E-09
$c_{3,1}$	-4.00E-04	-6.71E-04	$c_{17,1}$	3.26E-04	-9.75E-06	a_{33}	2.25E-02	3.39E-04
$c_{3,2}$	6.47E-07	1.22E-06	$c_{17,2}$	-7.08E-07	1.80E-08	$c_{33,1}$	-1.92E-04	-1.84E-06
a_5	3.99E-02	2.57E-02	a_{19}	-3.25E-02	1.18E-03	$c_{33,2}$	4.27E-07	3.12E-09
$c_{5,1}$	-1.16E-04	-1.35E-04	$c_{19,1}$	3.09E-04	-6.43E-06	a_{35}	2.60E-03	2.08E-04
$c_{5,2}$	1.31E-07	2.27E-07	$c_{19,2}$	-6.48E-07	1.10E-08	$c_{35,1}$	-1.11E-05	-9.12E-07
a_7	1.51E-03	1.33E-02	a_{21}	-1.29E-02	7.56E-04	$c_{35,2}$	1.80E-08	1.29E-09
$c_{7,1}$	1.23E-04	-7.86E-05	$c_{21,1}$	1.33E-04	-4.29E-06	a_{37}	-1.59E-02	3.06E-04
$c_{7,2}$	-2.78E-07	1.43E-07	$c_{21,2}$	-2.70E-07	7.53E-09	$c_{37,1}$	1.49E-04	-1.80E-06
a_9	-1.24E-02	3.08E-03	a_{23}	-4.27E-03	1.26E-03	$c_{37,2}$	-3.30E-07	3.22E-09
$c_{9,1}$	1.64E-04	-1.45E-05	$c_{23,1}$	6.40E-05	-7.31E-06	a_{39}	-1.10E-02	3.40E-04
$c_{9,2}$	-2.89E-07	2.18E-08	$c_{23,2}$	-1.46E-07	1.31E-08	$c_{39,1}$	1.01E-04	-2.15E-06
a_{11}	3.62E-03	6.87E-03	a_{25}	-1.91E-02	7.08E-04	$c_{39,2}$	-2.13E-07	4.06E-09
$c_{11,1}$	-6.00E-06	-4.41E-05	$c_{25,1}$	1.95E-04	-4.15E-06	a_{41}	3.45E-03	8.82E-05
$c_{11,2}$	8.15E-08	8.41E-08	$c_{25,2}$	-4.39E-07	7.46E-09	$c_{41,1}$	-2.94E-05	-2.88E-07

Similarly, Figure 3:28(c) and Figure 3:28(d) report the comparison for LED2. In such a case, it has been sufficient considering only the 3rd harmonic to obtain an estimation error of less than 10%. Moreover, to reach an error less than 1% on the estimation of PF the 3rd and 5th harmonics are enough. Such a strongly reduced number of harmonics to be considered is due to the higher PF with respect to LED1.

Figure 3:29 shows a screenshot of the PSpice netlist adopted to perform the simulation with the references to the equations provided in the model. The circuit model is parametric and for each LED light bulbs the coefficients are obtained by interpolation (Table 3:1), while the phase offset of each current harmonics measured at nominal voltage is adopted. Figure 3:30 reports a subpart of both lamps netlists which is included in the aforesaid main parametric circuit for obtaining the simulated waveforms. Therefore, the users can treat the lamp as a black-box where its behavior is emulated by the PSpice netlist which may be also modeled within a PSpice subcircuit (.SUBCKT). The subcircuits of different LED light bulbs can be used together with resistors and inductors that models the cable to obtain the current drawn from the overall lighting system (Figure 3:31). Such an approach is practicable because the PSpice subcircuit and, consequently, its underlying model is valid for typical THD voltage on the mains. This is due to the fact that the subcircuit output (i.e. the current drawn by the lamp) is not directly dependent on the other components, but it only depends on its input (the voltage at its terminals) and the other components affect the voltage without directly influencing its behavior.

According to the IEEE-Std-519, at the point of common coupling between a network operator and a user, the voltage distortion, in terms of THD, has to be limited to 8%. The value of the THD has been measured in the range of 2.2%-4.7% during the voltage and current measurements. As highlighted by the results (Figure 3:25, Figure 3:27, and Figure 3:28), the current waveform obtained by simulation neglecting the voltage distortion well approximates the current waveforms measured when the voltage on the mains has been distorted. Therefore, it is apparent that the model is enough robust at the use of a pure sinusoidal waveform for emulating the voltage supply at the simulation stage. In other words, although the model may fail when the voltage distortion exceeds the THD limits, it is plausible that it performs well until the limits are respected



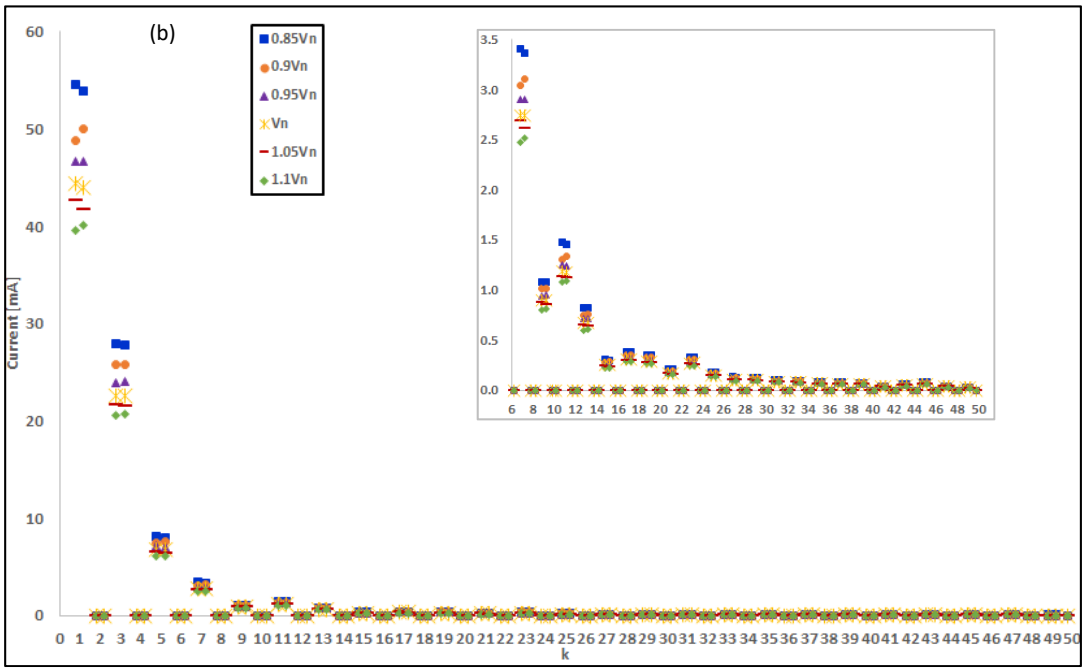
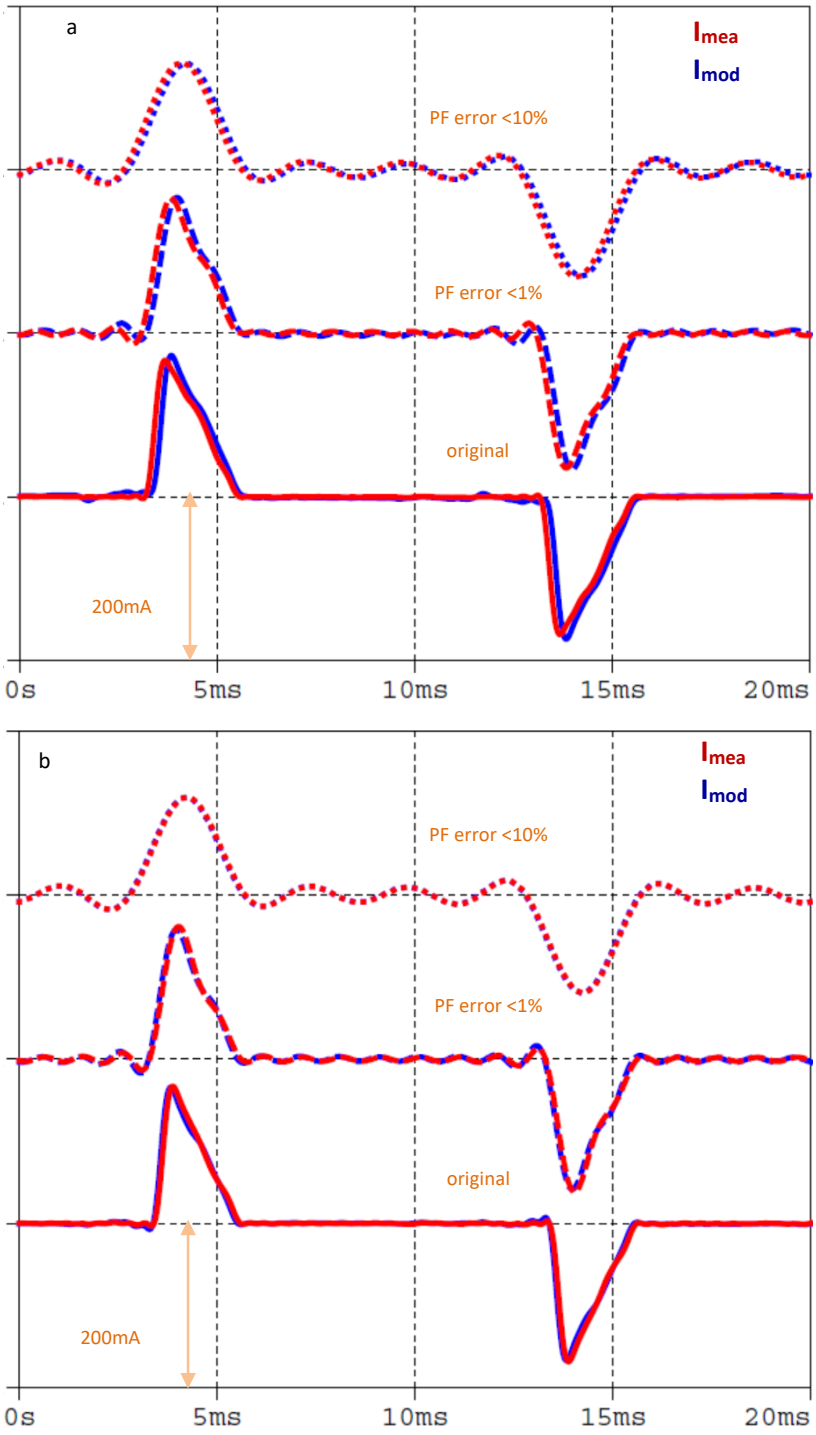


Figure 3:27 Fundamental and harmonics currents obtained by measurements (left) and simulation (right) at six voltage values for LED1 (a) and LED2(b). The sub-figure at the left corner presents a magnification to better observe higher-order harmonics amplitude.


a
Imea
Imod
PF error <10%
PF error <1%
original
200mA
0s
5ms
10ms
15ms
20ms
b
Imea
Imod
PF error <10%
PF error <1%
original
200mA
0s
5ms
10ms
15ms
20ms

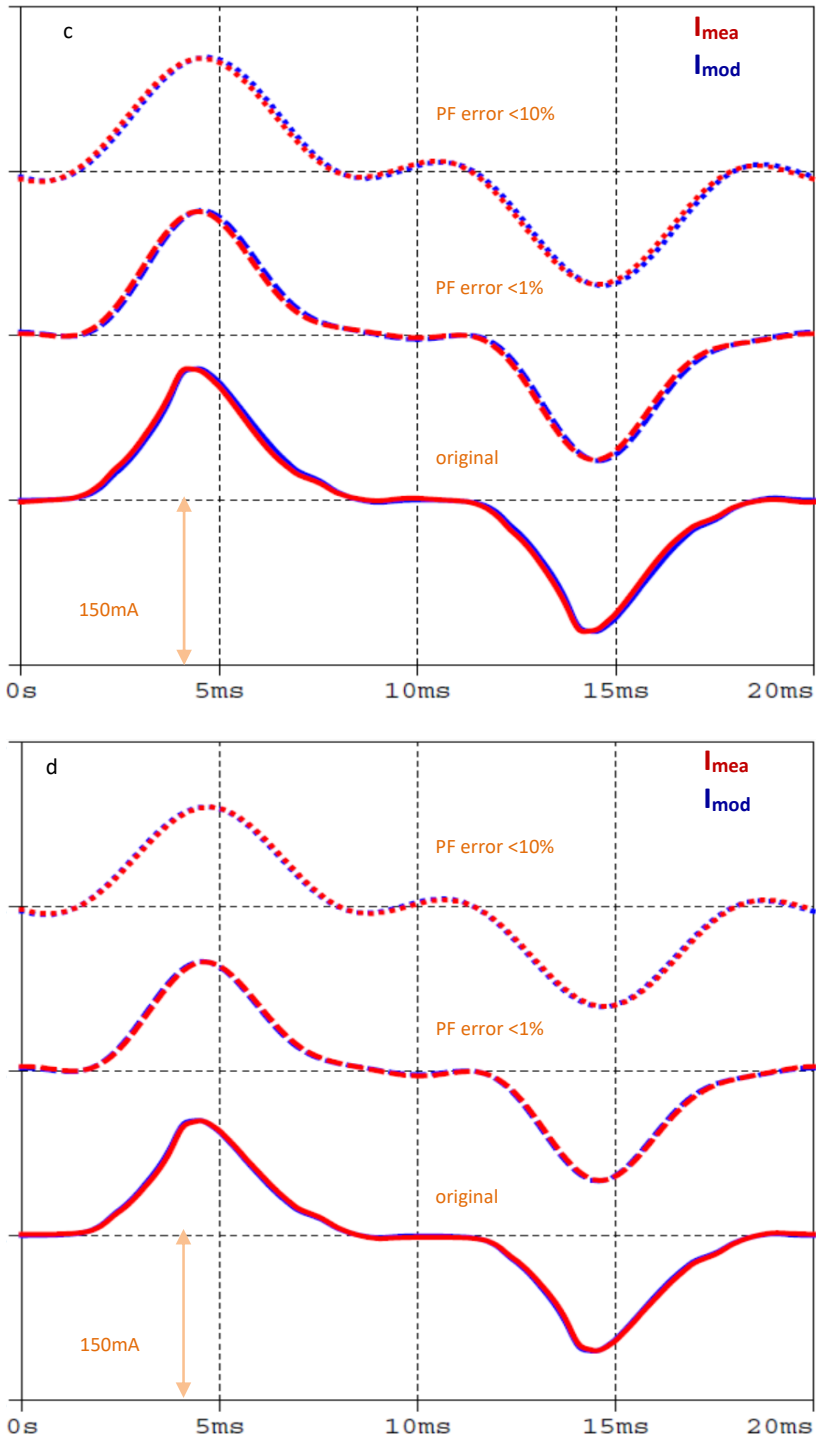


Figure 3:28 Total current drawn by the lamps. I_{mea} is the measured current (red trace) while I_{mod} is the simulated current (blue trace):
(a) LED1 at V_1 =212V - (b) LED 1 at V_1 =237V - (c) LED2 at V_1 =212V - (d) LED2 at V_1 =237V.

since the currents waveforms obtained by simulation considering a sinusoidal voltage on the mains well approximate the current measured in presence of a distorted voltage on the mains with a THD less than 8%.

It is worth noting that the normal situation is the one in which the THD limit is met since usually any countermeasures have been realized at the load/generation points along the distribution network to avoid exceeding the limit, for example by adopting filters in case of distorted load or generation units. In such a case, few lamps do not negatively affect the voltage THD due to the low current drawn. Therefore, the proposed model is suitable for estimating the current waveform of the whole (small) lighting system (Figure 1:9(a)). In the case of a large number of LED light bulbs, the model may fail at foreseeing the large current drawn from the whole light system when the current distortion level is so high that it lets the voltage THD at exceeding the limit (up case of Figure 1:9(b)). On the other hand, when the whole current is large but few distorted so that the voltage THD is left under the limit (down the case of Figure 1:9(b)), then using the model of each lamp is again sufficient to properly estimating the whole current. In this regard, the optimal

Figure 3:29. Parametric PSpice netlist of the circuit model of LED light bulbs.

```
.param np1 2
.param a0 89.280991m
.param a1 -0.435687m
.param a2 6.939111E-04m
.param phiq 90
.param nq1 2
.param b0 71.124783m
.param b1 -0.495145m
.param b2 9.254829E-04m
.param phi2 114.885
.param nq2 2
.param g2_0 -0.391683m
.param g2_1 0.004722m
.param g2_2 -1.059032E-05m
.param phi3 -138.665
.param nq3 2
.param g3_0 81.972203m
.param g3_1 -0.400274m
.param g3_2 0.000647m
.param phi4 -39.950
.param nq4 2
.param g4_0 -0.400904m
.param g4_1 0.004204m
.param g4_2 -8.739641E-06m
.param phi5 70.325
.param nq5 2
.param g5_0 39.902434m
.param g5_1 -0.116158m
.param g5_2 1.314473E-04m
*...
.param phi49 103.154
.param nq49 2
.param g49_0 -4.501035m
.param g49_1 0.041289m
.param g49_2 -8.836665E-05m
.param phi50 -82.918473
.param nq50 2
.param g50_0 0.058851m
.param g50_1 -4.289444E-04m
.param g50_2 1.005805E-06m
```

(a)

```
.param np1 2
.param a0 204.075076m
.param a1 -1.179307m
.param a2 2.096911E-03m
.param phiq 90
.param nq1 2
.param b0 17.817544m
.param b1 -0.101440m
.param b2 1.806128E-04m
.param phi2 -124.208
.param nq2 2
.param g2_0 1.260805E-06m
.param g2_1 -2.851741E-09m
.param g2_2 -2.878083E-13m
.param phi3 -161.590
.param nq3 2
.param g3_0 112.459249m
.param g3_1 -0.671219m
.param g3_2 0.001219m
.param phi4 -138.710
.param nq4 2
.param g4_0 6.504980E-07m
.param g4_1 -3.393923E-09m
.param g4_2 5.619167E-12m
.param phi5 51.967
.param nq5 2
.param g5_0 25.709018m
.param g5_1 -0.134761m
.param g5_2 2.273295E-04m
*
.param phi49 -176.290
.param nq49 2
.param g49_0 0.107504m
.param g49_1 -6.211024E-04m
.param g49_2 1.110824E-06m
.param phi50 89.125
.param nq50 2
.param g50_0 2.373896E-07m
.param g50_1 -1.452765E-09m
.param g50_2 2.6970215E-12m
```

(b)

Figure 3:30. Coefficients (Table 3:1) and phase offset reported in the parametric PSpice netlist of LED1(a) and LED2 (b).

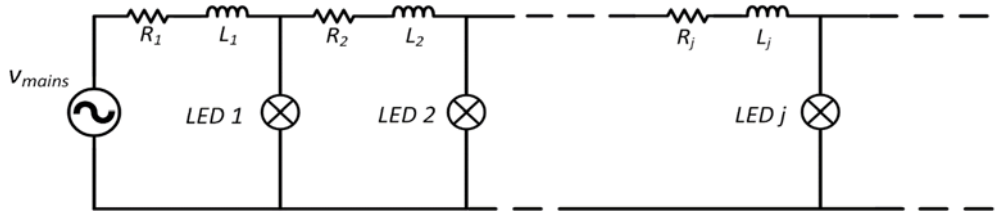


Figure 3:31. Circuit to simulate the current of the overall lighting system.

design of the large lighting system aims at reaching such a low-distorted overall current. Therefore, the proposed method is useful at the design stage because when a combination of LED light bulbs involves a:

- high-distorted current that involves voltage THD over the limit, a high-distorted current that does not well estimates the actual one is obtained by using the proposed model; but being the target of the optimization the combination with the lowest distorted current, such a combination leading a high-distorted current is however discarded regardless the accuracy of the current.

- low-distorted current that does not involve voltage THD over the limit, a low-distorted current that well estimates the actual one is obtained by using the proposed model; and the estimation accuracy is necessary to effectively find the combination with the lowest distorted current.

It is worth highlighting that, in the latter case, the model provides an accurate estimation of each lamp current and such a current may be high-distorted regardless the overall current is low-distorted. Indeed, all the currents may be high-distorted.

Chapter 4 The superiority of the unintentional LED for temperature detection.

4.1 Introduction

Nowadays, power electronics is widespread into a huge number of daily applications that improve services for the collective [94]. Furthermore, power electronic has a key role in renewable energy systems [95-96], lighting [97], electric mobility [98-99], and other systems that are enabling sustainable development [100].

A crucial aspect is the reliability and lifetime prediction of the whole power conversion system. The warrant of the highest robustness level while minimizing the product and maintenance cost is extremely mandatory. For example, the devices used in avionic and automotive applications must have a fault rate close to zero that imposes stringent requirements during the system design. In the same way, the wind farms must be guaranteed the normal operations without interruption, but it is extremely difficult due to the expensive access to the farm for easier maintenance. In this context, many approaches to forecast the lifetime of power electronic systems and the single power device have been intensively studied.

With the aim to guarantee a high level of reliability, it is important to comply with several standards [101-103], and furthermore, different strategies are usually performed such as the use of the fault-tolerant topologies with redundant components [104-105], and the advanced reliable design of power electronic devices using innovative materials [106-107].

Unfortunately, the enhanced system's robustness does not prevent failure and, indeed, it is never completely foreseeable. Therefore, a maintenance operation before a failure is necessary. Considering the costs of maintenance operations, lifetime prediction combined with condition monitoring approaches [108-109] are very useful tools to choose when a maintenance operation has to be carried out.

Several studies have shown that capacitors are fragile with a failure of 30% and the PCB and connectors failure are around 36% [110]. The remaining part is related to the semi-

conductor and soldering failures in device modules that consist of the most important area of concern for converter system failures. In this context, countless condition monitoring (CM) methods for the evaluation of the semiconductor state of health have been widely explored in the literature.

It is worth underlining that many papers have already studied and classified the CM methods based on the physical or electrical proprieties, where each method has a specific degree of intrusiveness with respect to the measurement to perform. It is worth noting that the intrusiveness level of each CM method has not been defined uniquely yet.

Hence, the definition of a unique figure of merit (FOM) able to represent the level of intrusiveness of the various CM methods is extremely interesting. In this perspective, in section 4.3 different criteria to establish the level of intrusiveness have been defined. They are related to the impact of a CM method in terms of the modification in the device, change in the converter operations, and system modification.

Then, three FOMs have been accordingly considered and assigned to all the CM methods by means of a mark based rule. Finally, a unique single-value FOM has been obtained from the product of the three FOMs. An application-based FOM that accounts for the importance of the different intrusiveness criteria in a given application has been also proposed. The use of a single value to compare the different CM methods is the main strength of these overall FOMs but they do not provide a fixed value due to the subjective of the marks. On the other hand, the rank of the CM methods according to an intrusiveness criterion is almost unbiased. Therefore, a strategy to compare the CM methods according to the rank instead of the mark is proposed by borrowing some reasoning from the Pareto optimality. Such an approach has revealed that the CM methods adopting, respectively, Integrated photodiode, IR Camera, Acoustic, and two thermo-sensitive electrical parameters (turn on-off delay time and peak gate current) are the best ones in terms of intrusiveness, and they are equivalent each other from the Pareto optimality point of view. Finally, the Integrated photodiode and the IR Camera CM methods are the less intrusive according to the overall FOM.

Among the various CM methods, the exploitation of the light emission phenomenon from the body diode of a SiC device is gaining more interest in the last decade. The electroluminescence phenomenon refers to the photoemission from a SiC material and it is related to its intrinsic body diode that operates in the third quadrant. The light brightness in the SiC intrinsic body diode depends on the junction temperature Tj and on the forward current that flows into the diode. The light intensity decrease at high Tj being equal to the current injected. Thus, the electroluminescence phenomenon can be a suitable indicator of the temperature of the SiC MOSFET chip during a general power converter application. Therefore, considering the results of the comparison among the CM methods performed in this chapter, which has highlighted that the use of the Integrated photodiode is one of the best choices, and considering the SiC MOSFET intrinsic diode as

an unintentional diode, in Chapter 5 has been proposed a new CM method adopting the Integrated photodiode in a SiC MOSFET module.

4.2 Overview of condition monitoring methods of power devices

Nowadays, various CM methods are gaining more interest since the various maintenance strategies allow to increase the lifetime of the power device, and hence, the reliability of the overall system can be enhanced. In many applications, it is becoming crucial to monitor the state of the health (SOH) of the power devices to prevent a failure, that is the possibility for the operators to obtain a lifetime estimation, thus properly scheduling any maintenance operations.

Table 4:1 Parameters dependence of different CM methods

Method	**Parameter Dependence**
Acoustic	Acoustic waves
OPTICAL - Fiber optic	Light wavelength
OPTICAL - Photodiode sensor	Light intensity
OPTICAL - IR camera	Light wavelength
Physical	Resistance
TTCs – NTC	Resistance
TTCs – Diode	Voltage
TSEP - On-state voltage, low current	V_{ce}, V_{ds}
TSEP - On-state voltage, high current	Device current, V_{ce}, V_{ds}
TSEP - Saturation current	V_{ce} - V_{ds}
TSEP - Gate threshold voltage	V_{ge} - V_{gs}
TSEP - Gate turn OFF voltage	V_{ge}-V_{ce}, V_{gs}-V_{ds} , Gate resistance
TSEP - Turn on-off delay time	Device current, V_{ce}-V_{ds}
TSEP – Voltage-Current change rate *di/dt*	Device current, V_{ce}-V_{ds}
TSEP - Peak gate current	V_{ge} - V_{gs}

The thermal stresses like the increasing of the means temperature and abrupt temperature fluctuations are the main failure mechanisms. Consequentially, the temperature is an index of the power device SOH. Although the purpose of a continuous thermal control improves the reliability of the power applications, the level of intrusiveness should be also taken into account. Other CM methods focus on other quantities. Table 4:1 summarizes the physical or electrical quantities measured for each CM method, and, in the following subsections, a brief overview has been presented. It is worth noting that, among the various CM methods in the literature, the acoustic one is used to detect the state of the aging of the power device without any estimation of the working temperature, while all the other strategies have been focused on the estimation of the junction temperature (JT). More specifically, some CM methods perform such estimation by directly measuring the temperature, other methods provide an indirect estimation by mapping electrical quantities in a temperature value.

4.2.1 Acoustic methods

Acoustic emission has been widely investigated in literature as a CM quantity useful in different applications fields such as pumps, industrial electrical machines, and so on. Moreover, in the field of power electronics, acoustic monitoring has been extensively used to detect any defects or damage in transformers and capacitors [111-113]. Only in the last decade, a few works have been focused on the acoustic phenomenon such as a measurement method for monitoring the SOH of the power semiconductor devices [114-119].

The acoustic emission has been used with the aim to detect any physical damage in a power module packaging by using an acoustic microscope. Furthermore, from the experimental evidence, it has been proved that acoustic emissions are related to the switching operations of the power devices. In the case of fast switching operation (tens of nanoseconds), a certain amount of current is switched and it causes large *di/dt* that involves magnetic interaction within the module packaging. This means that the magnetic force could be the source of the acoustic emission, such as the mechanical breaking of the structure inside the component package. However, the physical phenomena causing the acoustic emission are not definitively understood.

Thereby, the device under test (DUT) is monitored contactless with an acoustic sensor that is usually placed in the proximity of the package. It intrinsically eliminates the issues related to contact directly with the voltage probes.

A correlation between the SOH of the power module and the analysis of its acoustic emission during the switching process has been analyzed [114-116]. It has been demonstrated that the acoustic peak in an aged device is smaller in comparison to a new one. However, in these works, only the acoustic emission of an IGBT connected into short-circuit has been investigated. While [117] presents an experimental setup to detect the

acoustic emission during the normal operation of the converter. In [118] an acoustic emission variation of a power module, when it is subjected to solder delamination, has been measured. Furthermore, the authors in [119] have proved that this method can be used for non-invasively state of the aging of a power semiconductor module due to power cycling during a real application. The aging process has been observed with a simple acoustic sensor during the switching operation by using a resistive-inductive load. The experimental results have also proved a strong correlation between the acoustic emission and the on-state voltage drop that in turn, is used to understand the bond wires degradation of the module. More specifically, the on-state voltage drops increases as the bond wires degrade.

As for disadvantages, the acoustic method needs an expensive and complex sensing circuit to decode correctly the acoustic emission. Furthermore, the system has to be shielded against EMI and superposition of noise contributions.

4.2.2 Optical Methods

Temperature variation, especially the sudden increase of the JT, plays a significant role in terms of power device reliability [120-121]. CM methods performing on-line JT monitoring raise great interest in terms of planning maintenance operations because the working conditions of a power converter are extremely unpredictable. In this perspective, the CM methods based on the optical properties of the semiconductor power devices have been studied in depth because they are useful for temperature estimation. These methods are usually based on an optical beam that is reflected or scattered back from the semiconductor lattice. There is an inherent dependence between temperature and the energy-related to the photoemission. More specifically, such energy is a function of the JT, hence, in turn, the energy variation can be used to estimate the temperature of the chip. There are various techniques for a thermal mapping that are based on the use of an IR sensor [122-125], IR microscope [126], the 2-D radiometry [127-128] the laser deflection technique [129-131]. While the optical fibers [132-134] and the IR camera [135-139] can be used both to obtain a thermal mapping or the JT value.

Among the aforementioned techniques, the latter two are the most widespread because of their high accuracy and fast response time. As an example, in [134] an optical fiber sensor has been used to measure the die temperature of an IGBT power module in order to estimate the thermal impedance. The module top lid has been removed because the optical system has to be placed close to the die, while it has not been necessary to remove the dielectric gel. This kind of technique allows exclusively a local temperature measurement. Printing the die and bond-wires to increase the emissivity of the chip is usually preferable, but causing a cost increment and severely limiting the on-line use of the method.

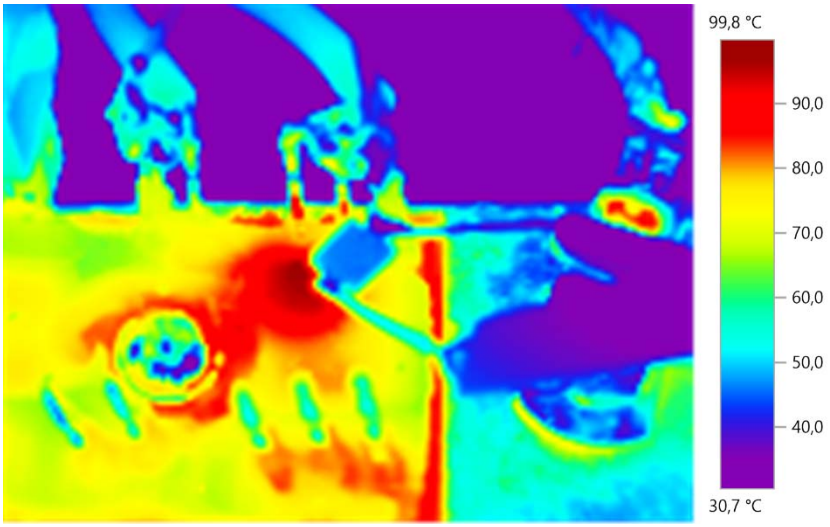


Figure 4:1 Thermal map of a SiC power module in case of current injection in the body diode.

The use of an IR camera [139] allows displaying the thermal map of the whole surface of the power module under test, as shown in Figure 4:1. As expected, the module temperature is not uniformly distributed: the temperature gradient between the center and the edge of the module can be greater than 40 °C. Usually, an IR camera is used to carry out a spatial thermal mapping on the device surface, but it is not able to provide an accurate measure of the device JT. It is worth remembering that some temperature measurement errors can be done using an IR camera due to the surface degradation of materials and the intrinsic low emissivity of aluminum. Even in this case, the IR temperature measurements are usually conducted by varnish the surface of the DUT with a particular solution that increases the thermal emissivity on the surface. These solutions based on optical quantities have some other drawbacks such as the high cost and the impracticality in high-voltage converters.

The SiC power MOSFETs are more and more diffusing devices since they concurrently enable high switching frequency, high voltage, and high-temperature operations. Therefore, the study of the electroluminescence proprieties of the SiC material for on-line CM has started to attract wide interest. For different reasons, the electroluminescence proprieties have already been studied back in 1907 [140], while, in the last three years, the inadvertent light emission phenomenon in the intrinsic body diode has been drawn attention. While the body diode is in forward conduction mode, the chip glows a visible blue light [141]. The light brightness of the SiC body diode strongly depends both on the injected current magnitude and on the JT. Hence, the measurement of light brightness can be used as a novel CM method for temperature detection, where only a few works have already focused on this topic [142-144]. The first proof of concept of the SiC light emission in a commercial power module has already proved the potentiality of this CM method [142]. An inexpensive passive sensing circuit, such as a silicon photodiode and a resistor, has been adopted and the photodiode output voltage has been correlated to

the light emission intensity as a function of the temperature. It is worth noting that the system is small enough that can be easily embedded in the package. Another approach considers a light circuit sensing by using two commercial photodiodes with an active signal conditioning circuit [143]. This approach has been adopted for JT estimation in a real application such as a PWM driven converter. The temperature-dependent changes in the spectrum of the light emission from the body diode of a SiC module have been also investigated [144]. The method has been proved by means of static characterization and dynamic double pulse measurement by using two Silicon Photomultipliers, that are able to detect the peak intensity and consequentially the dependence on temperature. Differently from the previous CM methods, the last one which is based on the light intensity of the SiC body diode enables high-voltage operations, and even more important, the JT can be estimated during on-line operations.

4.2.3 Physical Methods

The early works treating CM methods for the JT measurement have been done by directly contacting the chip surface with a thermo-sensitive material such as a point contact system. In this case, the direct access to the semiconductor chip is necessary and, consequentially, the package must be removed.

Various equipment has been used for the physical contact measurement: thermocouples, thermistors, scanning thermal probes, and multiple contact or blanket coatings, such as liquid crystals and thermographic phosphors [145-151]. The aforementioned equipment relies on the transfer of thermal energy from the DUT to the thermal sensors. In this case, the spatial resolution related to the contact measurements strictly depends on the size and the thermal capacitance of thermo-sensible materials. The ability to provide a temperature map by means of a matrix of thermocouple and a wide spatial resolution (can reach less than 100nm) are the main advantages. Notwithstanding, the physical contact methods are not over widespread in practical applications since the chip of the power module must be accessible to the thermal probe and in this perspective, the on-line measurements and high voltage operations are strongly limited. Furthermore, the measurement of the thermal variation of the power module strictly depends on the time response of the probe that may be considerably slower (few seconds) than the variation of the module JT.

The preliminary methods for the measurement of the JT in a power device have been obtained by using the Thermochromics Liquid Crystals [145] which consist of a thermal imaging tool for mapping surface and spatial temperature distributions. Nowadays, only in a few cases [146-147], the JT of an IGBT module has been experimentally measured during online converter operation. More specifically, the temperature has been determined by using several thermocouples physically connected to the chip. On the other hand, several works use the measurement of some thermocouples as target values used to prove the accuracy and effectiveness of new online junction temperature estimation models [148-151]. For example, the effectiveness of a model carried out, for a three-phase power module IGBT, by considering the transient thermal impedance has been

proved by using several thermocouples [148]. Experimental setup and an on-line control system that includes a microcontroller and a matrix of K-type thermocouples have been built up in order to verify a numerical thermal model for IGBT devices [149]. In [150] an electrical-thermal model has been carried out in terms of both the transient and steady-state responses. To validate the model, an array of thermocouple has been installed on the chip surface. A thermal model based on the Fourier series solution of heat conduction equations has been also validated by using several thermocouples placed both on the surface of the silicon die, on the base plate, and on the heat sink, in order to characterize the transient electrothermal behavior of an IGBT module [151].

4.2.4 Electrical Methods

Electrical methods for the JT measurement are often the preferred choice for the CM of power device because the temperature estimation can be carried out through the measurement of electrical quantities. More specifically, it is worth remembering that the proprieties of the semiconductor materials are temperature dependent and hence, the measurement of the voltage drop or the current that flows into the device can be used as a valid temperature estimator. Among various electrical CM methods, the Thermal Test Chips (TTCs) are directly fabricated on the die surface of the device, and the voltage drop can be used to estimate the temperature variations. On the other hand, the TSEPs are based on the measurement of the voltage drop (or current) during the converter operations. Generally, the measurement of the voltage drop can be carried out by using some voltage probes that are connected to the device terminals. The TSEPs are usually the preferred choice for CM because of their user-friendliness, fast response time to the temperature transients, and good accuracy.

4.2.4.1 Thermal Test Chips

TTCs have been originally developed for the thermal characterization of devices packages [152], and then they have also been used in IGBT power modules. TTCs act as thermal sensors to monitor the JT and they are fabricated on the proximity of the silicon chip.

TTCs can be suitable for online temperature measurements. Various types of TTCs have been realized, such as integrated diodes and resistance temperature detectors (RTDs) [153-161]. Since the forward voltage of the diodes strongly depends on the temperature variation, the measure of the voltage drop can be used for temperature estimation. It is worth remembering that the temperature presents an exponential dependence on the forward voltage. Likewise, RTDs are also used as the temperature-sensitive parameter because the voltage drop is related to the resistance variations. The variable resistance, R_t, can be expressed as:

$$R_t = R_0(1 + \alpha_0 \Delta T) \tag{96}$$

where R_0 is the value of the resistance at 0 °C, α_0 is the resistance temperature coefficient that strictly depends on the material, and ΔT is the temperature variation.

To use TTCs, a modified IGBT power module layout with an accessible on-chip temperature terminal has been proposed [153]. A string of diodes on the top of the chip has been fabricated and the measurement of the JT has been performed by measuring the forward voltage drop. Instead, in [154] a thin-film RTD placed on the top of the IGBT chip has been realized to measure the average temperature of the die. A similar solution where an NTC thermistor has been embedded in the IGBT power module has been also investigated [155]. Innovative use of a kelvin-emitter resistor, placed directly on the IGBT die surface, as a junction temperature sensor has been also adopted [156]. It provides only a local temperature measurement. While in [157] a chain of integrated diodes has been fabricated on the die surface with the aim to investigate the JT variations during a power cycling test.

The widespread of SiC power module in different power electronics applications has also driven forward the research of innovative control techniques that require real-time monitoring or estimation of the module's JT. In this perspective, several works [158-161] have been focused on the development of electrical models of the devices in which several NTC thermistors have been integrated on the die surface. The measurement of the temperature variation enables the estimation of the aging in a device and consequentially the device model can be continuously updated.

The main drawbacks of the TTCs are the production cost and the manufacturing complexity of the embedded sensors. Indeed, such layout modification complexity of the power module packaging can considerably increase and it also requires additional terminals for the temperature measurements. Furthermore, it is worth remembering that the diodes and RTDs can be affected by degradations along the lifetime of the device that may affect the accuracy of the measurement. These issues have limited the TTCs spread in commercial power devices.

4.2.4.2 Methods using the thermo-sensitive electrical parameters (TSEPs)

The CM methods outlined so far require visual or physical access to the chip. To overcome this limitation, the temperature measurement by thermo-sensitive electrical parameters (TSEPs) has been used as a valid alternative for the estimation of the JT of a power device. The key point consists of correlating the temperature of the semiconductor material with the electrical quantities during the normal operation of the converter. More specifically, the semiconductor devices have an intrinsic dependence on the temperature-related on different parameters, such as the mobility of the carriers $\mu(T)$, intrinsic concentration $n_i(T)$, and the bandgap energy $E_g(T)$. It is worth remembering that

the $E_g(T)$ and $n_i(T)$ increase at higher temperatures. While the $\mu(T)$ has a complex dependence with the temperature that is related to the doping concentration and traps in the gate oxide and silicon interface. Therefore, the temperature dependence on the aforementioned parameters may be written as [162]:

$$E_g(T) = E_g(T_0) - \alpha_1 \frac{T^2}{T + \beta_1} \tag{97}$$

$$n_i(T) = N^{\alpha_2} e^{-\gamma/T} \tag{98}$$

$$\mu(T) = \mu_0 \frac{\beta_2 \left(\frac{T}{T_0}\right)^{\alpha_3}}{1 + \beta_2 \left(\frac{T}{T_0}\right)^{\alpha_4}} \tag{99}$$

where α_1, α_2, α_3, β_1, β_2, and γ are empirical coefficients, N is the number per unit volume of effectively available levels states and T_0 is the room temperature.

Consequentially, the measurement of the electrical quantities measured at the device terminal can be used as a temperature estimator.

Therefore, TSEPs methods use passive voltage or current probes that measure the electrical quantities at the device electrodes, without direct access to the chip device, then the JT is estimated from these measurements. Furthermore, the TSEPs are the preferred approaches to obtain easily JT measurements on packaged devices with a fast time response (less than 100 microseconds). On the other hand, the TSEPs methods do not provide a thermal map of the DUT and hence the JT peak is often hard to evaluate [164]. Such an issue is more severe in multichip devices where the voltage or current measurements only provide a rough temperature of the whole device, without the possibility to know the effective temperature distribution among several paralleled chips [165]. In the following subsection, the main TSEPs methods are briefly discussed.

- **On state voltage measurement**

Among the different TSEPs methods, the on-state voltage measurement under low current injection has been the most used in many industrial and academic applications. In this case, the TSEP is the voltage drop across the device. The advantage of using this CM method relies on the easy calibration procedure and the negligible self-heating of the DUT.

This CM method is widely employed when the devices have a PN junction in their structure. More specifically, bearing in mind a MOSFET power device, the temperature varia-

tion can be evaluated as the on-resistance $R_{ds,on}$ fluctuations during the converter operations. For the sake of simplicity, the $R_{ds,on}$ can be approximated as:

$$R_{ds,on} \approx R_{ch} + R_d + R_{sub} + R_{cs} + R_{cd} + R_s + R_d + R_{jfet} \tag{100}$$

where R_{ch} is the channel resistance, R_d drift region resistance, R_{sub} is the substrate resistance, R_{cs} and R_{ds} are the source and drain contact resistances, R_s and R_d are the source and drain resistances and R_{jfet} is the JFET resistance. Furthermore, the R_{ch} and R_d can be evaluated as [163]:

$$R_{ch} = \frac{L_{ch}}{W_{ch}\mu_{ch}C_{ox}(V_{gs} - V_{th})} \tag{101}$$

$$R_d = \frac{L_d}{q\mu_d N_d A_d} \tag{102}$$

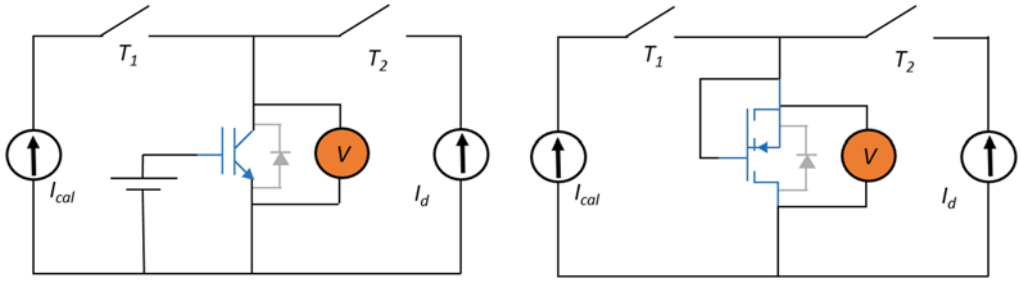
where L_{ch} and W_{ch} are, respectively, the channel length and width; C_{ox} is the gate capacitance; L_d and A_d are the drift region length and area; N_d is the doping concentration of the drift region; μ_{ch} and μ_d are the channel and drift region mobility. It is worth noting that the R_{ch} decreases at higher temperatures because of both the μ_{ch} and V_{th} decrease at higher temperatures. On the other hand, the R_d acts as a positive temperature coefficient thermistor due to the temperature dependence of μ_d that decreases at higher temperatures.

It is worth to underline that the temperature coefficient of the $R_{ds,on}$ may differ for the power devices from different vendors, that is mainly caused by the different design of the device. Therefore, notwithstanding an easier calibration procedure, the CM method must be calibrated when a different device is adopted.

Firstly, the calibration procedure is mandatory, which is used to find the relationship between the JT and the TSEP. Typically, the calibration step consists in the use of a current source I_{Cal}, in a range from 1 mA to tens of A. It is worth noting that during the calibration procedure, the device temperature can be usually fixed by a temperature-controlled heat sink. Then, the temperature measurement can be carried out during the dissipation stage, where the TSEP is measured in a typical converter application. In this case, a current source, *Id,* feeds the DUT in order to increase its temperature by means of power dissipations. Therefore, the voltage drop across the device, under known electrical conditions, is measured as a function of the temperature.

A simplified schematic of the circuits for the measurement of the voltage under low current is depicted in Figure 4:2 for an IGBT (Figure 4:2(a)) and a MOSFET (Figure 4:2(b)). The measurement can be carried out both for the on-state and-off state voltage. A voltmeter is usually connected in parallel to the DUT for the measurement of the voltage drop. It is worth noting that, the current *Ical* must be at least hundreds of mA to guaran-

tee a linear relationship between the voltage drop and the temperature [166-167]. In literature, many works [166-181] have focused on voltage measurement under low current injection in power diodes during forward polarization [170-173], in IGBT power modules [176-181], and also in power BJTs. Some works [180-181] have focused on the JT estimation in an IGBT power module whose on-state voltage (i.e. collector-emitter voltage, V_{CEon}) has a negative temperature coefficient. The main drawback of this method is the high dependence on the collector current during the measurement of the $V_{CE,on}$. Hence, the load current should be diverted during the measurement and this momentary interruption limits the use of this method in real-time applications.



(**a**) (**b**)

Figure 4:2 Electrical circuits for the static measurement of the voltage under a low current: (a) IGBT (b) MOSFET.

The principle of operation of the CM methods based on the on-state voltage measurement at high current injection is almost similar to the low current injection methods. The measurement of the $V_{CE,on}$ (or $V_{ds,on}$) voltage drop across the device is used as a TSEP as described for the low current injection mode. The main difference with respect to the previous CM method relies on the calibration procedure. More specifically, a higher current is used for the calibration procedure and it produces a non-negligible self-heating. In this perspective, the relation between the voltage drop on the DUT and the temperature depends also on the value of the injected current.

The experimental setup for the temperature measurement is depicted in Figure 4:3. A high current generator feeds the DUT with a pulsed current, I_H, and a voltmeter is connected in parallel to the DUT. It is important to point out that the measurement of the JT can be obtained during the heating process.

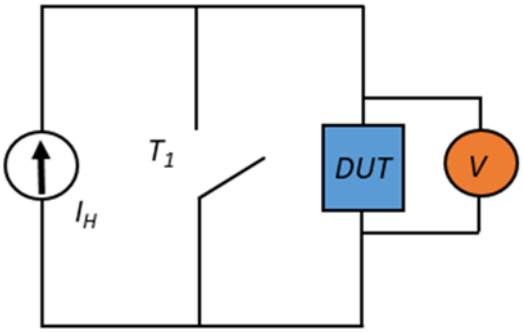


Figure 4:3. Electrical circuits of a DUT for the static measurement of the voltage under high current.

The TSEPs are usually the MOSFET on-state drain-source voltage [182], the power diodes forward voltage [176], and the IGBT on-state emitter-collector voltage [176]-[183]. The sensitivity of the aforementioned TSEP is strictly related to the on-state current value regardless of the specific device. The JT estimation is only practicable for current values greater than tens of Ampere [183]. Hence, this method appears to be very useful especially for online JT measurement during the normal converter operation. Several circuit solutions to measure the V_{CEon} of the power device have been devised [166],[176],[182-185].

This approach also presents some limitations due to the voltage swing between the on-state and off-state of the device. This implies the use of advanced electronic sensing circuits, thus increasing the complexity of the system. Innovative and compact sensing circuit to face these issues have been proposed [182,183].

Another issue is the contact resistances of the voltage probes that cause an undesired voltage drop that may produce an overestimation of the JT measurement [184]. This issue has been partially mitigated with a correction factor based on the layout of the power module [184-185]. Unfortunately, the introduced correction factor has to be calibrated as the device aging progress.

- **Saturation current**

The measurement of the saturation current, I_{sat}, has been also used as TSEP [173],[179],[186-187] in power module with IGBTs or MOSFETs. This current can be measured by using a current probe or a voltage probe (by adding a shunt resistor). The electrical quantities measured provide a JT estimation due to the dependence on the chip temperature of the channel electron mobility, μ_{ch}, of the threshold, V_{th}, and of the PNP transistor current gain β for the IGBT [186]. It is worth remembering that the current I_{sat} shows a complex temperature dependence, but under the assumption that all the devices are at the same temperature and by neglecting the self-heating, the current I_{sat} in a device can be simply approximated as:

$$I_{sat} = \frac{1}{2}\frac{\mu_{ch}(T)W_{ch}C_{ox}}{L_{ch}}\left(V_{GS} - V_{th}(T)\right)^2 \quad (103)$$

The measurement setup consists of a voltage source, V_{GT}, connected between the gate-emitter (or gate-source) terminals of the DUT and a DC source voltage, V_D, connected between the drain-source or collector-emitter terminals of the DUT. Figure 4:4 shows the setup for an IGBT device. The voltage value of V_{GT} is usually higher than the threshold voltage V_{th} of the device and a pulsed current is injected into the DUT by controlling the switch T_1. The saturation current can be measured through the voltage drop on the R_{shunt}. The setup clearly demonstrates that the thermal characterization of the device cannot be performed during the online converter operation.

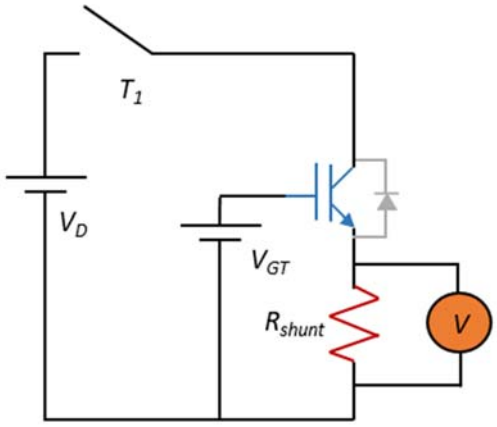


Figure 4:4 Electrical circuits for the measurement of the saturation current in an IGBT device.

The first procedure is the calibration step, where the DUT is usually placed in a controlled hot plate that overheats the device, and hence, the I_{sat} is measured at varying plate temperature. Then, the measurement procedure (see Figure 4:4) consists to perform a non-destructive short-circuit in order to produce a significant channel temperature variation during a short time. In this perspective, the measurement variation of the current I_{sat} can be associated with a specific temperature value. Moreover, the temperature calibration may not be performed without power losses that influence the device self-heating [186-187]. Furthermore, it has been demonstrated that JT measurement is more accurate only for high temperatures.

- **Gate Threshold Voltage**

The threshold voltage V_{th} is defined as the voltage to be applied to the gate-source terminals to have a given current, which is the minimum current that must flow into the device channel to assume the device turned on. Instead, from the standpoint of power electronic devices, the V_{th} is defined as the level of gate bias needed to observe a transition from weak-inversion to strong-inversion. For a MOS transistor structure, the V_{th} can be approximated as [188] :

$$V_{th} \approx 2\varphi_F(T) - \frac{Q_{SS}}{C_O} + \varphi_{ms}(T) + \sqrt{\frac{2\varepsilon q N_A}{C_O}}\sqrt{2\varphi_F(T)} \quad (104)$$

where φ_F is the Fermi potential Q_{SS} is the extrinsic change due to surface states, C_O is the gate oxide capacitance, φ_{ms} is the metal-semiconductor work function difference, ε is the oxide dielectric constant, q is the elementary charge unit and N_A is the body doping.

By referring to the (9), it can be demonstrated that the voltage V_{TH} decreases with increasing temperature [188] and it is a TSEP useful for temperature monitoring of MOSFETs [175], [189], and IGBTs [179-180], [190-191]. A potential measurement setup for the calibration procedure and the measurement of the V_{th} as TSEP in the case of an IGBT device is depicted in Figure 4:5.

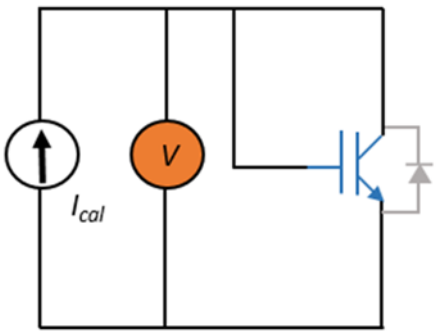


Figure 4:5 Circuit for the calibration step of the threshold voltage method.

The gate and drain (collector) terminals are short-circuited and a current source, I_{cal}, feeds the DUT while a voltmeter measures the V_{th}. It is worth noting that the calibration step is based on the low current injection method and whereby, the self-heating is negligible.

Some works [179-180] have focused on the temperature dependence of the V_{th} measured by varying the collector-emitter voltage and the current collector value for an IGBT device. The I_{cal} value has to be higher than 5 mA in order to have a correct calibration step for high temperatures and high sensitivity [179-180]. Other works [190-191] have

focused on the temperature measurements after the power dissipation of the device. More specifically, a current source with two different current levels, one for dissipation (high current injection) and the other for JT measurement (low current injection) has been proposed. This CM method is not suitable for online condition monitoring.

- **Gate–Source or Gate-Emitter Voltage turn ON-OFF**

The gate-emitter (source) voltage, V_{ge} (or V_{gs}) is used as a TSEP during the turn-on and turn-off of the switch [194-195]. The high sensitivity and the linear dependence of V_{ge} (or V_{gs}) with the temperature is the strength of this method. Similarly to the threshold voltage method, the V_{ge} (or V_{gs}) TSEP method cannot be used for online JT estimation in a power converter application, because the gate and collector (drain) terminal has to be shorted. The experimental setup of the gate-source or gate-emitter voltage as CM method is very similar to the threshold voltage one (see Figure 4:5). In this case the current injected into the DUT is higher than the current used in the threshold voltage method and consequentially the self-heating is not negligible.

Figure 4:6 depicts the simulation of the gate-emitter voltage V_{ge} of an IGBT during the turn-off at varying the device temperature. It is worth noting that the following analysis can be done by considering the turn-on of a device. The Miller plateau becomes wider as the temperature increases. In other terms, the time shift Δt in the figure is strictly related to the temperature of the chip and it can be detected by using a time counter that triggers from the first falling edge to the second one after the Miller plateau.

The Miller plateau width t_d can be approximated as [194]:

$$t_d = \frac{R_{Gint}(T) \cdot C_{rss}(T) \cdot (V_{DD} - V_{ON})}{\left(\frac{I_{load}(T)}{g_m(T)} + V_{th}(T)\right)} \tag{105}$$

where R_{Gint} is the internal gate resistance, C_{rss} is the Miller capacitance, V_{DD} is the DC-link voltage, V_{ON} is the on-state voltage, I_{load} is the load current, g_m is the transconductance. Equation (10) shows that t_d is directly proportional to C_{rss} and R_{Gint}. It is worth noting that the impact of temperature variation on V_{ON} and V_{DD} is negligible, while the temperature variation of the terms (I_{load} /g_m) and V_{TH} partly neutralize each other. The internal gate resistance depends on the temperature as the electron mobility decreases at higher temperatures. Therefore, t_d increases at higher temperatures due to the temperature dependence of C_{rss} and R_{Gint}. Therefore, the time interval t_d of the Miller plateau in the V_{ge} (or V_{gs}) voltage can be used as a TSEP to estimate the JT of IGBTs (or MOSFETs).

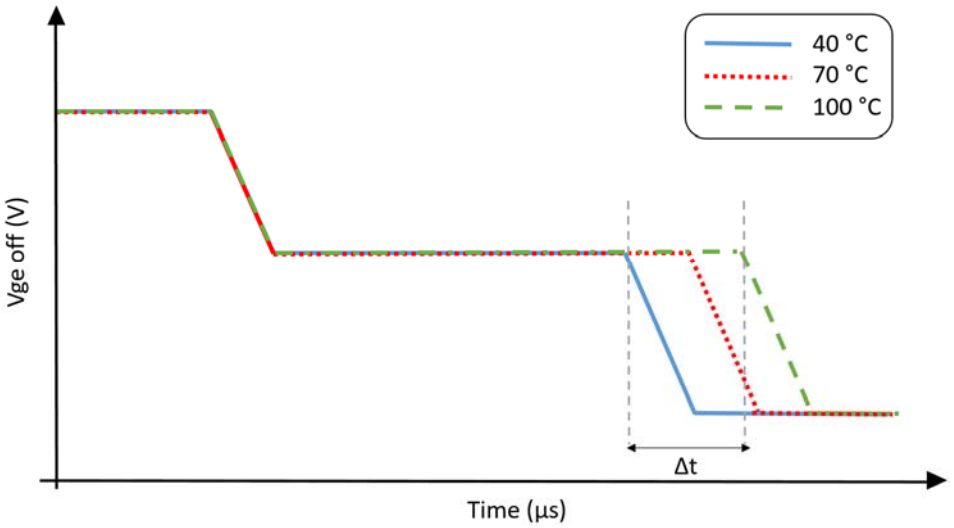


Figure 4:6 Simulated V_{ge} waveform during the turn off of an IGBT by varying the temperature working operations.

The authors in [194] have proved the temperature independence of the collector-emitter voltage. Instead, the calibration step measurement has been improved in [138] where an auxiliary sensing circuit has been added to the gate driver with the aim to reduce undesirable oscillations during the turn off of the device. While in [195] the linear dependence of t_d respect the temperature of the chip has been demonstrated and also, a parametric analysis by varying the JT, I_{load}, and the DC-link voltage has been performed.

- **Turn on-off delay time**

The switching behavior of the power devices has been also adopted as a CM method [196-202]. In this case, the TSEPs are the voltage and current waveforms during the turn-on and turn-off of the DUT. This method is quite similar to the V_{ge} (or V_{gs}) TSEP method, but the JT monitoring can be performed online during the converter operations. More specifically, the delay, ΔD, at turn-on, between the collector current i_c and the gate-emitter voltage V_{ge} for an IGBT device (see Figure 4:7) is used as a TSEP [196-198], as well as the delay between the drain current i_d and the gate-source voltage V_{gs} for a MOSFET device. Bearing in mind the IGBT devices, the turn-on delay is of great interest because ΔD increases linearly with the temperature [198], it only depends on the dc-link voltage and it is not influenced by the value of i_c. More specifically, during the switching on time interval t_{on}, the gate current charges the gate-emitter capacitance C_{GE}

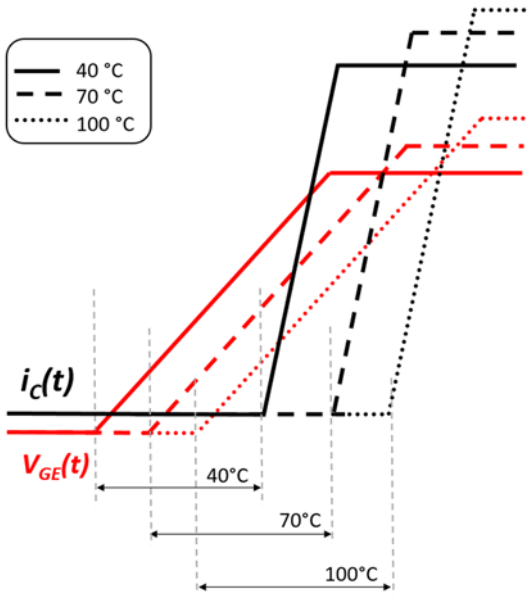


Figure 4:7 Simplified i_c -V_{ge} turn ON waveforms of an IGB at different temperature working operations.

that is connected in series with the gate resistance R_{Gint}. Therefore, the zero state waveform of the $v_{ge}(t)$ can be written as [194]:

$$v_{ge}(t) = V_G \cdot \left(1 - e^{t/\tau}\right)$$
$$\tau \approx R_{Gint}\,(T) \cdot C_{GE}(T) \tag{106}$$
$$t_{ON} \approx \tau(T) \cdot \ln\left(1 - \frac{V_{th}(T)}{V_G}\right)$$

where V_G is the driver gate-emitter voltage.

The dependence on the temperature of the turn-on delay ΔD can be analyzed by combining both the (9) and (11). V_{th} decreases as the temperature increases and the value of the time constant τ depends on the temperature variations too. It is worth underlining that the gate charge (the intrinsic gate capacitances) has a weak dependence on the temperature while the internal gate-resistance R_{Gint} has a stronger dependence on temperature due to the channel mobility μ that decreases at higher temperatures.

Figure 4:7 depicts the simulation of an ideal IGBT device during the turn-on at varying working operation temperatures (40 °C, 70°C and 100°C). The shift on the right of the waveforms is strictly related to the aforementioned temperature dependence. The previous method is valid also for the MOSFETs.

An advanced sensing circuit (voltage probes, FPGA, ADC) that records the transient evolutions of both V_{ge} and i_c waveforms have been proposed in [197]. The delay is calculated as the time interval between the time instant the rising edge of the V_{ge} is detected, and the rising edge of the current i_c (Figure 4:7). This method allows a sensitivity close to

2 ns/◦C. Moreover, since a gate resistor with a large resistance improves the accuracy of the temperature measurements during the switching behavior of the converter but worsen the efficiency, a variable gate resistor has been proposed in order to set a higher value exclusively when the JT is measured [198].

Similarly, the turn-off delay can also be used as a TSEP, reaching a sensitivity level close to the one obtained with the turn-on delay method [199]. Other works have proposed an alternative sensing circuit for the JT estimation during the turn OFF [200]. However, the turn-off delay method does not attract interest because it is not linear at high-temperature operations, and the time delay depends greatly both on the i_c current and on the DC link voltage [201-202].

In general, the turn-on and turn-off TSEPs methods require high bandwidth sensors and an advanced sampling circuit for temperature measurement, that increase considerably the cost of the overall system. Furthermore, these methods usually require an external circuit to trigger a counter for the estimation of the turn-on and turn-off delay time.

- **Current and voltage change rate**

In the last decade, the research has moved from the study of the electrical quantities (such as the voltage and current waveforms) to their derivative functions, which are observed during the device commutation, called dynamic thermo-sensitive electrical parameter (DTSEPs) methods. More specifically, the collector-emitter voltage change rate (dv_{ce}/dt) and the collector current change rate (di_c/dt) have been used as temperature estimators [203-207]. The dependence of both dv_{ce}/dt and di_c/dt with respect to the temperature has been explored theoretically and confirmed also experimentally [205-207].

As an example, the dV_{ce}/dt in an IGBT device can be approximated as [206]:

$$\frac{dv_{ce}}{dt} \approx \frac{1}{\tau_{gc}(T)} \left(\frac{V_{GE,ON} - V_{GE,OFF}}{1 + \left({C_O}/{g_m(T)\tau_{gc}(T)} \right)} \right) \tag{107}$$

$$\tau_{gc} \approx R_{Gint}(T) \cdot C_{GC}(T)$$

where C_O is the charge extraction capacitance, $V_{GE,\ ON,}$ and $V_{GE,\ OFF}$ are the on-off gate driver voltages.

It is worth noting that the term dV_{ce}/dt depends on the physical parameters of the IGBT device and the temperature dependence is not easy to obtain. More specifically, the JT affects the dV_{ce}/dt through the MOS channel parameters such as the L_{ch}, W_{ch}, the emitter recombination parameter, the channel mobility, and so on. A detailed discussion of all the temperature parameter dependencies is given in [206]. The dependence of many parameters influencing the derivative quantities on the temperature strongly limits the use of this CM method for online JT measurement in practical power converter applications. A wide investigation of the IGBT maximum dv_{ce}/dt for the JT estimation has revealed the severe limits due to the influence of the control method, the DC link voltage, and the load current [206]. Likewise, the maximum di_c/dt during turn-off as TSEPs has been also investigated [207]. Even in this case, the measurement of the current change rate has been performed by using an additional circuit able at capturing the current and voltage transient dynamics, which require both high bandwidth sensors and the use of voltage probes and Rogowski coil probes. Furthermore, this sensing circuit should be designed to avoid any disturbance, and also it has to be insensitive to the temperature variation of the system.

In the last generations of IGBT and SiC high power modules, the Kelvin emitter pin has been introduced. Such an additional pin involves in the package an integrated inherent parasitic inductance L_{eE} between the Kelvin pin and power emitters pin [208-210], as shown in Figure 4:8. The transient collector current characteristic during the turn OFF process has been introduced as a potential DTSEP, called maximum collector current falling rate $-dI_C/dt_{max}$ [210]: the collector current I_C flows in the inductance L_{eE} and the resulting voltage drop enables an easier investigation of the JT measurement.

Also in [207], both the static and dynamic behaviors of the stored carriers in the IGBT collector current during the falling rate have been analyzed. Furthermore, the influences of the physical parameters of the device on the temperature sensitivity of $-dI_C/dt_{max}$ have been fully investigated. However, several drawbacks of these methods are related to the strong dependence of the applied voltage and the gate resistance, and the thermal characterization can be done only offline.

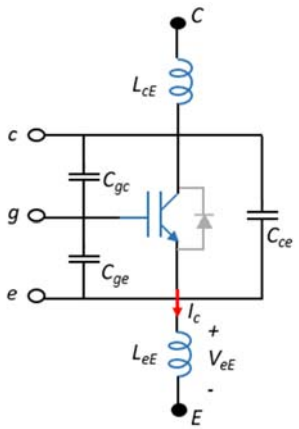


Figure 4:8 IGBT module equivalent circuit.

- **Peak gate current**

An innovative method for JT measurement in IGBTs and MOSFETs, based on the temperature-dependent of the internal gate resistance, has been studied in the last years. Firstly, the measure of the R_{Gint} in a power module has been already faced out by using a standard LCR meter [211], where a common approach is to consider the equivalent series resistance (ESR) of both the gate–emitter and gate–collector capacitance (see Figure 4:9(a)). Another method to estimate the R_{Gint} variation has been related to the measurement of the gate charge during the turn-on of the DUT [212]. Therefore, the peak gate current during the turn-on switching behavior has been assumed as a valid TSEP.

The JT measurement via the peak gate current can be studied during the standard charging cycles of the gate terminal. Considering an IGBT device, the turn-on process starts when the gate driver output voltage changes from a negative value to a positive one. Therefore, the gate current can be computed as the step response of a second-order RLC circuit [214] (see Figure 4:9(a)). The parasitic inductance L_G can be neglected and the peak current can be estimated by simply using the Ohm's law provided that the RLC circuit is overdamped. It is worth noting that the external gate resistance R_{Gext} has not a significant temperature dependence. Therefore, the temperature variation of R_{Gint} can be carried out by the measure of the peak current variation. In other words, the maximum value of the gate current provides a suitable strategy for the measurement of the chip JT. The measurement circuit is shown in Figure 4:9(b). The peak voltage on the external gate resistor during turn-on is measured with a peak detector circuit (a differential amplifier and a peak detector). Then, the acquired data are processed by an Analog to Digital converter to the microcontroller. This measurement circuit can be integrated into the gate driver, and the JT monitoring can be operated during the online operation of the converter. This method does not require calibration steps and more importantly, the voltage peak has a linear relationship with the temperature.

Only a few works have focused on the peak gate current as a TSEPs method. More specifically, the sensing circuit depicted in Figure 4:9(b) has been proposed in [215-216] where the JT has been esteemed in an IGBT power module. The authors have asserted that the proposed method has better accuracy for JT measurement compared to other TSEP methods in the literature. However, this method requires additional complex trigger circuits for the measurement of JT, which may introduce additional disturbance in the system. It is worth remembering that the aging of the power module may affect the internal gate resistances. Hence, a correction factor should be introduced for calibration with the aging of the device.

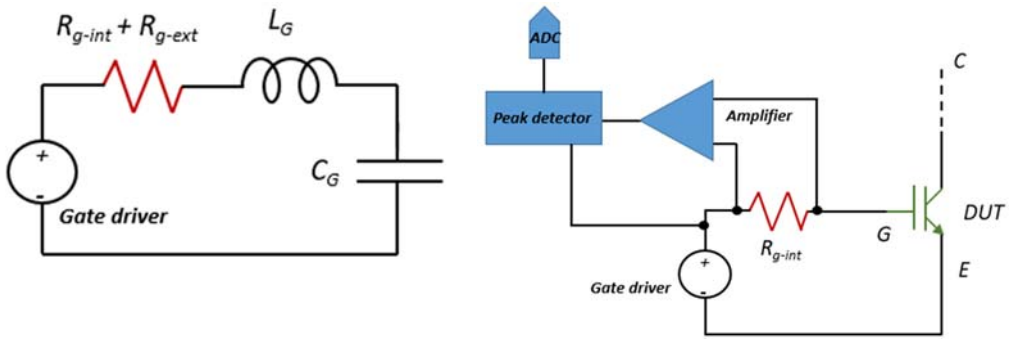


Figure 4:9 Gate driver RLC network. (a) Peak Detector Schematic to detect peak voltage over the external gate resistor.

4.2.5 Comparison of the CM methods

Table 4:2 Summarization of different CM methods.

Legend	Method	Advantages	Disadvantages
A	OPTICAL - Fiber optic	• On line measurements • High sensitivity • High accuracy	• Package modification • High cost
B	OPTICAL - Photodiode sensor - internal	• Online measurements • Contactless	• Technology not mature • Package modification
C	OPTICAL - Photodiode sensor - external	• Online measurements • Contactless	• Package modification
D	OPTICAL - IR camera	• Spatial resolution • Contactless	• Package modification • Poor response time • Poor accuracy
E	OPTICAL - IR camera print	• Spatial resolution • Contactless	• Package removal • Poor response time • Poor accuracy

F	Acoustic	• On line measurements • Contactless	• Technology not mature • Noise sensitive • High cost
G	Physical	• On line measurements • Good linearity • Good sensitivity	• Package modification • Poor response time • Obsolete
H	TTCs - NTC	• On line measurements • Good linearity	• Layout modification • Aging sensitive
I	TTCs - Diode	• On line measurements • Good sensitivity	• Layout modification • Poor linearity
J	TSEP - On-state voltage, low current	• High sensitivity • High linearity • Easy calibration	• High-cost sensing • Offline measurements
K	TSEP - Gate threshold voltage	• Good sensitivity • Good linearity	• Offline measurements • Unplug DUT
L	TSEP - On-state voltage, high current	• On line measurements • High linearity	• High-cost sensing • Aging sensitive • Load current dependence
M	TSEP - Saturation current	• High sensitivity	• Offline measurements • Poor linearity
N	TSEP - Gate turn OFF voltage	• High linearity	• Offline measurements • High-cost sensing • Inaccurate measurement
O	TSEP - Turn on-off delay time	• On line measurements • High linearity	• Aging sensitive • High-cost sensing

		• Less parameter-dependent	
P	TSEP - Peak gate current	• On line measurements • Good linearity • Easy to implement	• Aging sensitive • High-cost sensing
Q	TSEP – Voltage-Current change rate	• Good sensitivity • Good linearity	• Offline measurements • High-cost sensing • Gate resistance dependence

Table 4:2 summarizes all the CM methods discussed previously. A comparison between the advantages and disadvantages of each approach has been outlined. It has been strongly highlighted the linear dependence with the temperature in the case of the optical, physical, and TTCs methods. Furthermore, the investigation revealed that the aforementioned methods and a few TSEPs methods (on-state voltage high current, turn on-off delay time, and peak gate current) can be adopted for online measurements in a real power converter application.

On the other hand, it has emerged as the TTCs requires a layout modification of the power module, notwithstanding the high linearity and independence from any physical parameters. Although the optical and acoustic methods are able at contactless monitoring the SOH, the technology is not yet well mature to be widespread in commercial solutions.

4.3 Intrusiveness criteria classification

The SOH of power electronic devices and systems can be evaluated with the research of innovative and enhanced strategies of CM methods. Several works have presented different CM strategies aiming at reaching a high level of accuracy and user-friendliness. On the other hand, the estimation of the intrusiveness level of the various CM methods has not yet drawn adequate attention.

In the following, some intrusiveness criteria and a classification that takes into account several factors that may affect the monitoring operations in a power conversion system have been discussed. Firstly, it has been analyzed whether a specific CM method needs to modify the device structure, then the impact of the monitoring on the converter operations as well as any modification on the overall power conversion system has been investigated. In the following, the three different intrusiveness criteria have been de-

scribed, then the CM methods have been analyzed based on the introduced intrusiveness criteria.

4.3.1 Description of the Intrusiveness criteria

4.3.1.1 Power device modification

The device modification criterion relates to alterations or changes in the structure of the power devices (e.g. package, layout, and so on) due to a selected CM method. More specifically, the monitoring of the SOH needs the measurement of a physical or electrical quantity, the greater the device modifications necessary to perform the measurement the greater the CM method intrusiveness at the power device level.

In some cases, the CM method does not involve any changes in the device, such as the acoustic method [111-119] where an acoustic spectrometer is placed in the proximity of the DUT. Similarly, only the electrical quantities are measured at the device terminals in the case of TSEPs methods. On the other hand, other CM methods have to drill one or several holes on the package structure for the JT measurements. For example, the use of the fiber optical method [120-144] requires the inclusion of probes close to the die. Other CM methods require a particular modification in the packaging structure of the device, such as an integrated photodiode sensor for the JT estimation in a SiC power module. In this case, the sensor has to be integrated inside the device package and two terminal has to be added to the pin layout of the power module. An impressive modification of the internal layout of a power module may occur in the case of TTCs [152-161], where a diode or an RTDs is fabricated on the surface of the die. While in different works the package has to be partially removed or a complete lift-off of the package has to be performed for the measurements, such as the use of an IR camera when a painting solution is used at the device surface.

4.3.1.2 Modification of power conversion system operation

The conversion system operation criterion is based on the level of influence during the common working operation of a power converter. Several CM methods are not able to carry out the JT measurements during the online operation of the converter, and in this perspective, the power conversion system has to be shut off. Therefore, these CM methods are strongly intrusive especially when the power converter has to be unplugged from the application and a dedicated experimental setup has to be used for the monitoring. Most TSEPs methods are strongly invasive such as those based on the measurement of the on-state voltage under low current injection, the saturation current, the gate threshold voltage, the gate turn-off delay, the current change rate, and the voltage change rate [164-200]. On the other hand, the physical [145-151], optical [120-144], and acoustic methods [111-119] can be used during online converter opera-

tions. Furthermore, it must be taken into account also the influence of the voltage probes during the measurements, such as the probe bandwidth or o any contact of the probe with the DUT. For example, the thermocouples [145-151] are directly placed on the die surface, while in a TSEPs method [164-216] the voltage probes are connected in the external connectors.

4.3.1.3 System modification

The overall system can be assumed as the set of power converters, the load, and power supplies. The system modification criterion is based on the level of changes in the systems components and/or their interconnections, that can be also specific for a particular application. This criterion also takes into account the impact of a CM method in terms of the use of cumbersome tools for data acquisition, the need to open the chassis protection of the system, whereas the auxiliary circuitry may be bulky respect the applications and so on.

The system modification criterion strongly depends on the specific application and in this perspective, it has to be evaluated how the CM methods may impact in terms of size and modification on the overall system. For example, various optical methods [120-144] may have a different level of intrusiveness. Bearing in mind the IR camera used after painting the surface of the device asks for the opening of the converter system and therefore, it is extremely intrusive. While in the case of the integrated photodiode the level of intrusiveness is lower since the voltage drop is measured thought two BNC cables connected to an oscilloscope. The intrusiveness of the physical methods, such as the thermocouple, is higher than the previous ones because of an auxiliary circuit is needed in order to correlate the resistance variation with the JT estimation. Furthermore, in the case of several TSEPs methods [164-216], the intrusiveness level is even higher due to the need to use auxiliary switches or auxiliary signal conditioning circuits that are able to detect the JT variation in the power module.

4.3.2 Classification of the CM methods based on the intrusiveness criteria

The adoption of a unique figure of merit (FOM) representing the intrusiveness of a CM is highly desired. In this perspective, it is advantageous to first define an index of intrusiveness for each criterion. Therefore, a triplet of numerical marks, each in the range from 1 (nonintrusive) to 10 (fully intrusive), is assigned to a CM method according to the intrusiveness criteria. More specifically, for a given criterion the following procedure has been adopted to assign the marks to each CM method. A mark equal to 1 has been assigned to the methods fully nonintrusive. A CM method satisfies such a condition when there is not any change after the introduction of the method. After that, the CM methods that involve a slight modification have been analyzed. They are ranked according to

the modification degree and a mark in the range 2-4 has been assigned to each of them according to my opinion. Similarly, the other methods involving an intermediate modification have been analyzed and a mark in the range 5-7 has been assigned to them. Finally, a mark between 8 and 10 has been assigned to the CM methods involving a strong modification. Although the assignment of the mark is subjective the rank of the CM methods according to an intrusiveness criterion can be considered almost unbiased.

4.3.2.1 FOM_D*: Evaluation of the intrusiveness according to the* Device modification criterion

The device modification criterion refers to alterations or changes in the structure of a power device due to a given CM method with respect to the same device without employing any CM. In this perspective, each CM method has been analyzed in-depth to reveal the intrusiveness at the device level and, thus the index of intrusiveness FOM_D has been assigned. The lowest value of FOM_D is assigned when no modification or packaging alterations are done neither by the manufacturer and the user. The FOM_D index increase as the package modifications increase (e.g. drills in the package to insert probes). Furthermore, FOM_D also increases in case of changes in the layout of the power module, and finally, FOM_D is set to the highest value when there is a complete package removal. In the following, the CM methods are ranked according to the device modification intrusiveness criterion, and the marks are assigned by adopting the procedure described before.

TSEPs CM methods present the lowest intrusiveness because the monitoring of the temperature can be carried out by exclusively measuring the electrical quantities on the device terminals. As evident, this approach does not require any modification of the device package or layout. Likewise, the acoustic methods (F) have also the lowest intrusiveness because an acoustic spectrometer records the acoustic emission, and then it is possible to estimate the state of the aging of the power module without any modification. The spectrometer may be placed close to the device, around a few centimeters, without any package modifications. In the field of optical CM methods, only the use of an IR camera (D) shows the lowest FOM_D. In this case, the measurement of the device temperature can be carried out by placing the IR camera until one meter from the DUT. Hence, the FOM_D has been set equal to 1 for all these methods. On the other hand, another optical CM method, that is the one adopting the fiber optic (A), it has been considered a little more intrusive with respect to the previous ones. In this case, a small device package modification has been introduced: two small holes in the package to insert the fiber optic wires close to the device chip. In this perspective, a FOM_D equal to 2 has been assigned. The intrusiveness of the optical CM methods based on photodiode sensor inside the package should be distinguished in two different scenarios:

- the sensor has been fabricated directly (*a priori*) into the package from the device manufacturer (B).

- the photodiode is placed a *posteriori* by a user (C).

In the first case, the overall package can be optimized by the manufacturer in order for the device to perform well meanwhile the modification could be limited. In this perspective, the device modifications are more than a simple hole on the package and hence, it has been assigned a FOM_D equal to 4. In the other scenario, the device package has to be opened and the photodiode placed by a user. Hence, the latter solution has higher intrusiveness with respect to the integrated one, and hence, it has been assigned a FOM_D equal to 5.

Whereas the DUT has been printed on the surface to increase its emissivity in the case of an IR camera (E), FOM_D must be set to a higher value due to the partial opening of the package structure. In this case, a FOM_D value equals to 6 has been assigned. In a similar way, the use of a TTCs such as the RTD (H) and integrated diodes (I) that are usually fabricated on the surface of the die allows the measurement of the JT by measuring the voltage drop. Therefore, the internal layout and the pin layout of the power module has to be redesigned from the original one. In this perspective, the FOM_D value that has been assigned 8 and 7 respectively because they require a substantial redesign of the device layout.

Finally, the CM method using the thermocouple (G) is the most intrusive due to the need to open the device package and to place the thermistor on the chip of the power (FOM_D equals to 9). It is worth remembering that the device package must be drilled to place the BNC cables for the measurements.

Figure 4:10 depicts a bar diagram that represents the values of FOM_D of each CM method.

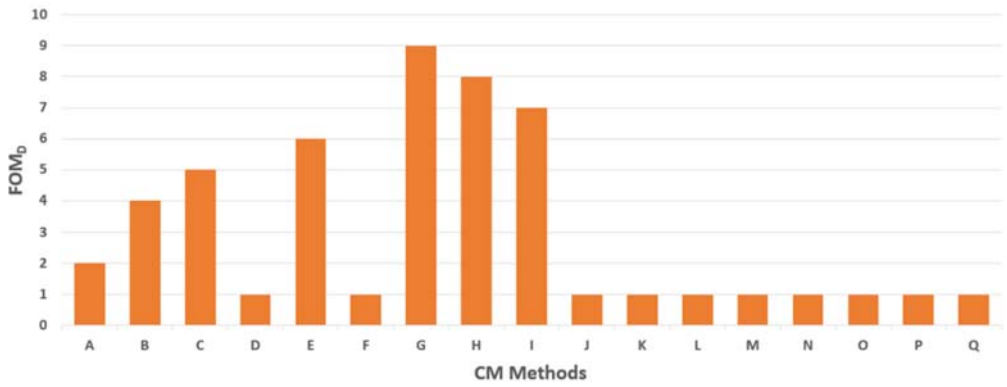


Figure 4:10 FOM_D assigned to the CM methods

4.3.2.2 FOM$_C$: *Evaluation of the intrusiveness according to the* Conversion system operation criterion

The conversion system operation criterion refers to the impact of a CM method on the normal working operations of a power converter. In this perspective, each CM method has been analyzed with the aim to fully understand the intrusiveness level, thus the index of intrusiveness FOM_C has been assigned. The lowest value of FOM_C is assigned

when on-line monitoring is possible and there is not any physical contact between the conversion system and the measurement system (e.g. the measurement is performed without any probes or wires). It is worth underlining that the electrical probes have several limitations in their use such as limited bandwidth, intrinsic parasitic capacitances, and also, they cannot always be used for high voltage operations. In this perspective, the use of the voltage or current probes may be intrusive for the measurements. In the following, the CM methods are ranked according to the conversion operation intrusiveness criterion, and the marks are assigned by adopting the procedure described before.

It is a matter of fact that all the optical CM methods that are based on the measurement of the light brightness or the measurement of the emissivity change of material present the lowest intrusiveness. As an example, the use of an IR camera (D) is fully non-intrusive since the spatial measurement of the temperature gradient on the power module can be done without any direct contact with the converter. Furthermore, both the use of the optical fibers (A) or the integrated photodiodes (B) or the external photodiodes (C) introduce the lowest value of intrusiveness, where the monitoring of the JT can be carried out without direct contact and without interrupting the converter operations. In a similar way, the acoustic method (F) uses an acoustic spectrometer placed in the proximity of the device, and therefore, the converter is not affected by the use of this method. Hence, the FOM_C has been also set equal to 1 to all these CM methods.

The physical methods (G) and the TTCs (H and I), have a slightly higher level of intrusiveness with respect to the previous CM methods. More specifically, to perform the JT estimation, a voltage drop is measured by using a voltage probe on the external connectors of the power module. Therefore, the monitoring of the device SOH could be lightly affected by the sensing equipment that may introduce a little disturbance, thus a FOM_C equal to 2 has been assigned.

The TSEPs Turn off-on delay time (O) and peak gate current (P) CM methods are able to carry out the JT monitoring during online working operations. More specifically, for the turn-off delay, the time delay between the voltage and current waveforms are measured. Therefore, the use of at least two different probes (e.g. current probe and voltage probe) is mandatory. In a similar way, the peak current gate CM method requires the use of two voltage probes, and hence, the level of intrusiveness is comparable. In these cases, the FOM_C has been set equal to 4 for both the CM methods. The On-state voltage at higher current (L) also allows the monitoring of the JT during the online operation, but at cost of a high current injected into the device (30 A is a typical value). Notwithstanding the ability to monitor the JT during online operations, the pulsed current injected into the device must have a time width of hundreds of microseconds, and consequentially the converter operations have to be changed for a short time period from the typical functionalities. Furthermore, the measured TSEP is the on-state voltage, and hence, it requires an active clamping and extremely sensitive circuit to measure the lower on-state voltage, which increases the level of intrusiveness. In applications where the monitoring must be frequently or continuously performed such a CM method become equiv-

alent to the ones that cannot be performed online since none of them is usable in such kinds of application. In this case, the FOM_C has been set equal to 8 due to the alteration in the converter system, which is strongly greater than the previous methods.

On the other hand, the On state voltage under low-level injection (J), the threshold voltage (K), the saturation current (M), the gate emitter voltage turn on-off (N), and the voltage-current change rate (Q) CM methods shows the highest level of intrusiveness. These TSEPs methods need to shut off the converter in order to perform the JT measurement. Moreover, these methods require the unplugging of the device and a dedicated circuit (such as switches, current generator, etc.) has to be used for monitoring. Consequently, a FOM_C equal to 10 as been assigned to them.

Figure 4:11 summarizes the values of FOMC for each specific CM method.

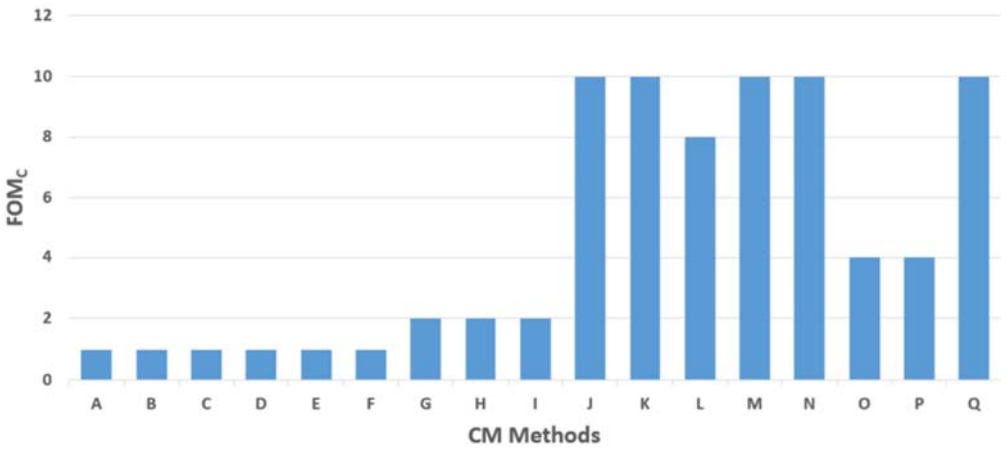


Figure 4:11 FOM_C assigned to the CM methods.

4.3.2.3 FOM$_S$*: Evaluation of the intrusiveness according to the* System modification criterion

The System modification criterion has been defined as the impact of a CM method on the conversion system (such as the chassis removal) as well as the introduction of components or modifications in the final application (e.g. the addition of auxiliary electrical circuits).

Several CM methods have been analyzed with the aim to highlight their intrusiveness level in order to rank them and to assign the index of intrusiveness FOM_S based on the system modification criterion. The lowest value of FOM_S is related to the case when limited modifications or addition of auxiliary electrical circuits are introduced in the final applications with respect to the scenario without CM.

The measurement of the JT by means of an integrated photodiode (B) only requires the measurement of the voltage drop on the resistor. This means that no auxiliary circuit or

external supply voltages are needed for the monitoring. Hence, the use of integrated photodiode has the lowest intrusiveness, thus a FOM_S equal to 1 has been assigned to the method of adopting an integrated photodiode. On the other hand, the adoption of an external photodiode (C) involves a little higher intrusiveness since it usually needs a signal conditioning and external power supply. Similar considerations are valid for TTCs based CM methods. The monitoring of the JT consists of a simple measurement of the voltage variation that can be carried out by using a voltmeter sensing circuit. Therefore, the intrusiveness level in the real system is very low. Then a FOM_S equal to 2 has been assigned to these three methods (C-H-I). Instead, the thermocouples (G) lead to a further slight increment in the level of intrusiveness because a simple and compact auxiliary circuit (e.g. Wheatstone bridge) able to detect the resistance changing with the temperature is usually employed. In a similar way, the turn on-off delay (O) and the peak current (P) CM methods have the same level of intrusiveness. In the first one, the measure of the JT can be carried out by measuring the time delay between the voltage and the current of the DUT. The time interval measurement can be done by using an FPGA or microcontroller that is able to detect the signal variations in a range of microseconds. The sensing circuit may be integrated into the gate driver, otherwise, the auxiliary sensing circuits are placed close to the converter system. Similarly, the peak gate current method uses two voltages probes and a detecting circuit that is able to measure the voltage variation on the gate resistance. A FOM_S equal to 3 has been assigned to them (G-O-P).

The JT monitoring through an IR camera (D) requires that the chassis of the converter system has to be removed, and the IR camera is placed at about one meter from the DUT. Besides, whereas the device surface must be varnished (E), the level of intrusiveness is higher due to this further modification. Hence, a FOM_S equal to 4 and 5 has been assigned in case of the use of an IR camera respectively, without and with the surface varnishing.

The on-state voltage at a low current injection (J) method requires a sensing circuit able at measuring a voltage variation during the switching on-off of the device. Furthermore, an additional active clamping circuit able at measuring a low voltage value. Hence, the auxiliary circuit and sensing circuits lead to intrusiveness comparable with the previous case, thus a FOM_S equal to 4 has been assigned. The threshold voltage (K) and gate emitter turn off voltage (N) CM methods require a low current generator for the calibration step. For example, considering an IGBT device, the gate and the collector terminals are shorted and then, the collector-emitter voltage drop is measured through a voltmeter. Hence, the gate driver has to be modified in order to perform the measurement. According to this, the FOM_S related to the system modification criterion has been set to 5. Similar reasoning can be carried out in case of the voltage-current change rate TSEP CM method.

The measurement of the JT in case of the on-state voltage at high injected current (L) CM method requires a high DC pulsed current source that feeds the DUT by using sever-

al switches and a voltmeter measures the voltage drop of the device. Furthermore, this CM method does not have high accuracy for the JT measurement, and hence, sophisticated and cumbersome sensing circuits are usually employed. Therefore, the aforementioned method shows a higher level of intrusiveness in the overall system and hence, FOM_S has been set to 7. Similarly, the saturation current (M) CM method requires a DC source and a switch that can inject into the DUT a current pulse width of hundreds of microseconds. Furthermore, the JT monitoring can be carried out by using an auxiliary circuit that is able to detect the saturation current of the device. The FOM_S has been set equal to the previous CM method since it involves similar modifications in the system.

It is worth underlining that the CM method based on the optical fiber (A) and the acoustic (F) methods are the most intrusiveness ones. In detail, the first method requires an advanced sensing circuit and a data acquisition station is usually employed. The data acquisition station generally consists of a PC server, several ADC converters, and a dedicated power supply system. It is worth noting that the data acquisition station may result in bulky and the integration with the preexisting applications is not easy. Likewise, the acoustic CM method uses an acoustic spectrometer that requires a specific circuit sensing that may be bulky to be easily integrated into the converter system. Furthermore, the chassis of the system has to be removed to place the acoustic spectrometer in the proximity of the power device. Thus the FOM_S has been set to 8 for these methods.

Figure 4:12 summarizes the FOM_S value for each CM method for the System modification criterion.

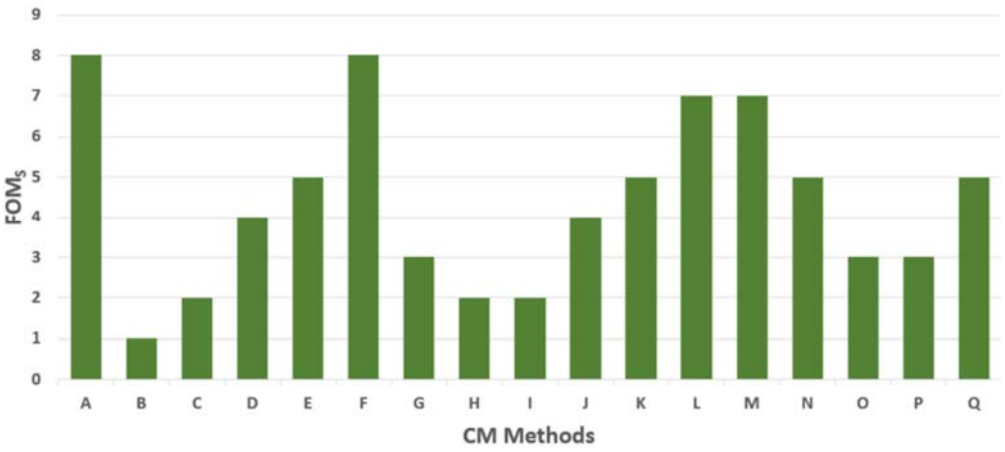


Figure 4:12 FOM_S assigned to the CM methods.

4.3.3 Figures of Merit (FOMs)

The adoption of a unique FOM representing the general level of intrusiveness of a CM is highly desired. It is important to underline that the FOM must be able to give a qualitative evaluation of the overall intrusiveness among the CM methods and therefore, to have a fast and practicable impact of intrusiveness. Such a general FOM can be obtained by properly combining the previous levels of intrusiveness, being each of them computed for a given criterion.

In the following, an overall FOM (FOM_O) that provides a numerical evaluation of the intrusiveness level for each CM method has been proposed. However, the aforementioned FOM provides a single value accounting for the three intrusiveness criteria, and hence, it may suffer from the biased marks proposed to compare the CM methods. In this perspective, an alternative strategy to estimate the level of intrusiveness of the CM methods has been based on the Pareto optimality [217].

4.3.3.1 Overall and application-based Figures of Merit.

An overall FOM, FOM_O assigned to a specific CM method, m, has been defined as the product of the three levels of intrusiveness FOM_D, FOM_C, and FOM_S. In detail:

$$FOM_O(m) = FOM_D(m) * FOM_C(m) * FOM_S(m) \tag{108}$$

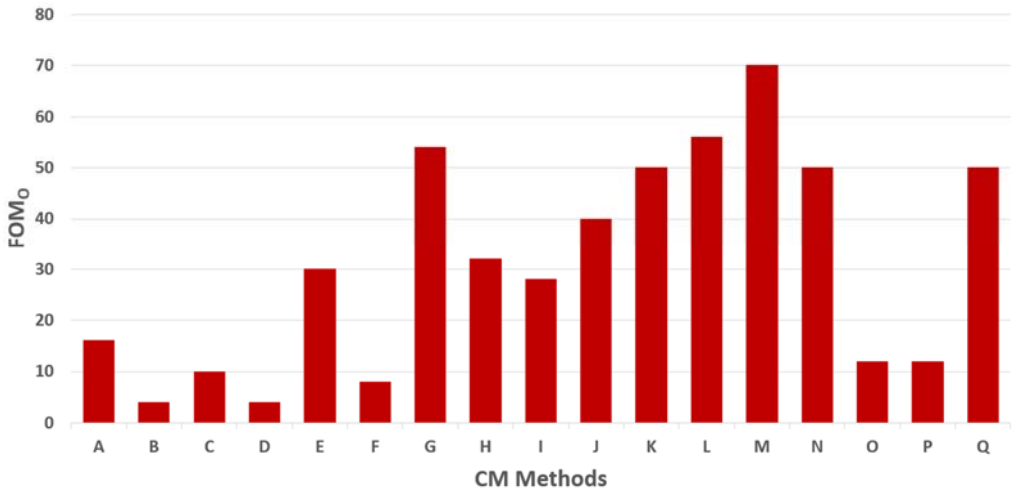


Figure 4:13 FOM_O assigned to the CM methods.

Figure 4:13 depicts the value of the FOM_O computed for each CM methods. The most invasive CM method results the TSEP - Saturation current (M). It is worth remembering that the monitor of the JT can be carried out only by switching off the power converter and furthermore, it requires the use of a DC source and a switch that controls the injection of a current pulse width of hundreds of microseconds into the DUT. Also, the JT monitoring can be estimated by using an auxiliary circuit that must be able to detect accurately the saturation current of the device. In this perspective, the high values both of FOM_C and FOM_S lead to an increase in the overall intrusiveness.

Other TSEPs CM methods, such as the On-state voltage under low and high current injection (J and L), Gate threshold voltage (K), Gate turn OFF voltage (N), and Voltage-Current change rate (Q) show also a high level of intrusiveness. These CM methods need to switch off the power converter and consequentially the FOM_C has been set to the maximum value. Furthermore, the FOM_S also has been set at a higher value, because it is usually used cumbersome equipment to measure the JT variation. Among the TSEPs CM methods, the Peak gate current (P) and Turn on-off delay time (O) shows a lower value of intrusiveness with respect to the aforementioned methods. More specifically, both CM methods are able to measure the JT without any converter shut off, and hence, the FOM_C does not impact the overall intrusiveness level. It is worth noting that the Physical CM method (G) shows a higher level of intrusiveness due to the high value of FOM_D, where the device package must be open in order to place the thermocouples.

The less intrusive CM methods are the ones using the integrated photodiode (B) and IR camera (D) according to the FOM_O. More specifically, the use of an integrated photodiode does not introduce a significant device modification, and the JT can be estimated during the online converter operations. Furthermore, system modification is negligible, because the key point of this CM method consists of the measurement of the voltage drop across the integrated photodiode. Similarly, the IR camera is able to measure the temperature of the DUT without any contact with the system. The FOM_S is the highest contribution due to the need to remove the chassis on the application. The Acoustic CM method (F) also shows a low value of overall intrusiveness. In this case, the device modification is negligible and the SOH can be carried out during the online converter operations. The major contribution that increases the level of intrusiveness is due to system modification, where the acoustic spectrometer is usually cumbersome and it is not easily integrated into a preexistent power application.

Finally, it has been defined as invasiveness FOM f_a, which is application related. More specifically, the FOM takes into account all the intrusiveness criteria, but the importance of each of them in the specific application is considered. For a given CM method (m) and a specific application (a), the FOM is computed as follows:

$$f_a = w_{a,1} \cdot FOM_D(m) + w_{a,2} \cdot FOM_C(m) + w_{a,3} \cdot FOM_S(m) \tag{109}$$

where $w_{a,1}$, $w_{a,2}$, and $w_{a,3}$ are weights that strictly depend on the specific application and their sum is equal to 1. For example, in a wind farm, the on-line CM is fundamental. Therefore, in such an application, $w_{a,2}$ is set close to 1 while the others are nearly 0.

4.3.3.2 Intrusiveness comparison based on the Pareto optimality

As said before, although the assignment of the marks is subjective since it is based on my personal opinion, the rank of the CM methods according to an intrusiveness criterion is almost unbiased. Therefore, the previous overall FOM, which provides a single value accounting for the three intrusiveness criteria could suffer biased marks when they are adopted to compare the CM methods. A strategy to compare the methods according to the rank instead of the mark is then important. With this in mind, the Pareto optimality [217] reasoning has been adopted as described in the following.

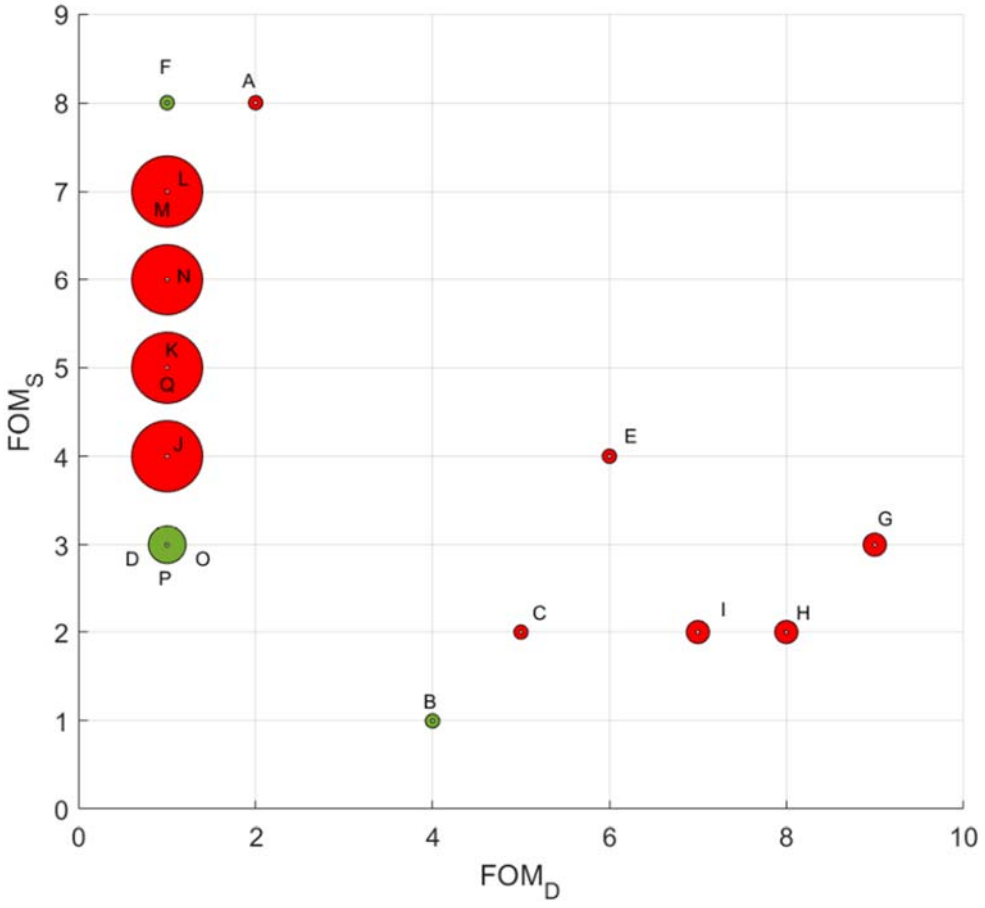


Figure 4:14 *FOM_D Vs FOM_S* represents the center of the circle, while the circle radius is set proportionally to *FOM_C*

Figure 4:14 reports a rough classification based on a simple visual inspection that aims to concurrently compare the CM methods in terms of the three intrusiveness criteria. More specifically, each method has been represented by a circle in the figure. The cou-

ple of values FOM_D-FOM_S represent the center of the circle, while the circle radius is set proportionally to FOM_C. More specifically, whether a CM method is placed on the left, it is better than one in the right, in terms of intrusiveness with respect to the FOM_D (x-axis). But the former is worse in terms of FOM_S (y-axis) if it is placed over the latter, otherwise the former present lower intrusiveness with respect to both criteria. On the other hand, the last condition does not imply that the former is better than the other at all since the FOM_C (circle radius) must be also considered. To formalize the comparison, some concepts are borrowed from the Pareto efficiency analysis. A CM method, Ψ, is said optimum, according to the Pareto optimality when [217]:

$$\begin{gathered} \nexists\, m \in \{A, B, \dots Q\} : \\ FOM_D(\Psi) \geq FOM_D(m) \\ FOM_C(\Psi) \geq FOM_C(m) \\ FOM_S(\Psi) \geq FOM_S(m) \end{gathered} \tag{110}$$

In other words, Ψ is said optimum when there is not any CM method better of it. The green circles represent all the optimum CM methods, that is the methods satisfying (15), while the red circles represent the others. It this perspective, all the CM methods that have been represented with a green circle belong to the Pareto front.

Figure 4:14 highlights that Acoustic (F), On state voltage at high current injection (L), Saturation current (M), Gate emitter voltage turn off (N), Voltage current change rate (Q), the Threshold voltage (K), On state voltage at low current injection (J), Turn off delay time (O), IR camera (D) and Peak gate current (P) have the same level of intrusiveness in terms of FOM_D. On the other hand, the methods L, M, N, Q, K, and J are worse than the method O (which is equivalent to D and P) in terms of both the two other criteria. Consequently, L, M, N, Q, K, and J are not optima (red circles). The lowest index of intrusiveness in terms of converter operation criterion (FOM_C) (it is depicted as a smaller radius of the circle) has been assigned to method F. Therefore, the CM method F is better than O from this criterion point of view, although it has a higher value of intrusiveness in terms of the system modification criterion (greater FOM_S). Therefore, both O, D, P, and F belong to the Pareto front and, consequentially, they are optimum in terms of intrusiveness according to the definition in (15).

The circle related to the CM method A presents the same radius of the one representing F, and it is located at the same height, that the same FOM_C and FOM_S values have been assigned to them, but A is not optimum since present a worse value of FOM_D.

The remaining CM methods such as the ones based on the external photodiode (C), the IR camera print (E), the TTCs-diode (I), the TTCs-NTC (H), and the Thermocouple (G) are located in the upper right of the CM method based on the integrated photodiode (B). Moreover, none of them presents a lower FOM_C (i.e. lower radius) than B. Then, they are not optima (red). The circle related to method B is on the right of O and F (i.e. B is worse of them in terms of device intrusiveness). On the other hand, the CM method B

presents the lowest intrusiveness in the conversion system (FOM_S). Therefore, B is an optimum CM method according to 15 (green circle), regardless of the fact it presents a negligible impact on the converter operation (FOM_C).

Chapter 5 Non-invasive SiC MOSFET Temperature Estimation Method based on the unintentional Light Emission from the Intrinsic Diode

5.1 Introduction

As evident from the analysis performed in the previous chapter, online junction temperature (T_j) monitoring has been widely studied in the literature [207],[218],[219]. The TSEPs methods are well-established solutions but they require an adequate calibration and decoupling procedure [220].

Other methods such as acoustic monitoring [117],[119] optical methods [132],[134],[136],[139], and so on guarantee a high accuracy, low complexity, and a fast transient response, without the aforementioned TSEPs drawback. Optical methods are common techniques but are rarely easy enough for the online temperature estimation.

The exploitation of the light emission phenomenon from the body diode of a SiC device may overcome these limitations. The electroluminescence phenomenon refers to the photoemission from a SiC material and it is related to its intrinsic body diode that operates in the third quadrant. The light brightness in the SiC intrinsic body diode depends on the junction temperature and on the forward current that flows into the diode. The light intensity decrease at high junction temperature being equal to the current injected. Thus, the electroluminescence phenomenon can be a suitable indicator of the temperature of the SiC MOSFET chip during a general power converter application.

As widely discussed in the previous chapter, the results of the comparison among various CM methods for power device has highlighted that the use of the Integrated photodiode is one of the best choices since it involves the lowest intrusiveness level. By considering the SiC MOSFET intrinsic diode as an unintentional diode, in this chapter, a new CM method adopting the Integrated photodiode in a SiC MOSFET module has been proposed.

In recent years, some works have already investigated methods for a non-intrusive and online junction temperature measurement based on the detection of the emitted light intensity by the intrinsic body diode [143-144],[221]. All these solutions use expensive sensing circuits, such as silicon photomultiplier and active circuit for biasing the photo-detector. This involves an increase in the complexity of the online temperature estimation system and the repeatability of the measurements is difficult. In this perspective, the proposed system presents an innovative method to characterize the junction temperature that overcomes the previous limitations. In detail, the gate-source voltage of the SiC MOSFET has been shorted and a pulsed current has been injected into the intrinsic body diode to emulate a potential third quadrant operation. The transient light emission has been acquired by using an inexpensive, simple, and effective passive sensing circuit, such as a commercial photodiode and a resistor connected in parallel. After that, the output voltage values of the photodiode at different temperatures and current pulses have been analyzed offline with the aim to obtain a dependence between the output voltage and the junction temperature. The average of the voltage values in two different time subinterval has been computed. Even if the solution is extremely simple, the proposed method highlights a good ability in the junction temperature estimation. The investigation provides a relation between the transient light emission with the junction temperature and the current magnitude. In the following, the proposed experimental setup has been widely described and several results have been shown.

5.2 Electroluminescence and prior art

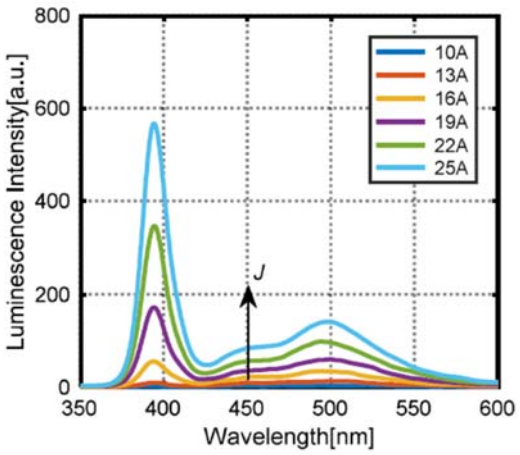


Figure 5:1 Luminescence intensity under different forward currents at 120 °C. (spectrum adopted from [221]).

In recent years, the electroluminescence phenomena related to the photoemission from a SiC material has been already used to characterize and monitor the state of the health of a commercial SiC MOSFET. More specifically, the electroluminescence phenomenon is

related to the intrinsic SiC body diode that operates in the bipolar conduction mode. There are three kinds of recombination processes in the low doped region: the direct band, Auger, and defect energy level states assisted recombination. The latter is related to the photon emission of the extra energy of the free carriers [222]. Bearing in mind the relationship between the peak wavelength λ related to the emitted photons and the bandgap energy E [223]:

$$\lambda = \frac{hc}{E} \tag{111}$$

where h is the Planck constant and c is the speed of light in a vacuum, it is possible to evaluate the peak wavelength of the emitted light for a 4H-SiC material. The peak wavelength is around 380 nm, which is the visible wavelength range of the blue light. Figure 5:1 shows the spectrum of generated light and the luminescence intensity under different forward currents at 120 °C for a 4H-SiC MOSFET [221].

As widely studied in the literature, the light color emitted by the SiC intrinsic body diode depends on the junction temperature T_j, which affects the wavelength, since the generated light is the result of the radiative recombination process [142], [221]. Moreover, the brightness depends on the magnitude of the forward current that flows into the diode[224-225]. It is worth noting that the light intensity decreases at higher T_j at the same current.

In many practical applications, the intrinsic SiC body diode may be used instead of the antiparallel SiC Schottky barrier diode, by providing a cost-effectiveness solution without sacrificing the conversion efficiency [226]. Thus, the aforementioned electroluminescence phenomenon can be a suitable indicator of the temperature of the SiC MOSFET chip in a generic power converter application. Only a few works in literature have been already focusing on this topic. The authors in [221] have proposed an online T_j estimations by measuring the light brightness of a SiC intrinsic body diode in a power module during the PWM inverter operations. This method has a low sensitivity and the measure of the light intensity requires an injected pulsed current with a large time width of about 15 ms, which is higher than the switching period in actual power converter applications. Furthermore, the method requires an active circuit sensing that may be bulky and consequentially, the monitoring system cannot be integrated easily in the device package. In [144] the temperature-dependent changes in the spectrum of the light emission of a SiC intrinsic body diode have been also studied. The approach has been validated by means of static characterization and dynamic measurements. Although the approach shows good sensitivity and it is able to detect the light variation in case of a pulsed current of about 1μs, the experimental setup is extremely expensive (two Silicon Photomultiplier photon detectors) and it is too bulky to be integrated inside the package of the device for an online T_j measurement.

5.3 Experimental setup

A schematic of the experimental setup is depicted in Figure 5:2. The passive sensing circuit consists of a photodiode from Vishay [227] and a resistor R_s of 500 kΩ connected in parallel (yellow block in Figure 5:2).

The main features of the photodiode have been summarized in Table 5:1. It can operate both in photovoltaic or photoconductive mode. The latter has a higher dark current that varies directly with the photodiode temperature. In other words, the measurement performed by the photodiode in photovoltaic mode is less sensitive to the temperature of the photodiode itself, thus enabling the repeatability of the measurement of the SiC device. Therefore, the photovoltaic mode has been chosen to obtain unbiased operations for ultra-low light level applications.

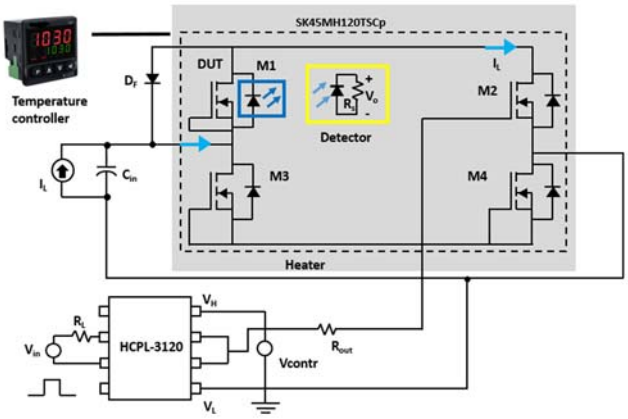


Figure 5:2 Experimental setup schematic.

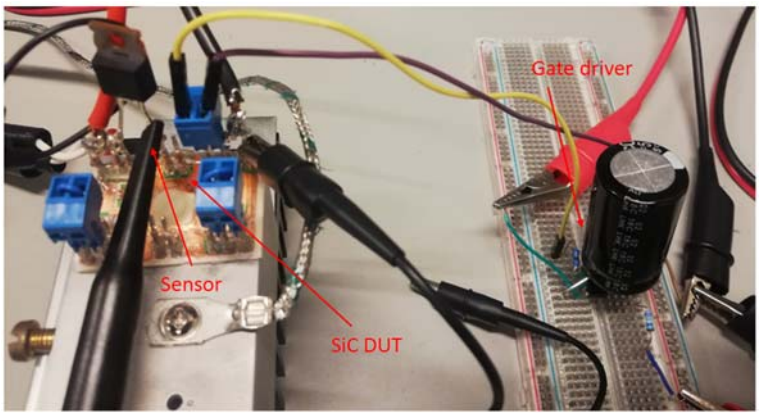


Figure 5:3 Picture of the experimental setup.

Table 5:1 Main features of the Silicon PIN photodiode at 25°C.

Parameters	Value
Reverse dark current	0.123 nA
Range of spectral bandwidth	430 to 1100 nm
Noise equivalent power	400 pW/√Hz

Table 5:2 Main features of the power module at 25°C.

	Parameters	Value
MOSFET	Breakdown Voltage	1200 V
	On resistance	56 mΩ
	Drain Current	40 A
BODY DIODE	Forward Voltage	6.4 V
	Forward Resistance	50 mΩ
	Maximum forward current	160 A (PW≤10µs)

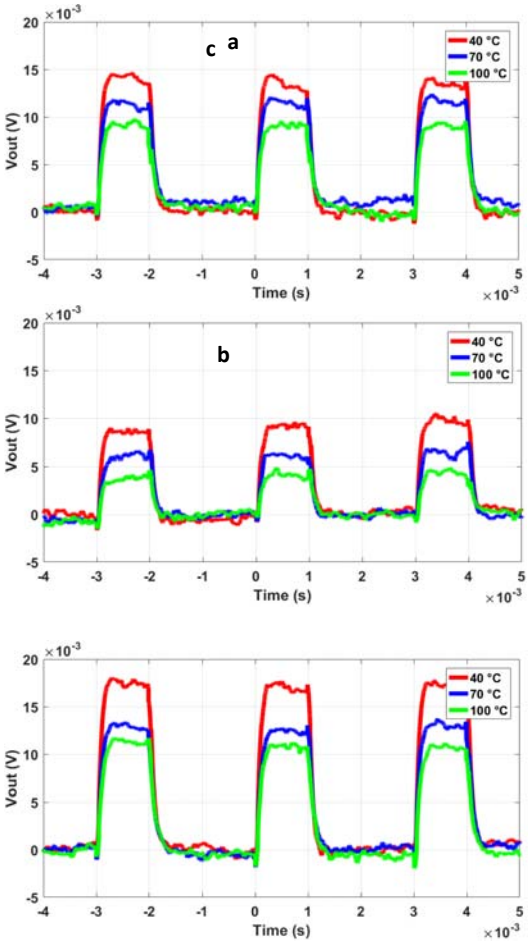


Figure 5:4 Photodiode voltage output at different T_j and different diode forward current values: (a) I_L =4,5A (b) I_L=7,5 A (c) I_L = 11,5 A.

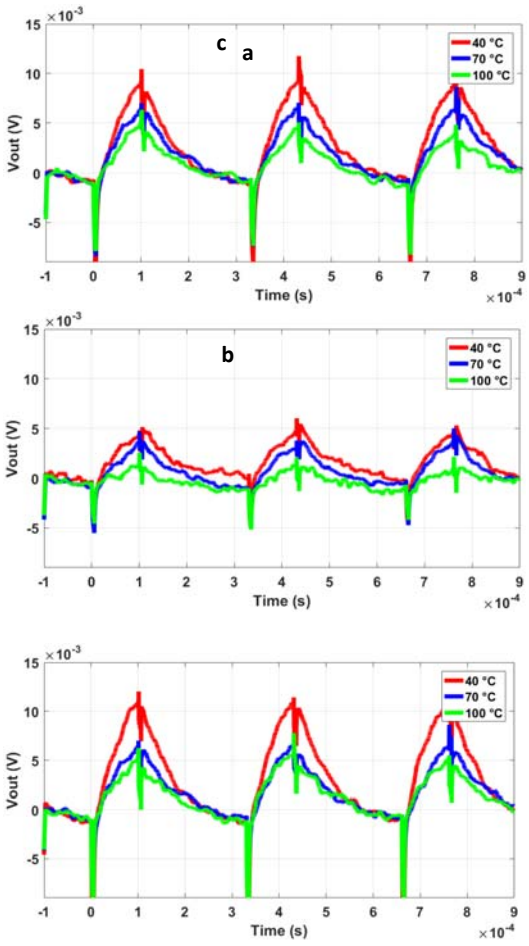


Figure 5:5 Photodiode voltage output at different T_j and different diode forward current values: (a) I_L =4,5A (b) I_L=7,5 A (c) I_L = 11,5 A.

The photodiode absorbs photons and it generates a current proportional to the incident light that, in turn, depends on the SiC devices temperature. Therefore, the SiC devices temperature is translated into an output voltage (*Vo*).

A 1.2 kV/40 A power module from Semikron [228] (main feature in Table 5:2) has been used for the experimental characterization (black dashed block in Figure 5:2). M1 has been chosen as a device under test (DUT).

The gate and source terminals of M1 have been shorted and the source of M2 has been connected to the negative terminal of the DC source. Similarly, M3 and M4 are kept off by short-circuiting the gate to the source to avoid undesired turn on. A freewheeling diode D_F has been connected in parallel to the SiC MOSFET, M1.

The intrinsic body diode has been biased with a current pulse, I_L, by means of a DC source paralleled with a capacitor C_{in} (50 mF). The pulsed current has been controlled by the MOSFET M2 and the gate driver HCPL-3120 [229]229. The function generator produces a square voltage waveform, V_{in}, with a constant period and duty cycle equal to one-third. The gate output control voltage, V_{contr}, is equal to 15V, and it is in series with a resistor R_{out} (10 Ω).

Figure 5:3 displays the experimental setup. The module top lid has been removed and the photodiode has been placed approximately 2 mm over the SiC MOSFET chip to detect the light emission. There is no voltage limitation to the application because the photodiode is not in contact with the SiC MOSFET.

It is worth noting that the measurements of the light brightness have been carried out without removing the metallization in place in the power module. Furthermore, the measurements have been obtained without removing the dielectric gel between the die and the photodiode sensor. Further research would be interesting to deepen whether the use of the dielectric gel can affect the light brightness measurements.

The SiC module has been placed on a temperature-controlled hot plate. For the sake of simplicity, the measurements have been done right after powering up, so that it has been reasonable to assume that T_j is equal to the plate one.

5.4 Experimental results

Figure 5:4 and Figure 5:5 depict the transient waveforms of the sensing output voltage V_O for three different current amplitudes I_L (4.5 A, 7.5 A, and 11.5 A) at three different case temperatures (40 °C, 70°C and 100°C) by using a pulsed injected current at 333Hz and 3 kHz, respectively.

From the experimental evidence, the measurements confirm that the light output strictly depends on the combination of the current magnitude I_L and T_j. More specifically, the voltage output, V_O, decreases for increasing temperature and it increases at higher current injections.

The measured voltage V_O fluctuates and it is not constant for each temperature measurement. This is more evident in the case of the highest frequency. The problem is due to the simple and extremely inexpensive sensing circuit that has been employed for the measurement, where no active filters or EMI shielding have been used for the light brightness measurements. Moreover, the commercial photodiode used in the experimental setup has an intrinsic time constant in the range of tens of microseconds, which is not enough for switching frequencies higher than 10 kHz. It is worth to underline that the V_O value is in the range of tens of mV.

Figure 5:4 shows the results in the case of a 333 Hz pulsed current with an on-time (T_{on}) of 1 millisecond, whereas Figure 5:5 shows the results in the case of 3 kHz, T_{on} = 100 microsecond. It is worth noting that in some cases, linearity is very low and some overlaps appear.

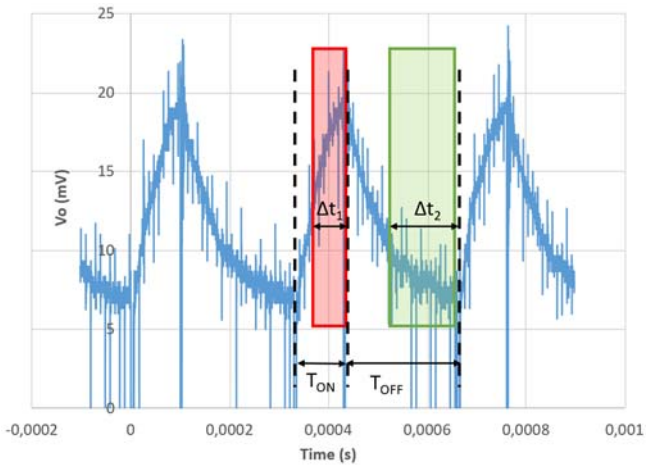


Figure 5:6 Experimental photodiode voltage output at T_j =40 °C with a I_L = 11,5 A at 3 kHz. Both the subinterval Δt_1 and Δt_2 represent the last 30% of the T_{on} and T_{off} time.

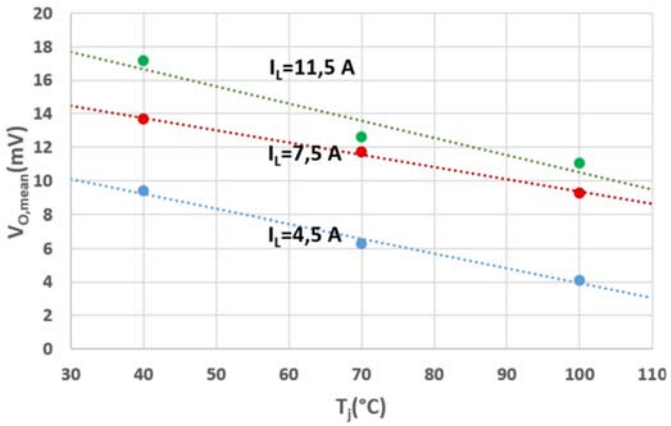


Figure 5:7 Dependence of V_{OM} with T_j and I_L at 333 Hz.

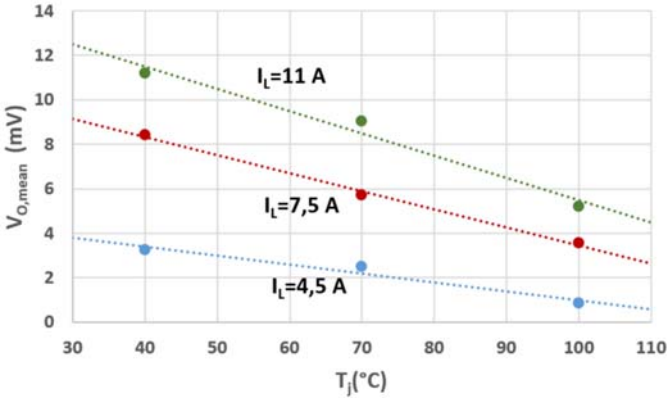


Figure 5:8 Dependence of V_{OM} with T_j and I_L at 3 kHz.

For instance, Figure 5:5(c) shows that the waveforms at 100°C (green trace) partially overlaps the one at 70°C (blue trace).

Notwithstanding the aforementioned limitations, the proposed strategy always makes able to distinguish fairly easily the temperature variations in a SiC power module in case of a pulsed current until 10 kHz. The simple key idea is to consider the average of the voltage values of the output voltage V_O during a portion of the T_{on} (i.e. Δt_1 of Figure 5:6) and T_{off} (i.e. Δt_2 of Figure 5:6). As depicted in Figure 5:6, both the subintervals Δt_1 and Δt_2 are measured at the last 30% of the T_{on} and T_{off} periods. We have calculated the average value of V_O during Δt_1, named V_{OH} (red box of Figure 5:6) and Δt_2, named V_{OL} (the green box of Figure 5:6).

The difference between V_{OH} and V_{OL} has been calculated and averaged out for fifteen consecutive time periods as follows:

$$V_{O,mean} = \frac{\sum_{i=1}^{15}\left(V_{OH,i} - V_{OL,i}\right)}{15} \tag{112}$$

Table 5:3 Coefficients of the polynomial functions Equation (113)

Current I_L [A]	T_{on} = 1 ms (333 kHz)		T_{on} = 100 µs (3 kHz)	
	α [mV/°C]	β [mV]	α [mV/°C]	β [mV]
4.5	-0.09	12.75	-0.04	5.01
7.5	-0.07	16.64	-0.09	11.61
11.5	-0.10	20.77	-0.10	15.47

Table 5:4 Coefficients of the polynomial functions Equation (114)

Current I_L [A]	T_{on} = 1 ms (333 kHz)	T_{on} = 100 µs (3 kHz)
4.5	± 4.6 °C	± 10 °C
7.5	± 5.5 °C	± 5.04 °C
11.5	± 3.9 °C	± 4 °C

Such a quantity has been used as an indicator of the device temperature. This approach has turned out to be extremely effective, especially, in the case of a measure at higher frequencies.

The dependence of V_{OM} on T_j and I_L, both for 333 Hz and 3 kHz and for different currents has been reported in Figure 5:7 and Figure 5:8, where the vertical axis is $V_{O,mean}$ and the horizontal one is T_j. Fitting lines have been added to the figures.

Since V_{OM} varies linearly with T_j, $V_{O,mean}$ can be estimated by means of a linear interpolation of the measured quantities (dashed lines in Figure 5:7 and Figure 5:8). Hence, the $V_{O,est}$ can be written as:

$$V_{O,est}(T_j) = \alpha T_j + \beta \tag{113}$$

where the term α is the slope and β is the intercept of the function. Table 5:3 summarizes the coefficients of the polynomial functions for each test set. Rearranging eq. (113) in terms of T_j yields an estimate $T_{j,est}$ of junction temperature as a function of $V_{O,est}$:

$$T_{j,est}(V_{O,est}) = \frac{V_{O,est} - \beta}{\alpha} \tag{114}$$

The proposed method can be integrated into a power module for the T_j monitoring during real operations. In detail, the evaluation of $V_{O,mean}$ at a known current enables the estimation of T_j by using (114).

Furthermore, the measuring system is very promising with respect to the measurement uncertainty, where the oscilloscope has a sensitivity of 1 mV and the photodiode has an uncertainty of about 20%, based on the datasheet. More specifically, the measurement uncertainty of the T_j has been calculated by referring (114), where it has been considered the ratio between the uncertainty of the voltage terms, $V_{O,est,}$ and β, respect the uncertainty of the slope α. Table 5:4 shows the calculated uncertainties at different currents and frequencies. It is worth noting that the uncertainty related to the $T_{j,est}$ decreases at increasing currents. The worst-case accuracy occurs at 3 kHz and 4.5 A, showing a reasonable uncertainty of ±10°C.

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