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Discrete and integrated circuits and systems for interfacing differential type capacitive sensors

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SUMMARY

In a reality where integrated and highly autonomous systems are adopted in any area of everyday life, great efforts are spent in the research and industrial environments so to design systems able to harvest energy from the environment around them and, in general, to maintain a very high efficiency level across all their possible working conditions. As a matter of fact, measurement subsystems (which are ubiquitous in any application field) play a significant role in this regard since, on one hand the transducer almost inevitably needs a power source to convert the measurand, and, on the other hand, being the electronic interface necessarily analog, it does not gain benefits, in terms of power consumption, from the simple technological scaling, as instead does the processing part of the complex system, typically digital. That said, on one hand it makes sense to use transducers which, by their nature, guarantee a very low power consumption and, on the other, it is worth carrying out research aimed at designing interfacing circuits that maximize readout performances avoiding spoiling the aforementioned constraints. In light of this, capacitive sensors have established in many applications, replacing the piezoresistive counterparts, since they consume virtually zero in terms of dissipated power, while not giving up in terms of robustness to temperature variations and sensitivity.

The doctoral dissertation proposed here, entitled "*Discrete and integrated circuits and systems for interfacing differential type capacitive sensors*", focuses on showing the state of the art and the development of new circuit and systems for the readout of differential capacitive sensors. Being a subset of the capacitive ones, this type of sensors has their same advantages while being inherently excellent at rejecting common mode disturbances.

The first chapter of the thesis is focused on an introduction to standard and differential capacitive sensors, characterizing them from a physical and electronic (circuit) point of view. The corresponding analytical parameterization of this type of sensor is also treated, based on the physical nature of the sensor, offering insights on the advantages and disadvantages of the various alternatives. The following chapter offers, instead, a review on the state of the art, both in terms of interface

architectures and in terms of building block used to implement them. In particular, this chapter is focused on the voltage mode approach. Indeed, there are several alternatives, among which the most common is represented by switched capacitor architectures whose operations, simplifying, depend on the status of a number of internal switches. By changing their status it is possible to perform a sequence of steps which eventually lead to the actual measurement. These interfaces, although effective, suffer from various relevant problems related to the non-ideality of the switches themselves (clock feedthrough and charge injection). In fact, there are "switchless" interfaces, typically based on oscillators, capable of adjusting the frequency (or duty cycle) of the output signal according to the value of the transducer. The limit of these proposals is linked, in particular, to the stability of the oscillator itself and to the almost inevitable mismatch between the passive components that constitute the circuit. Other alternatives are also analysed, comparing them between each other.

The third chapter introduces all the voltage mode readout techniques and circuits for interfacing differential capacitive sensors, derived from the research conducted during the three year doctorate. The innovation factor in this sense lies both in the methodology and in the design of ad hoc discrete and integrated architectures: after a brief introduction on the concepts of synchronous demodulation and self-balanced bridge, it is shown how these have been effectively used for the objectives listed above, and how, thanks to them, it is possible to overcome some limitations of the classic proposals. The designed circuits and the results coming from the simulations and the measurement of the same circuits are then shown, offering an in-depth comparison with the literature. In the second part of the same chapter, a possible methodology, translated into a circuit, to compensate capacitive parasitic elements, is also given. In particular, being it independent from the interface, it is shown how it has been retrofitted to the circuits developed along the chapter.

The fourth chapter gives an insight into the status of the art about current mode techniques to evaluate differential capacitance transducers. Unlike the voltage mode approach, the literature, in this topic, is rather standardized, in other words, all proposals are based on a well-defined theory. Although, indeed, encapsulating information in a current has numerous advantages over a purely voltage mode

signaling, making it possible to obtain extremely simple architectures, allowing high speed readings and high sensitivity values, at a very low power consumption, it has also crucial drawbacks. In fact, a current mode interface results extremely sensitive to the non-idealities of the sensor and of the electronics itself (parasitic capacitances and offset of the amplifiers). Moreover, the voltage across a capacitor, under the action of a constant reference current, tends to linearly increase, making it necessary for the designer to find a way to periodically discharge it. On these weaknesses, the research work elaborated in the following chapter is justified.

In the fifth chapter, we therefore propose a novel circuit developed for interfacing differential capacitive sensors with a current mode approach. The research in this direction has been twofold: on one hand we have developed an interface circuit which is capable of dynamically eliminate the effects of stray capacitances, on the other, for the first time, we have taken advantage of the benefits coming from a totally new building block, the second generation voltage conveyor (VCII). The theoretical analysis as well as all the measurements conducted on a prototype are shown in the chapter.

In the sixth and last chapter of this thesis we report our contributions on the topic of integrated active blocks that can be profitably employed as building elements for interface circuits and systems. In particular, in the first half of the chapter, after a short literature review, we propose two novel architectures to implement advanced second generation current conveyors (CCIIs). Similarly, in the second half of the chapter we propose many novel topologies to synthesize the aforementioned VCII. Each of the proposals is thoroughly analysed from a theoretical point of view. Simulation results are also given.

A short discussion summarizing the main achievements is given at the end of each paragraph.

ACKNOWLEDGEMENTS

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1 INTRODUCTION

The need of electronic devices able to *sense and manipulate* magnitudes of different nature, such as mechanical, chemical, hydraulic or electromagnetic, is nowadays ubiquitous. Indeed, may it be the driving of an industrial process, or the monitoring of biological parameters of a patient, or even a simple data collection of the health of civilian infrastructures, a device or system able to translate the magnitude of interest into a signal that is actually understandable by the end user, is obviously essential.

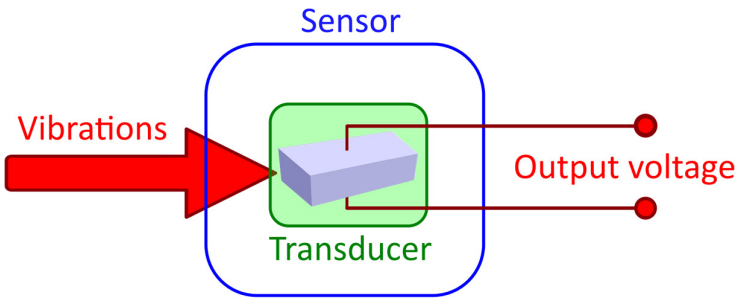
1.1 Sensors: a brief review

Generally speaking, the name given to devices able to detect real phenomena is "transducers". A transducer is a device capable of converting a magnitude, often called measurand, from an energy domain to another, which does not necessarily correspond to the electrical one. Signal processing, however, needs electrical inputs to be acquired, this means that the energy domain in which a "sensing" process always aims to is the electrical one.

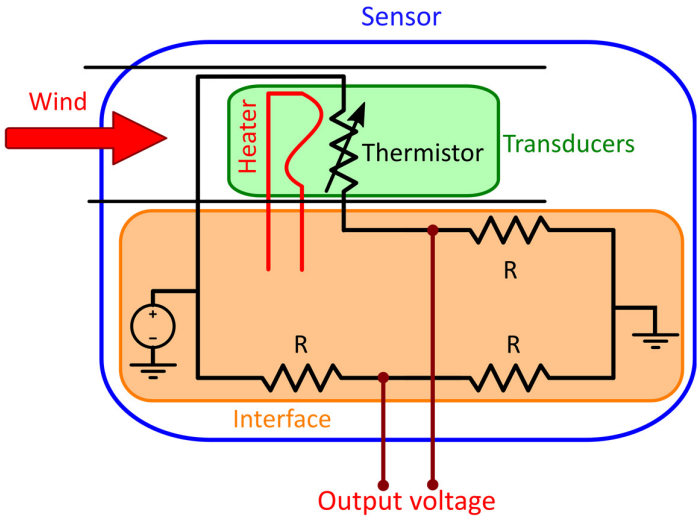
Devices or systems, which convert energy from a given domain to the electrical, are called "sensors". A sensor either can correspond to a single transducer (see Fig. 1.1a) or can be seen as a complex system made of multiple transducers, followed by an electronic circuit which carries out the final conversion (see Fig. 1.1b). For instance, a piezoelectric device is both a transducer and a sensor, since is capable of

converting vibrations into an electrical signal. On the other hand, a hot wire anemometer, like the name suggests, evaluates the wind speed by measuring how much a heater gets cooled down from a starting temperature. Therefore, the wind speed is converted into heat, which in turn varies a thermistor resistance whose changes are sent to an electronic readout interface (for example a Wheatstone bridge in Fig. 1b).

The final information coming from a sensor (or from a sensing system) can be of different nature. In fact, it can be fully analog, but also digital, ready to be processed by a microcontroller. In particular, in the latter case, analog-to-digital converters are required. Moreover, it is often necessary to equip the



a)



b)

Figure 1.1 a) single transducer sensor, b) multiple transducer plus interface sensor.

overall system with dual devices, i.e. digital-to-analog converters that supply one or more actuators, which carry out an inverse transduction, from an electrical domain to a non-electric one (the "actuator").

Capacitive sensors, in general, present important advantages over their counterparts such as resistive and piezoresistive sensors. Indeed, they show better sensitivity, temperature and drift performances and, most importantly, they consume virtually no power. Another noticeable advantage is that they can be micromachined together with the readout electronics over a silicon substrate (MEMS capacitive sensors), making them miniaturized without losing key features like sensitivity and resolution [1-4].

1.2 Capacitive sensors

1.2.1 Physical properties

An interesting aspect of a capacitor, from a sensing point of view, is that capacitance value is influenced by its geometrical and physical properties. Taking into consideration two parallel plates facing each other, which is the most used geometry due to its ease of fabrication, it is possible to define its capacitance as:

$$C = \varepsilon_0 \varepsilon_r \frac{S}{d} \tag{1.1}$$

where ε_0 and ε_r are the dielectric constants of the vacuum and of a specific medium respectively, S is the overlapping surface between the two electrodes and d is the distance between them (see Fig. 1.2). If an external magnitude is capable of modifying one of these parameters, a consequent variation in the capacitance value is experienced and, hence, can be read by a suitable electronic interface.

It is called '*spacing variation capacitive sensor*' a device (see Fig. 1.3a) where the variable magnitude is the distance between the two plates (Eq. 1.2). In this case, the space variation changes the value of the same capacitance according to the following relation:

$$C = \varepsilon_0 \varepsilon_r \frac{S}{(d + \Delta d)} \tag{1.2}$$

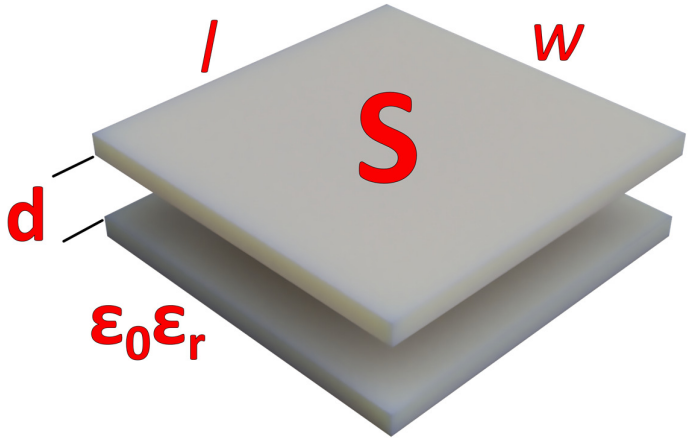


Figure 1.2 A parallel plates capacitive sensor configuration.

Since often one of the two plates is fixed, while the other is a vibrating conductive membrane, rather than the pure distance, the mean value of this magnitude across the entire plate area is given by:

$$C = \iint_{x,y} \varepsilon_0 \varepsilon_r \frac{1}{(d + \Delta d)} dxdy \tag{1.3}$$

Obviously, in Eq. 1.3 the magnitude Δd is a function of x and y. This configuration results to be very sensitive to the measurand since it acts on the smallest dimension of the sensor, so a reduced variation of distance can be reflected in a large variation of the capacitance. It is noticeable that variations of the capacitance with respect to the dimension d are nonlinear (Eq. 1.2); however, if the evaluated parameter is the impedance ($Z_C = 1/j\omega C$) the same relationship becomes linear:

$$Z_C = \frac{d + \Delta d}{j\omega \varepsilon_r \varepsilon_0 S} \tag{1.4}$$

Similarly, an '*overlapping area variation capacitive sensor*' relies on the modification of the common surface shared by the two electrodes (see Fig. 1.3b). An advantage of this approach with respect to the previous one is that capacitance variation is inherently linearly related to the surface variations. On the other hand, however, since plate dimensions are much larger than the gap between them, the sensitivity of this approach results lower if compared to the previous one (in other words, to produce the same amount of capacitance alteration, the measurand must

have a wider variation). Lastly, it is possible to take advantage of the dielectric constant of different mediums so to achieve a capacitance variation as shown in Fig. 1.3c. This specific scenario is often used to detect liquid or gas levels into a tank, or even to reveal the presence of a particular gas in an environment. Remarkably, these techniques can be used not only for linearly moving electrodes, but also to detect rotation and tilt angles. More complex structures (based on arrays of parallel plates capacitors) can act as multidimensional detectors, which means that they can simultaneously and independently sense more than one measurand variations.

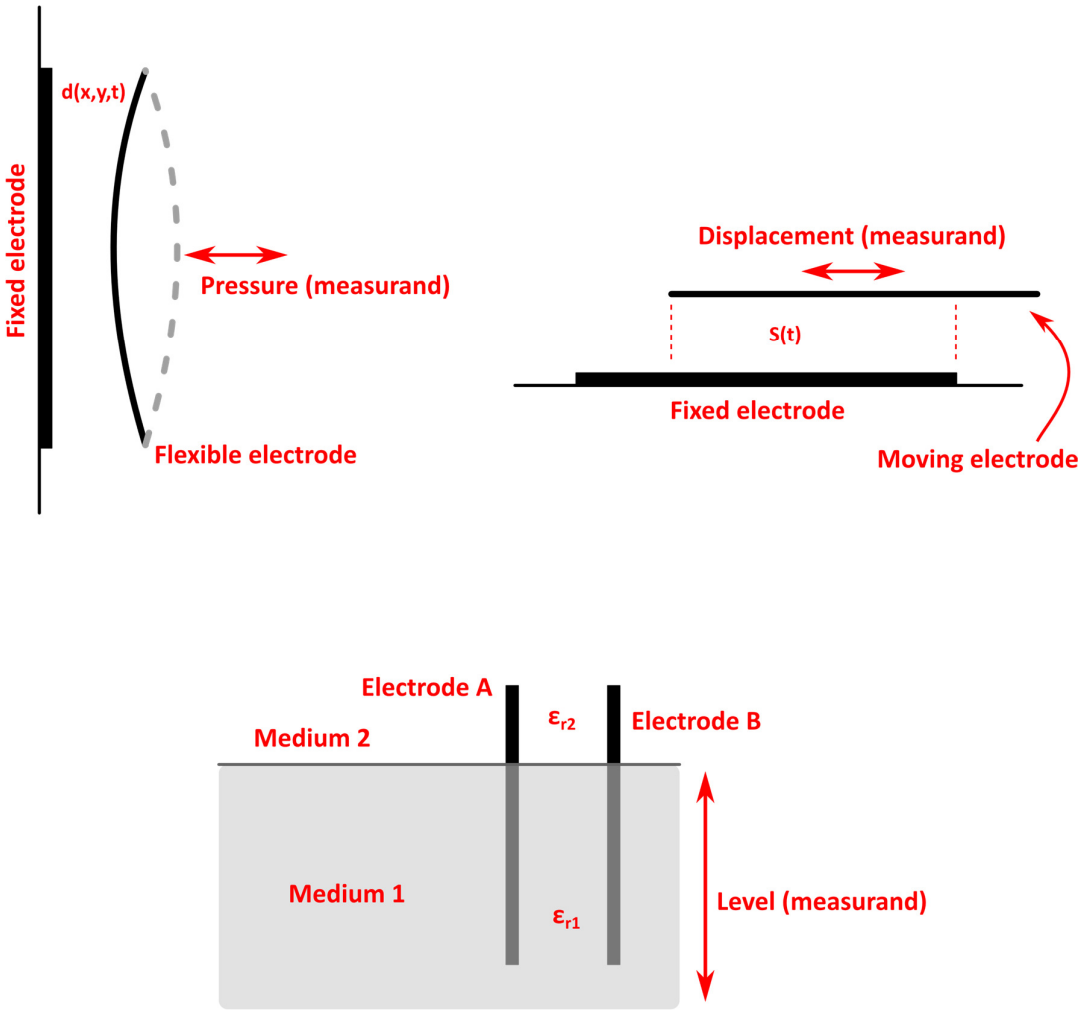


Figure 1.3 Three different use cases for a parallel plates capacitive sensor: a) distance variations; b) overlapping surface variations; c) dielectric constant variation.

1.2.2 Basic interfaces for capacitive sensors

Interface type and performances are strictly related to the designer needs and to the application. The main key points that determine the appropriate choice for the interface are the baseline of the sensor, how broadly it can vary, how much common mode disturbs can affect the measurement (environment), how parasitic capacitances of the interface are placed with respect to the sensor, how much power can be consumed by the circuitry and, in some cases, how much space the circuitry can occupy (or, in other words, how complex the interface is). Also, an accurate analysis of the application scenario is mandatory before designing the sensor interface [4].

The first and most simple method is based on a DC readout. A basic circuit is given in Fig. 1.4. The working principle is the following: the sensing capacitor is precharged to a reference voltage V_{ref}; then, by supposing that the signal varies with a frequency greater that $1/RC$, it is possible to consider the charge accumulated at the capacitor electrodes as a fixed value equal to:

$$q_{std} = C_{bl} V_{ref} \tag{1.5}$$

where C_{bl} is the value of the capacitor at the steady state (baseline). Then, by knowing that $C = Q/V$, it is possible to rewrite Eq. 1.5 as:

$$V_{out} = \frac{C_{bl} V_{ref}}{C_x} \tag{1.6}$$

where C_x represents the value of the sensing capacitor under the action of the measurand. Although very straightforward, this method lacks robustness with respect to circuital noise, works only for relatively fast capacitor variations and requires an extremely high impedance and low offset amplifying stage. Moreover, owing to the constraint on the time constant, it is not good for wide variations of the sensor from its baseline.

A solution that is particularly suitable for large variations from the baseline is the so-called capacitance to frequency (or period) conversion. The key point of this technique is the employment of the sensor in an oscillator configuration (even a

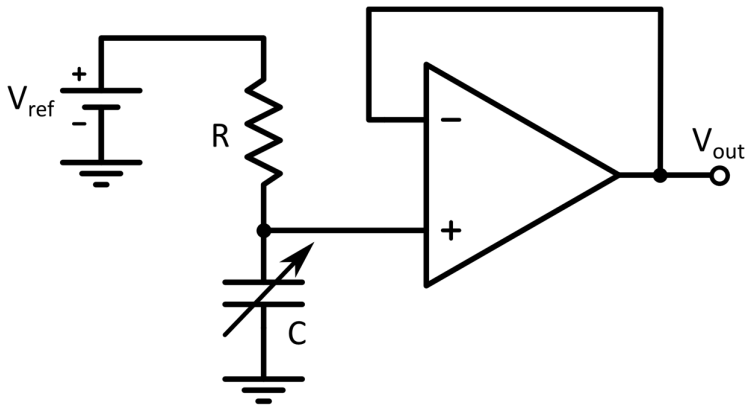


Figure 1.4 DC readout technique.

basic RC oscillator) and the tracking of its variations by measuring changes in the output frequency. Sometimes, rather than on the frequency, output variations are induced on the duty cycle of the signal. Fig. 1.5 depicts a simple astable oscillator where C_s represents the sensing capacitor. The relationship that links the frequency to the capacitor is the following:

$$f_{out} = \frac{1}{2R_3C_s \ln\left(1 + 2\frac{R_1}{R_2}\right)} \tag{1.7}$$

According to the oscillator nature (RC, LC and so forth) it is possible to reach different frequency ranges. As noticeable from Eq. 1.7, RC oscillators produce an output frequency that is proportional to 1/RC, whereas for LC oscillators, the output frequency is proportional to $1/\sqrt{LC}$, so the designer has to take into account the output non linearity.

This kind of readout technique has numerous advantages. One of the most noticeable is that they do not require knowing the capacitor baseline to perform the readout, this reflects in the possibility to achieve good measurements even if the sensor drifts with time.

Another benefit is that the output is intrinsically digital: measuring a time, for a microcontroller or a single board computer, does not require the presence of ADCs and hence reduces the system complexity and the conversion error.

On the other hand, drawbacks of oscillator-based interfaces are their sensitivity to stray capacitances and electronic mismatches, and their poor noise rejection. This can lead to accuracy errors and, in general, requires specific precaution at design

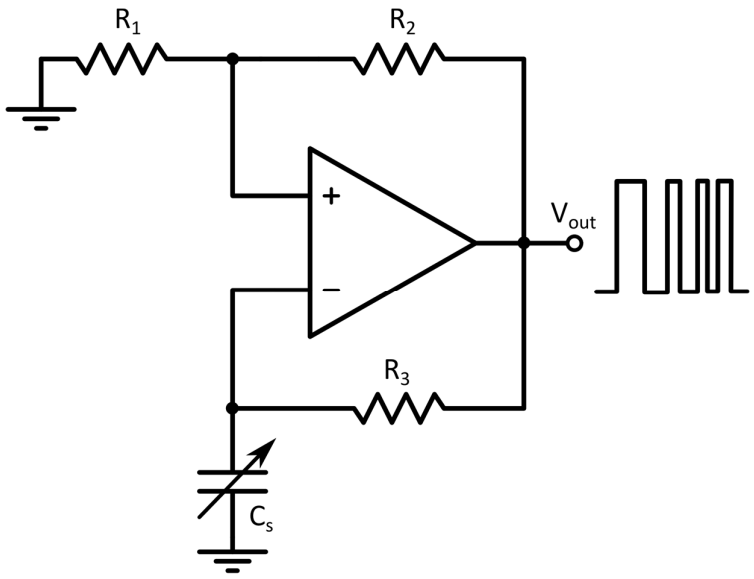


Figure 1.5 RC oscillator based readout interface.

stage, like inserting shielding lines and complicating the actual interface. Another critical aspect is that an oscillator based interface has typically a low sensitivity value, which makes it unsuitable for extremely low capacitance variations from the baseline value.

One of the best methods to detect very low measurand variations, maintaining high accuracy levels, is to make use of synchronous demodulation architectures. The basic idea here is to excite the sensor by a high frequency signal (typically a sinusoidal signal with a frequency greater than 10 kHz) and then, through suitable circuitry, to bring back the measurement output to the baseband through a demodulation stage. This process, although intricate at a first glance, has many benefits. First, exciting a capacitor with a sufficiently high frequency reduces its impedance. This allows to relax the high impedance requirements for the primary conversion stage, minimizing matching errors. Second, the presence of a low pass filter during the demodulation process allows to cut down higher frequencies noise. Third, being an AC excited technique, part of the parasitic capacitances are inherently nullified (this will be discussed deeper in the following).

A simple circuit that exploits the synchronous demodulation is given in Fig. 1.6. As visible, the sensor is coupled with a reference capacitor through a voltage divider. A simple non inverting buffer reads the voltage at the output of the divider and feeds it to a demodulator. It consists of a multiplier and a filter: the multiplier uses a

reference signal with the same frequency and phase respect to the buffer output (synchronous) to generate the DC output together with an unwanted high frequency signal, which is removed by the filter. An improved version of the same interface is shown in Fig. 1.7. Rather than relying on a simple voltage divider, it uses a bridge-based architecture to perform a fully differential measurement in order to improve the rejection to common mode disturbs increasing the resolution of the whole interface.

The best choice for the first stage is, in this case, an instrumentation amplifier (INA) since, unlike a simple Op-Amp, offers a suitably high impedance at both inputs while converting the signal to single-ended maintaining a controllable gain.

There are several techniques to use a bridge-based architecture with wide varying capacitive sensors. They will be analysed in the next chapters.

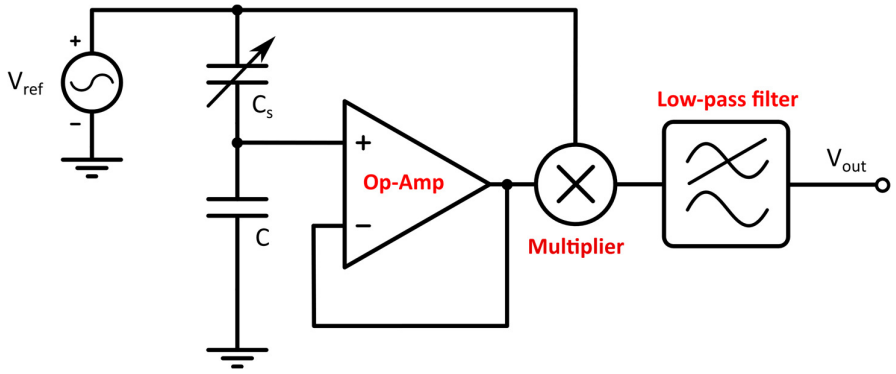


Figure 1.6 Single-ended synchronous demodulation technique applied to capacitive sensing

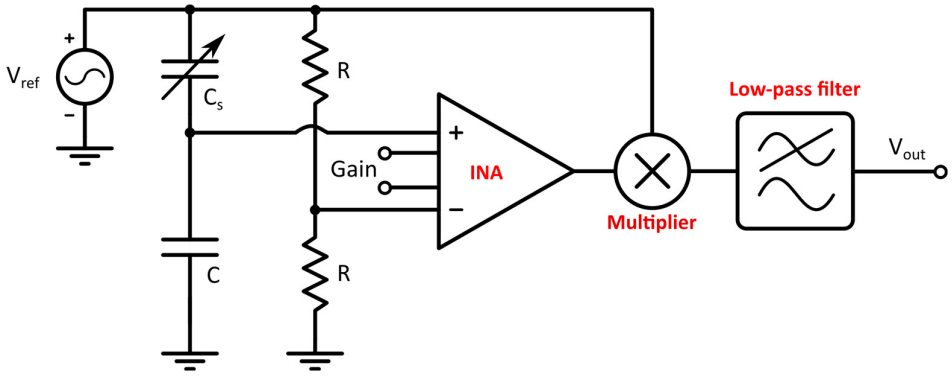


Figure 1.7 Fully differential synchronous demodulation technique.

1.3 Differential capacitive sensors

A differential capacitive sensor, depicted in Fig. 1.8, is an important subset of the capacitive sensors family. It is a three terminals device made of a couple of capacitors, C_1 and C_2, which share a common node (called D). The value of these two capacitors vary from a common baseline in a differential fashion under the action of the measurand. The main advantage of this behavior is that it allows to eliminate common mode disturbs from the readout process, thus increasing the overall sensitivity and resolution of the sensor, making them suitable in applications where low capacitive variations are induced by the measurand (such as measurement of acceleration, dielectric characteristics of a medium, angular velocity, displacement and so on [5-7]).

1.3.1 Physical properties

According to the physical behavior of a differential capacitive sensor in response to the measurand, it is possible to divide them into two main categories: linear sensors and hyperbolic sensors. Fig. 1.9 represents a linear differential capacitive sensor: as visible, it consists of three plates, two of them are fixed (the upper ones), while the third one (the bottom one) is free to move. When no external magnitude is applied, they lay at a certain distance d, sharing a certain amount of area S_0. These conditions define the baseline of the sensor, C_{bl}, which can be calculated according to Eq. 1.1. The action of the measurand here determines a differential change in the overlapping areas of the three plates.

Unlike the simple capacitive sensors, it is possible to define a range of variations for the sensor uniquely as follows:

$$\mathbf{0} < \boldsymbol{C_{1,2}} < \mathbf{2}\boldsymbol{C_{bl}} \qquad \textbf{(1.8)}$$

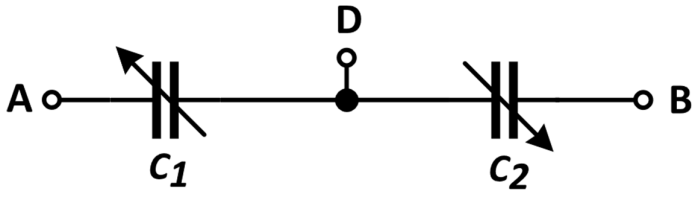


Figure 1.8 Ideal equivalent model for a differential capacitance sensor.

Fig. 1.10 represents a hyperbolic differential capacitive sensor. The baseline condition can be calculated with the same procedure utilized in the linear sensors. However, for this kind of sensors, the measurand acts on the distance between the three plates: the external ones are typically fixed, while the internal one is movable. As a consequence, the range in which a hyperbolic sensor varies can be estimated as:

$$\frac{C_{bl}}{2} < C_{1,2} < \infty \qquad (1.9)$$

Based on what analyzed so far, it is possible to make some considerations. As already pointed out in the previous paragraphs, a hyperbolic sensor tends to be more sensitive to the measurand respect to the linear counterpart due to the fact that, for any given displacement, the smallest dimension (d) is much more affected in terms of percentage variation that the largest one.

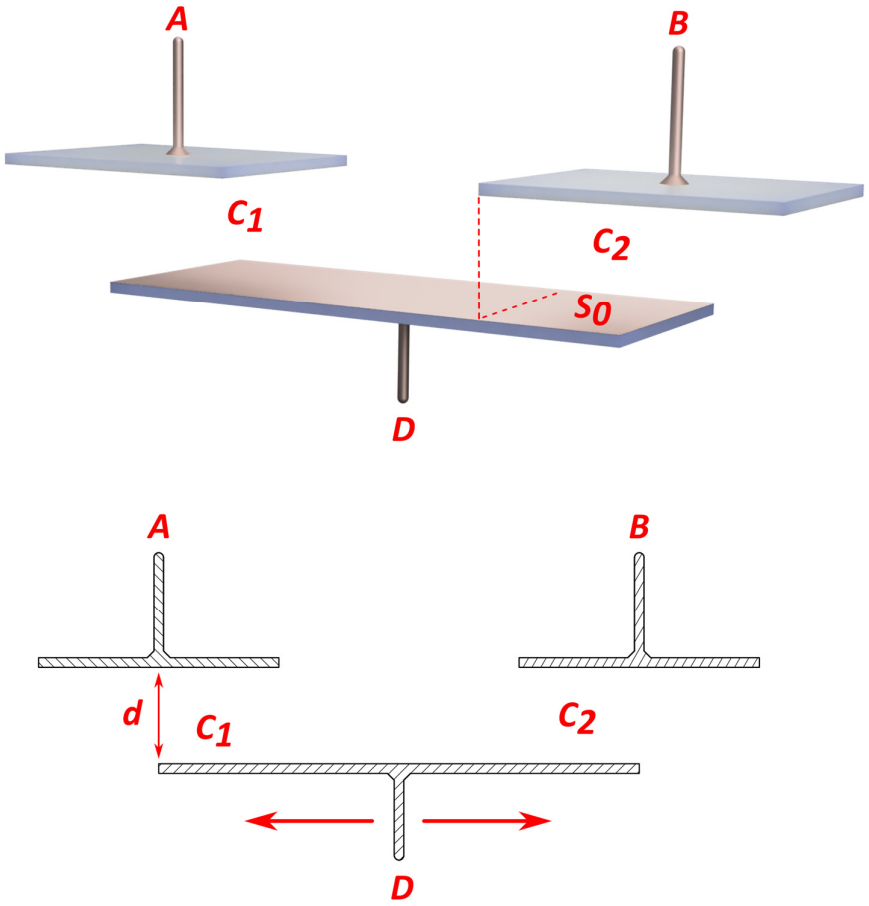


Figure 1.9 A linear differential capacitive sensor.

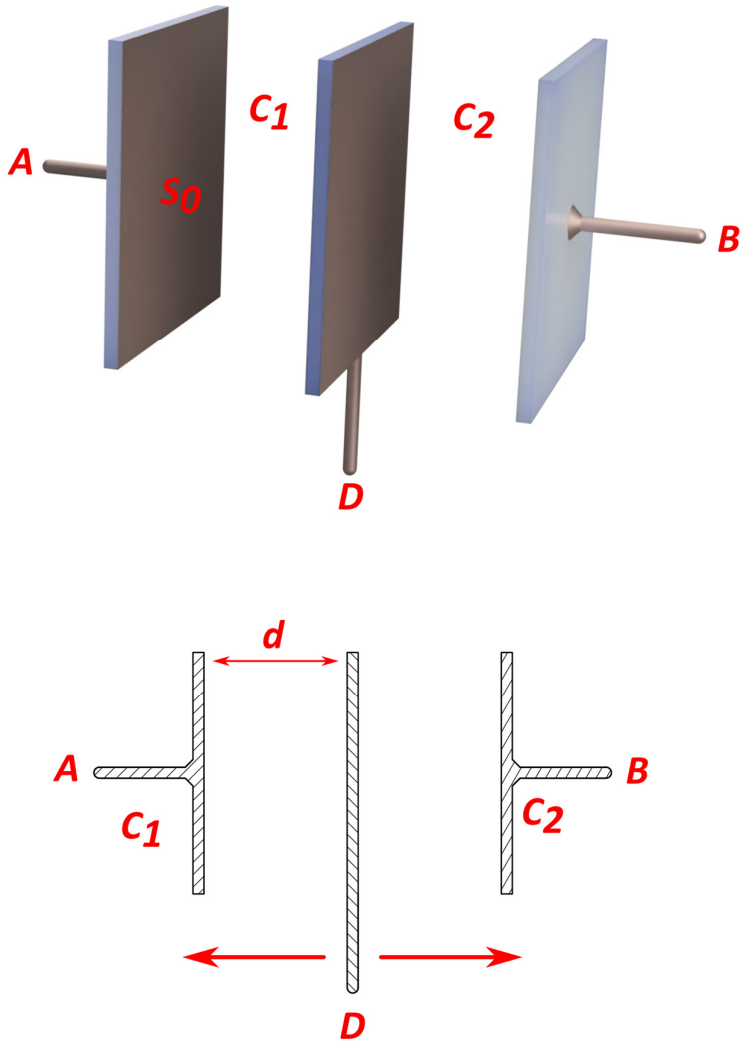


Figure 1.10 A hyperbolic differential capacitive sensor.

This makes a linear sensor more suitable for measurands with large variations.

Eq. 1.8 and Eq. 1.9 show the difference in the ranges that the two different options can assume. On one hand, linear sensors are easier to interface with, due to the finite variation span. On the other, however, the fact that one of the two capacitors can assume very low values, makes them more addicted to the effects of parasitic capacitors in some applications. For both of the options, the extreme boundary conditions cannot be reached because the differential capacitor would degenerate into a simple capacitor.

1.3.2 Parametrization

Regardless of the type of sensor, due to the intrinsic differential behavior, the evaluation of the measurand can be pursued by evaluating a dimensionless parameter *x*, which can be defined as the ratio between the difference of the two capacitors C_1 and C_2 of the sensor, and their sum:

$$x = \frac{C_1 - C_2}{C_1 + C_2} \tag{1.10}$$

In other words, *x* defines how much the sensor value has changed relatively to the baseline, therefore it is often expressed as a percentage. As easily noticeable, its variations are bounded between -1 and 1, values that, as visible from Eq. 1.8 and Eq. 1.9 can be never reached.

From an analytical perspective, it is therefore advantageous to parametrize the behavior of a differential capacitance sensor with respect to *x*. Eq. 1.11 shows how a linear sensor can be expressed as a function of *x*:

$$\begin{aligned} C_1 &= C_{bl}(1 + x) \\ C_2 &= C_{bl}(1 - x) \end{aligned} \tag{1.11}$$

The positive and negative sign are given to the *x* according to Fig. 1.11a. Similarly, Eq. 1.12 shows how a hyperbolic sensor can be parametrized:

$$\begin{aligned} C_1 &= C_{bl}\frac{1}{1 - x} \\ C_2 &= C_{bl}\frac{1}{1 + x} \end{aligned} \tag{1.12}$$

The positive and negative sign are given to the *x* according to Fig. 1.11b.

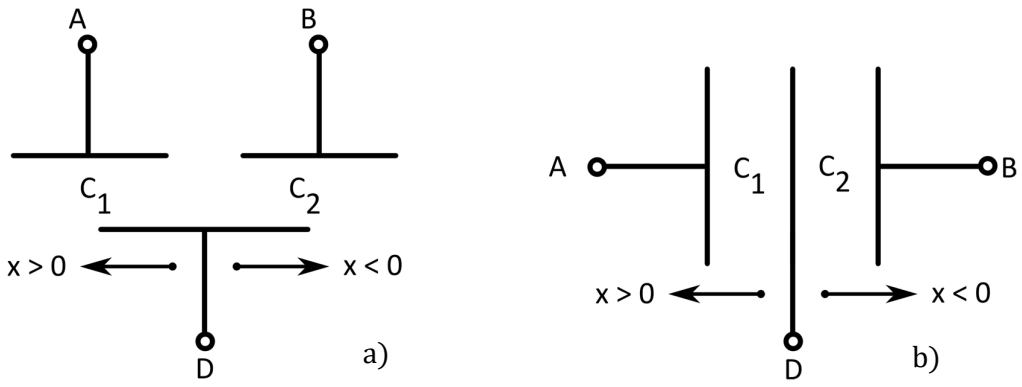


Figure 1.11 Definition of the sign of x according to the sensor type: a) linear; b) hyperbolic.

1.3.3 Basic interfaces for differential capacitive sensors

The basic solutions that have been given in section 1.2.2 for capacitive sensors can be applied to differential capacitance sensors as well. Fig. 1.12 represents two simple oscillators implementing a capacitance to time conversion.

We have two solutions, each of which is usable only with a specific type of sensor: the linear one (Fig. 1.12a) and the hyperbolic one (Fig. 1.12b). That is due to the intrinsic behavior of the sensor: for the linear one the parallel configuration would remain constant across all the measurand variations making the interface unsensitive to the measurand, while for the hyperbolic sensor, the series configuration would result in a constant output frequency regardless of the measurand.

This basic solution is unable to detect which one of the two capacitors has a greater value. In other words, it does not take advantage of the differential feature of the sensor.

On the contrary, synchronous demodulation configurations can benefit of a differential capacitance sensor. Fig. 1.13a and Fig. 1.13b show both the single-ended and the fully differential configurations, respectively. The presence of a differential capacitive sensor allows to obtain a better sensitivity and an improved resolution (due to the lower noise).

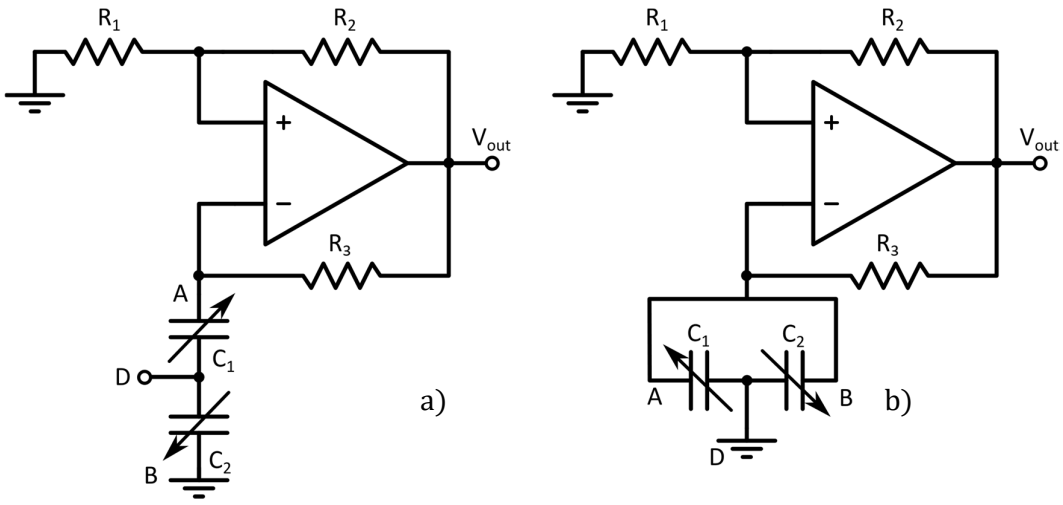


Figure 1.12 Oscillator based differential capacitive sensor interface a) for linear sensors; b) for hyperbolic sensors.

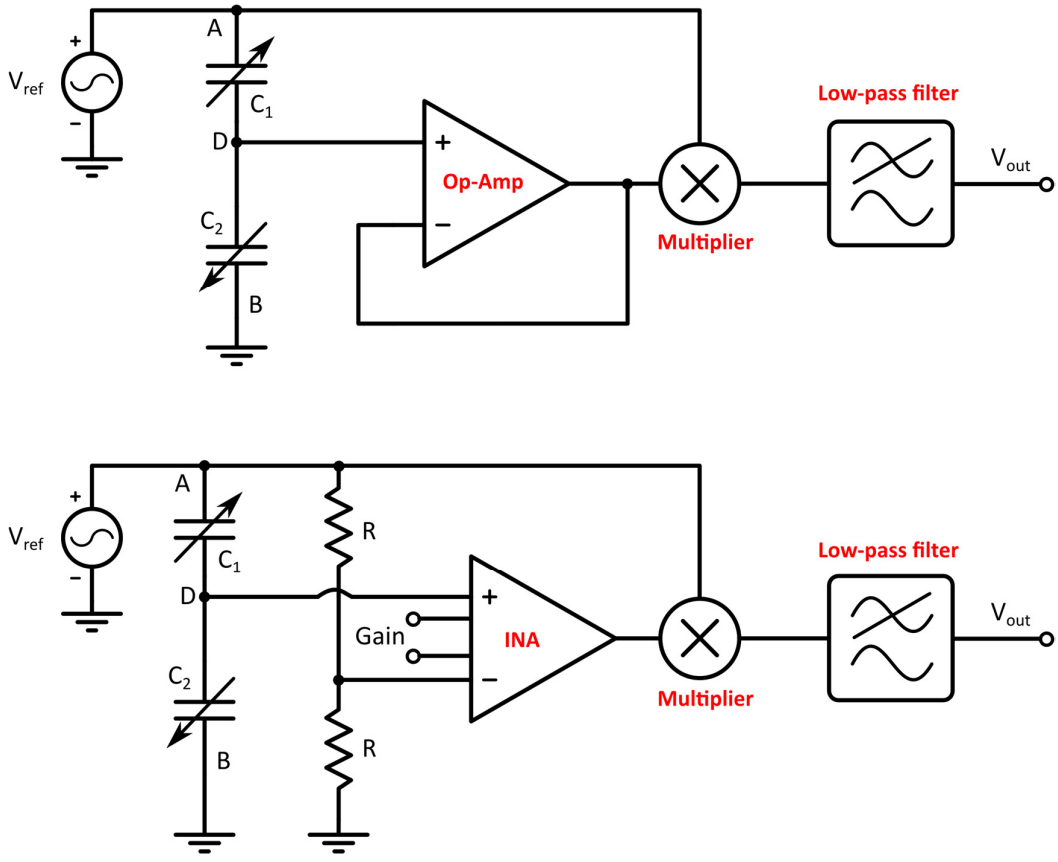


Figure 1.13 Differential capacitive sensors asynchronous demodulation readout: a) single-ended; b) fully differential.

1.3.4 Considerations on parasitic capacitances

One of the key points that, with the scaling of the technology, has become a necessity for obtaining an interface suitable for example, for evaluating MEMS behavior or, in general, very low baseline sensors, is its capability to deal with sensor parasitic impedances [8]. In fact, there are cases where stray capacitances are even greater than the actual sensor baseline. Fig. 1.14a shows the equivalent model of a real-world differential capacitive sensor. As visible, there are three main capacitive contributions to the overall stray impedances: C_{pu}, C_p and C_{pl} [9-10].

The mitigation of the effects of both C_{pu} and C_{pl} is typically exploited by means of a suitable topology: for instance, the use of an AC-driven setup inherently mitigates both of them since (see Fig. 1.13) C_{pl} is grounded, while C_{pu} is connected to a very low impedance signal generator. The following considerations will then be focused on the effects of C_p only.

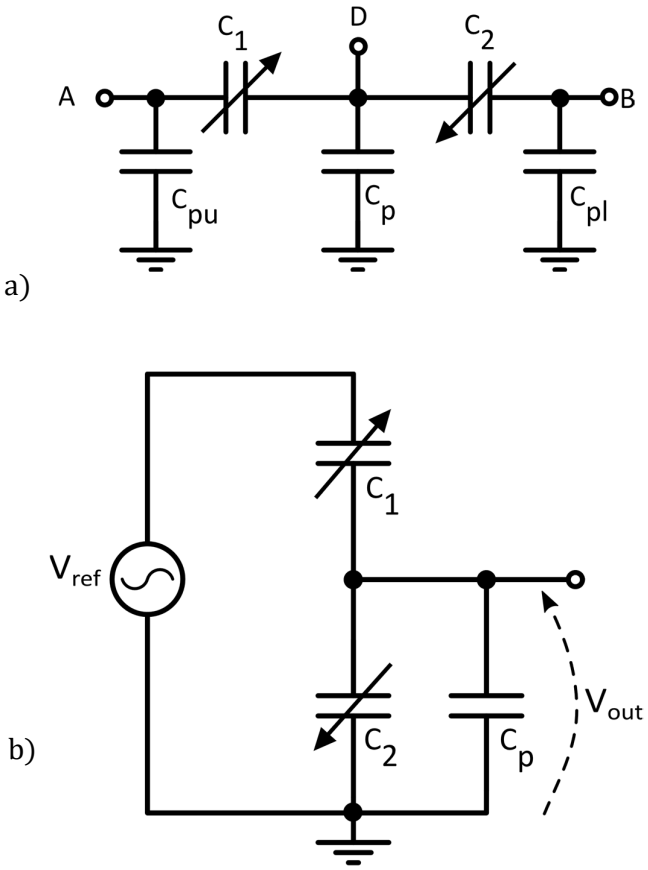


Figure 1.14 Real-world differential capacitive sensor equivalent model: a) generic, b) driven by an AC source.

In this sense, let us consider the simple configuration of Fig.1.14b; we can write that:

$$V_{out} = V_{ref} \frac{C_1}{C_1 + C_2 + C_p} \tag{1.13}$$

Therefore, by substituting Eq.s (1.11) and (1.12) into Eq. (1.13), we can find the relationship between the input voltage (V_{ref}) and the output voltage (V_{out}) for linear sensors as:

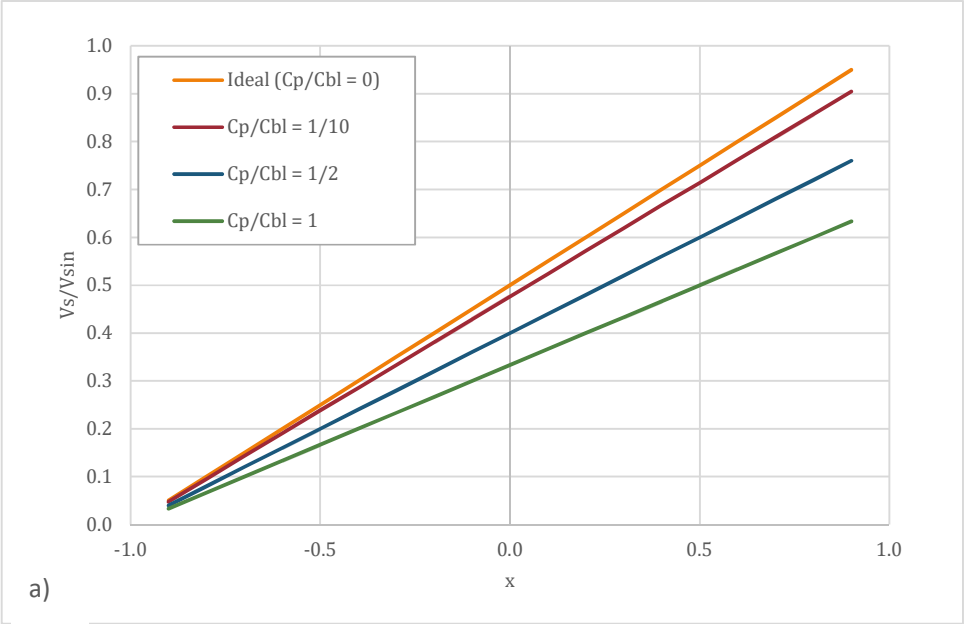
$$V_{out} = V_{ref} \frac{1 + x}{2 + \frac{C_p}{C_{bl}}} \tag{1.14}$$

and for hyperbolic ones as:

$$V_{out} = V_{ref} \frac{\frac{1}{1 - x}}{\frac{2}{1 - x^2} + \frac{C_p}{C_{bl}}} \tag{1.15}$$

Ideally ($C_p = 0$) both equations tend to the same one. However, as visible, in presence of parasitic capacitances, the readout circuit suffers a decrease in sensitivity (maintaining a linear behavior) in case of linear sensors (see Fig. 1.15a), while in case of hyperbolic ones, linearity worsens if the ratio C_p/C_{bl} increases (see Fig. 1.15b). This analysis holds for more complex interfaces.

Advanced interfacing techniques employing a mitigation of the effects of parasitic capacitances will be discussed in the following chapters.



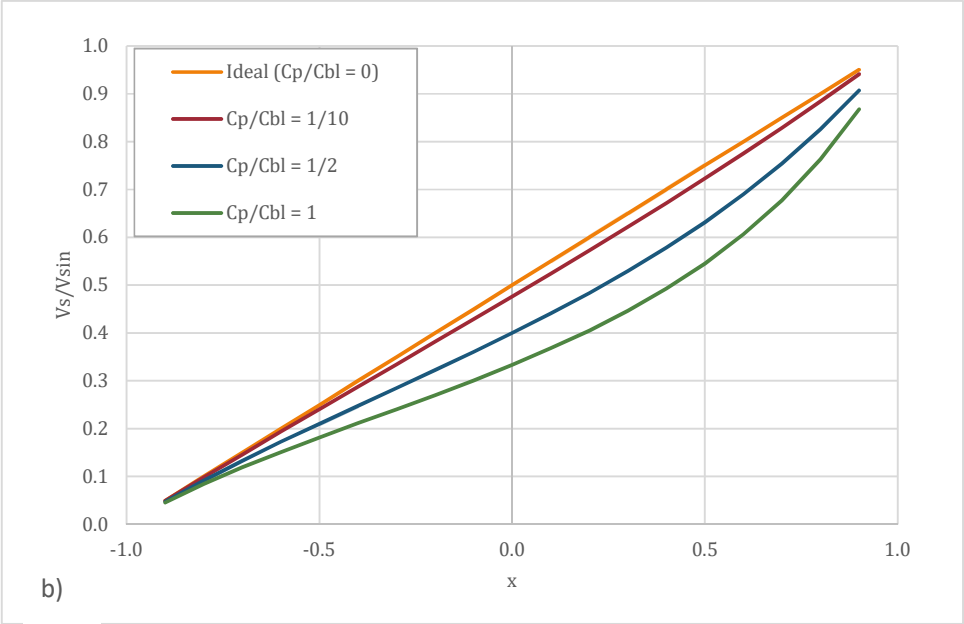


Figure 1.15 Effects of Cp on the readout of a) linear sensors, b) hyperbolic sensors.

2 VOLTAGE MODE DIFFERENTIAL CAPACITIVE SENSOR INTERFACES: STATE OF THE ART

In this chapter, we will analyze the state of the art in the design of voltage mode electronic interfaces for a differential capacitive sensor, highlighting benefits and drawbacks of each solution. We will consider as voltage mode all these techniques where the majority of the processing of signals within the actual interface involves the manipulation of voltages, or in other words, all these interfaces where, even if there is the presence of a current signal, this is converted into a proportional voltage for further processing [11-12].

The discussion will be focused on four macro approaches: the *step measurement*, where the sensing process involves many preparatory phases prior to the actual readout, *the oscillator based* capacitance to time conversion, *the time continuous* capacitance to voltage conversion and the capacitance to digital conversion. The output of the latter three groups is well defined (a time, a voltage or a binary code) whereas the first group can have both a time or a voltage output.

Both discrete and integrated solutions will be analyzed, without paying too much attention underlining this feature, but rather focusing on their working principle.

2.1 Step measurement

As the name suggests, these techniques involve the use of switches and driving clocks through which it is possible to modify the topology of the circuit to adequately carry out one of at least two steps to perform the differential capacitance readout.

The first proposal [13-14] is intended to be used with micromachined transducers, and hence aims to have good sensitivity, accuracy and immunity to noise and circuit non idealities. The equivalent schematic is shown in Fig. 2.1. It can be thought of as a sample and hold where the holding capacitor is represented by the two differential sensor capacitors. There are two switching signals, Φ_1 and Φ_2, sharing the same frequency and opposite phases, therefore the readout process involves two distinct steps.

During the first one, switches S_1, S_2 and S_3 are on, while S_4, S_5 and S_6 are off. Sensing capacitors are therefore precharged to V_{ref} and $-V_{ref}$ respectively. The holding capacitor C_h is added so to provide Op-Amp gain error compensation, across the two phases together with C_1 and C_2 (this technique is thoroughly explained in [15] and strictly resembles the correlated double sampling CDS technique). During the second phase, Φ_2, switches status is inverted.

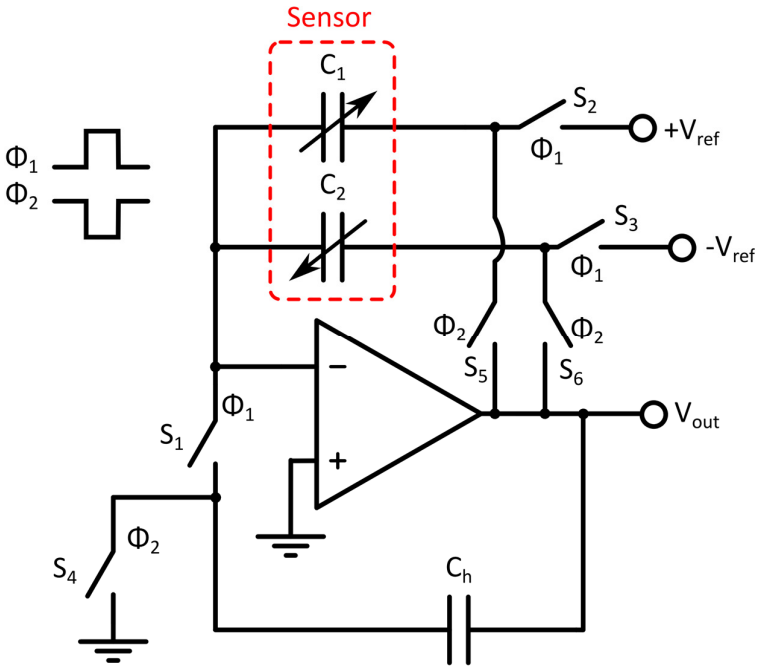


Figure 2.1 Sample and hold based interface [13].

This means that the two capacitors C_1 and C_2 of the sensor are connected in parallel, and therefore, neglecting non idealities, it is possible to calculate the output voltage as follows:

$$\boldsymbol{V_{out}(\Phi_2) = \frac{Q_{TOT}}{C_{TOT}} = \frac{C_1 V_{ref} - C_2 V_{ref}}{C_1 + C_2} = x V_{ref}} \tag{2.1}$$

Taking back into consideration non idealities, the first thing to notice is that this technique allows to neglect the effects of parasitic capacitances C_{pu} and C_{pl} which are in parallel with C_h during the measuring stage (Φ_2) because they are always connected to a low impedance node.

Due to the negative feedback, at a first glance it might appear that also C_p could be neglected, however the effects of a finite gain might make this statement wrong. As a consequence, the effects to be taken into consideration are Op-Amp finite gain A and offset, as well as charge injection which is a typical drawback of switched capacitors topologies. Considering the nth cycle, the output voltage for Φ_1 and Φ_2 can be computed as:

$$\boldsymbol{V_{out}(\Phi_{1,n}) = V_{out}(\Phi_{2,n-1}) + \\ + \frac{1}{C_h} \frac{(C_1 + C_2) V_{out}(\Phi_{2,n-1}) - (C_1 - C_2) V_{ref}}{1 + \frac{C_h + C_1 + C_2 + C_p}{A C_h}}} \tag{2.2}$$

$$\boldsymbol{V_{out}(\Phi_{2,n}) = \frac{(C_1 - C_2) V_{ref} + \frac{(C_1 + C_2 + C_p) V_{out}(\Phi_{1,n})}{A}}{(C_1 + C_2)\left(1 + \frac{C_h + C_1 + C_2 + C_p}{A C_h}\right)}} \tag{2.3}$$

Under the condition $C_h >> C_1 + C_2$ Eq. 3.2 can be simplified in:

$$\boldsymbol{V_{out}(\Phi_{1,n}) = V_{out}(\Phi_{2,n-1})} \tag{2.4}$$

Substituting Eq. 3.4 in Eq. 3.3 it is possible to simplify it:

$$V_{out}(\Phi_{2,n}) = \frac{(C_1 - C_2)V_{ref}}{C_1 + C_2} = xV_{ref} \quad (2.5)$$

From this analysis it is clear that, more than a compensation, the proposed topology helps relaxing the high gain condition on the active device allowing to achieve, with a lower gain, the same performances (in terms of accuracy) that are attainable only with a much higher Op-Amp gain. This is a helpful property when designing with very low pitch technologies where high gain is hard to achieve. On the other hand, the main limitation of the interface is due to the charge injection of switches S_1, S_2, S_3 on the sensor capacitors. This can be estimated as a 'parasitic' voltage, given by:

$$\delta V_{out}(\Phi_2) = \frac{Q_{inj}}{C_1 + C_2} \quad (2.6)$$

The amount of total injected charges Q_{inj} strictly depends on the adopted technology parameters and can be only mitigated by decreasing the dimensions of the switches.

Another possible approach concerns the use of an oscillator and rely on its switching frequency to execute the ratiometric operation [16]. This is the working principle of the following interface which, anyway, relies on a capacitance to voltage conversion. This means that the magnitude that is proportional to the x parameter remains a voltage amplitude.

The circuit solution is shown in Fig. 2.2 and consists of a switched inverting charge sensitive amplifier (OA), a comparator (OB) and a low pass filter. The CSA, together with the comparator, implements a relaxation oscillator. The low pass filter is responsible for the generation of the output voltage. In the circuit, there are 5 switches: S_1 and S_2 are driven by a fixed external clock signal with a period T_c and 50% duty cycle allowing the sensor capacitors to charge and discharge at a fixed rate, while S_3, S_4 and S_5 are driven by the oscillator itself. The two reference voltages V_{ref} and $-V_{ref}$ are used to precharge C_1 and C_2 and to generate the output signal. S_3 and S_4 allow only one between C_1 and C_2 to be connected at the OA amplifier at a time.

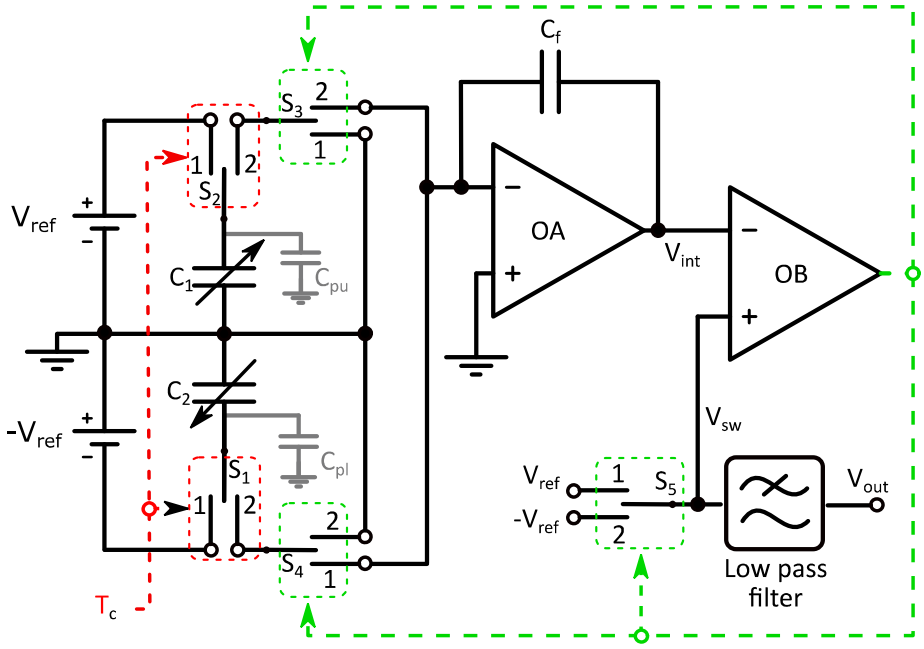


Figure 2.2 Switched capacitor oscillator based C to V interface [16].

The interface works as follows: let us suppose as a starting condition that the output of the integrator is positive, as well as its first order derivative.

Switches S_3, S_4 and S_5 are in the 1 condition, while S_1 and S_2 change between 1 and 2 at each clock cycle (1 at the rising edge, 2 at the falling edge). As long as they remain in condition 1, C_1 is charged to $+V_{ref}$, while C_2 to $-V_{ref}$. When the switches toggle to position 2, C_1 is grounded while C_2 is connected to the CSA. This means that at each clock cycle, the feedback capacitor C_f receives part of the charges stored in C_2 and therefore the output voltage of the integrator increases by a fixed step:

$$\boldsymbol{V_{int}(n) = V_{int}(n-1) + V_{step+}}$$

$$\boldsymbol{V_{step+} = V_{ref}\frac{C_2}{C_f}} \qquad (2.7)$$

This trend continues as long as the integrator output reaches the threshold of the comparator V_{ref} when S_5 is on the position 1. Once this condition is reached, the comparator output V_c becomes low and switches S_3, S_4 and S_5 are driven to position 2. In this condition at each external clock cycle, capacitor C_1 is connected to the integrator, which, as a consequence starts decreasing its output:

$$\boldsymbol{V_{int}(m) = V_{int}(n) - |V_{step-}|} \qquad (2.8)$$

$$|V_{step-}| = |V_{ref}|\frac{C_1}{C_f}$$

This situation, again, stands as long as the output of OA reaches the comparator negative threshold. The behavior described so far repeats until unperturbed. The time T_H that V_{int} takes to ramp up to V_{ref}, depends therefore on C_2, while the time T_L that it takes to ramp down to -V_{ref}, depends on C_1, as shown in Fig. 2.3. From Eq. 2.7 and Eq. 2.8 it is possible to calculate T_H and T_L as:

$$T_H = T_c\frac{2V_{ref}}{V_{step+}} = T_c\frac{2C_f}{C_2} \tag{2.9}$$

$$T_L = T_c\frac{2V_{ref}}{V_{step-}} = T_c\frac{2C_f}{C_1} \tag{2.10}$$

Taking into consideration the low pass filter input voltage V_{sw}, this signal oscillates between V_{ref} and -V_{ref} according to the T_H and T_L times (see Fig. 3.3) so, by setting a sufficiently low cutoff frequency $fc << 1/(T_H+T_L)$ it is possible to express its output as:

$$V_{out} = \frac{1}{T_H+T_L}\left(\int_0^{T_H} V_{ref}\,dt + \int_{T_H}^{T_H+T_L} -V_{ref}dt\right) = \\ = \frac{T_H-T_L}{T_H+T_L}V_{ref} = \frac{C_1-C_2}{C_1+C_2}V_{ref} = xV_{ref} \tag{2.11}$$

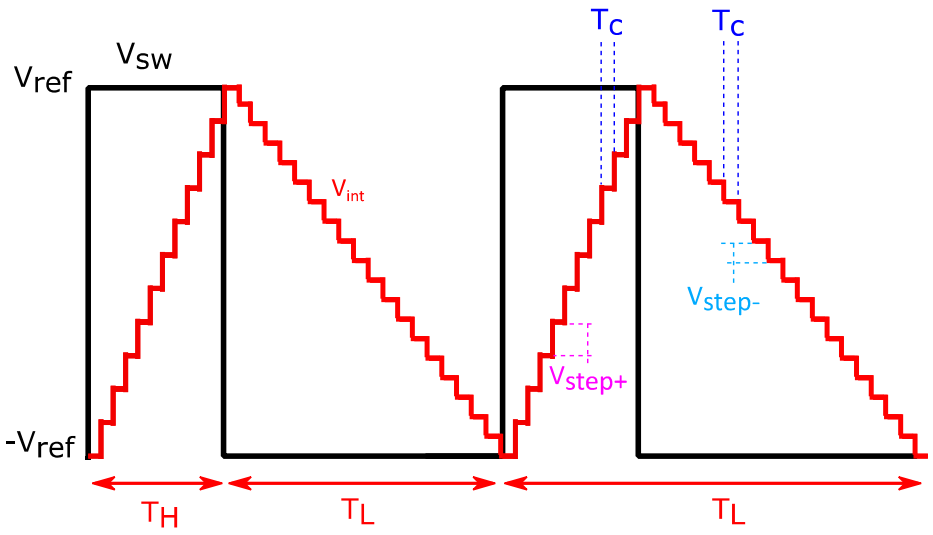


Figure 2.3 Interface behavior when $C_1 > C_2$ [16].

Unlike the previous solution, in this interface the effects of stray capacitances have to be taken into account. Particularly, C_p can be neglected since it is always grounded. C_{pu} and C_{pl} however affect the measurement since they modify T_h and T_l introducing both a loss of sensitivity and an offset:

$$\boldsymbol{V_{out} = \left(\frac{C_1 - C_2}{C_1 + C_2 + C_{pu}} + \frac{C_{pu} - C_{pl}}{C_1 + C_2 + C_{pu}} \right) V_{ref}} \qquad \textbf{(2.12)}$$

Concerning charge injection and clock feedthrough, the same considerations as before are applicable to this scenario.

There are solutions expressively developed to deal with parasitic capacitance effects, as shown in Fig. 2.4 [17-18].

The circuit consists of a charge amplifier and 8 switches that work in different steps, driven by two clocks sharing the same frequency ($1 / T$) and opposite phase. During the first stage (Φ_1 high), switches S_2, S_3, S_5, S_6, S_8 are active. Capacitor C_i is therefore discharged, while it is possible to calculate the total amount of charges stored in this configuration (using V_{ref} as reference potential), as follows:

$$\boldsymbol{Q_{tot\Phi 1} = \frac{V_{DD}}{2} C_1 + \left(-\frac{V_{DD}}{2} C_2 \right) + V_{DD} C_{pu}} \qquad \textbf{(2.13)}$$

Noticeably, C_p and C_{pl} are not present into Eq. 3.13: indeed, C_{pl} is grounded, so it does not contribute to the overall charge, while C_p, although charged to V_{ref}, does not experience boundary condition changes during Φ_2 and therefore is not present in Eq. 3.13. At time equal to $nT-T/2$, Φ_2 goes high, while Φ_1 turns low.

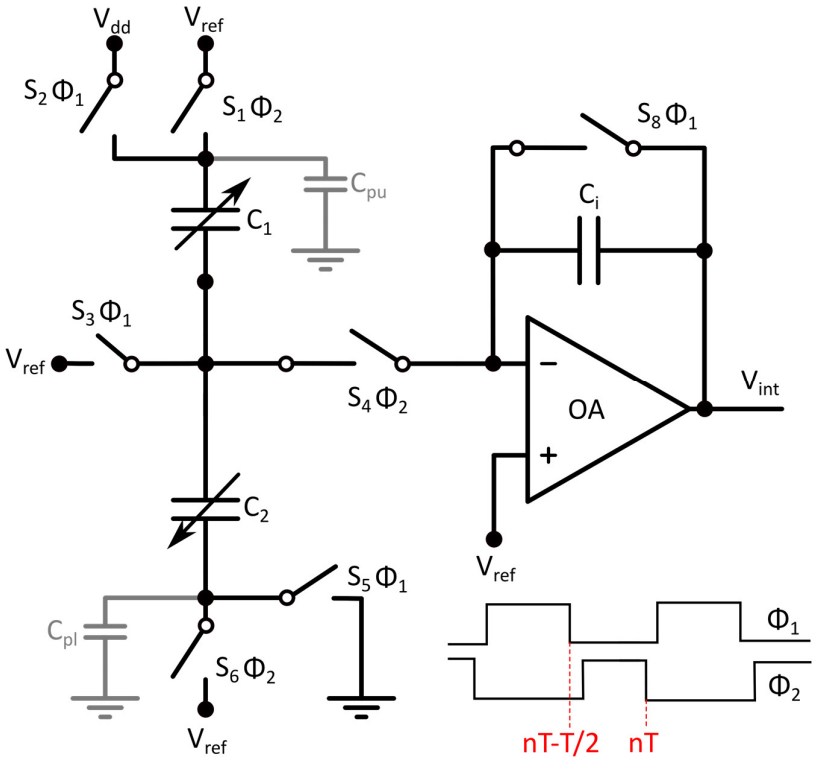


Figure 2.4 Switched capacitor CSA interface with parasitic cancellation [17].

It is possible to compute the total charge stored in this new configuration as:

$$\boldsymbol{Q_{totΦ2} = \frac{V_{DD}}{2}\left(C_T + C_{pu} + C_{pl} + (1+A)C_i\right) - (C_T + (1+A)C_i)V_i} \qquad \textbf{(2.14)}$$

where C_t is given by $C_1 + C_2$ and A is the amplifier gain. Now, considering that the output voltage at any time can be calculated as:

$$\boldsymbol{V_{int} = A\left(\frac{V_{DD}}{2} - V_i\right)} \qquad \textbf{(2.15)}$$

and that the total amount of charges in both phases has to remain equal, it is possible to evaluate the output of the interface as:

$$\boldsymbol{V_{int}(nT) = \frac{AV_{DD}(C_{pu} - C_{pl} - C_i + 2\Delta C)}{2(C_T + C_i(1+A))}} \qquad \textbf{(2.16)}$$

The x parameter is contained in the ΔC factor at the numerator and, as visible, parasitic capacitors are absent from the denominator. Therefore, the sensitivity error is inherently removed from the measurement. Although apparently effective,

an offset error arises in this interface circuit in the likely scenario where, due to fabrication processes, values of C_{pu} and C_{pl} are different from each other.

To deal with common mode disturbs, indeed, the same techniques based on a charge sensitive amplifier can be used in a differential fashion as in [19-20]. Fig. 2.5 depicts such a scenario, where a fully differential switched capacitor CSA based interface is shown.

This interface makes use of the correlated double sampling technique to reduce amplifier gain error and offset. The interface consists of a bridge-like structure made of sensor capacitors C_1 and C_2 and reference capacitors C_R. C_f is the feedback capacitor of the CSA, while C_c and C_h work with the sample and hold structures in order to provide an easy analog-to-digital conversion of the output.

According to the switches status shown in Fig. 2.6, the circuit executes a readout in four steps: *discharge*, *sensing A (Charge)*, *sensing B (Charge)*, *sampling*. The two sensing phases are used to carry out the CDS algorithm, so the errors coming from Op-Amp non idealities are stored and then compensated.

The working principle of the interface is the following. During the *reset* phase, S_2 and S_6 are on, while also S_4 toggles between on and off. This ensures the full discharge of sensor capacitors, reference capacitors and feedback capacitors. Charge *sensing 1* phase starts with switches S_1, S_2 and S_6 toggling their state.

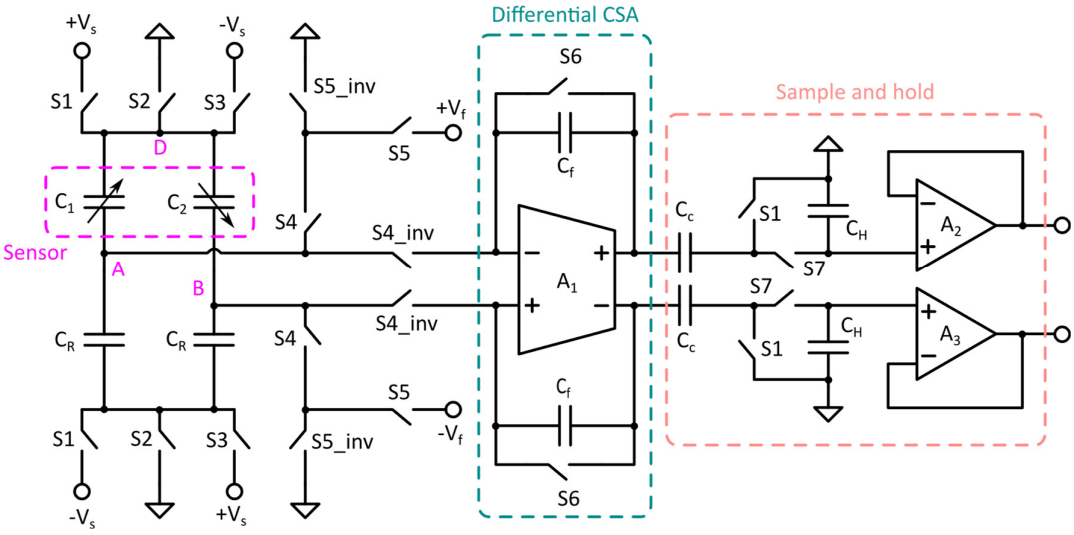


Figure 2.5 Fully differential switched capacitor CSA interface [19].

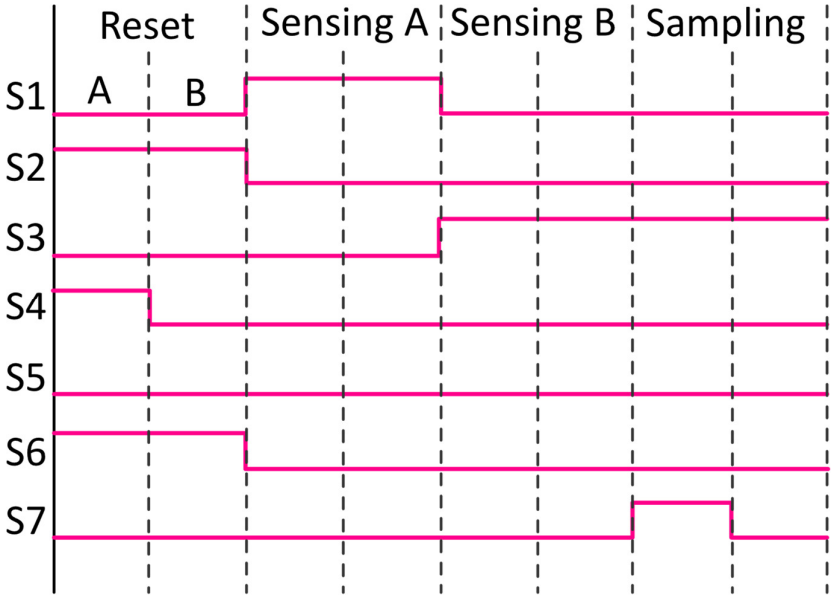


Figure 2.6 Switches status of the analysed interface according to the relative phase of the readout [19].

This makes sure that the bridge is biased between the two reference voltages $+V_s$ and $-V_s$. Under these circumstances, the differential output of the CSA is given by:

$$\Delta V_{out,1} = V_{error} - V_s \frac{C_1 - C_2}{C_f} \tag{2.17}$$

During the *second sensing* stage, the switches S_1 and S_3 are toggled and therefore the reference voltages are swapped. The CSA output is given by:

$$\Delta V_{out,2} = V_{error} + V_s \frac{C_1 - C_2}{C_f} \tag{2.18}$$

Finally, during the *sampling phase*, switch S_7 is activated. The differential output voltage of the sample and hold results proportional to $C_1 - C_2$ and independent from the voltage Verror:

$$\Delta V_{out,SH} = \Delta V_{out,1} - \Delta V_{out,2} = 2V_s \frac{C_1 - C_2}{C_f} \tag{2.19}$$

Due to the differential structure, the interface is less sensitive to common mode disturbs, however, switches have to be carefully designed and driven in order to minimize charge injection and clock feedthrough.

2.2 Switchless capacitance to time converter

In this section, capacitance to time interfaces will be analyzed. Unlike in the previous one, they do not employ clock driven switches and therefore, are inherently immune to clock feedthrough and charge injection errors.

The authors, in [21], propose a relaxation oscillator based circuit, shown in Fig. 2.7. It consists of a voltage integrator (*A1*), characterized by a variable feedback path, an inverting voltage adder (*A2*) and two comparators (*A3* and *A4*). The integrator together with the variable threshold comparator (*A3*) implement the relaxation oscillator, while *A4* acts as a simple voltage squarer. For the following analysis, diodes D_1 and D_2 can be considered ideal, since they are in the negative feedback path of an amplifier. Since they are back-to-back positioned, only one of them at a time can be active, according to voltages V_{c1}, V_{c2} and V_1. $R_{1\text{-}3}$ are assumed equal to each other. As a matter of fact, we can say that *A2* is effectively a simple inverting voltage follower.

The oscillation period of the circuit is determined by the sum of four distinct times (see Fig. 2.7 and Fig. 2.8). Let us impose as a starting condition, T_1, that V_4 is high (V_u), as well as V_1. Therefore, D_2 is active, C_2 is charged while V_1 decreases linearly. This phase lasts until V_1 reaches *0 V*, therefore D_2 is turned off. Calling V_d the starting voltage across the capacitor C_2 (note that V_d should be equal to V_u, any imbalance is reflected in the readout process), it is possible to quantify T_1 as:

$$\boldsymbol{T_1 = C_2 R_t \frac{V_d}{V_u}} \qquad \textbf{(2.20)}$$

During T_2 phase, the diode D_1 is active. Since V_3 is still lower than V_4, the latter voltage remains high, equal to V_u and therefore the output of the integrator continues decreasing with a slope that depends on C_1. Since this phase is not influenced by the voltage because the integrator is driven by the threshold voltage of the comparator, the time that is taken to V_1 to reach the threshold voltage of the comparator *A3* ($-V_u$) is given by

$$\boldsymbol{T_2 = C_1 R_t} \qquad \textbf{(2.21)}$$

At this stage, V_4 changes polarity and the same for the threshold voltage of the comparator *A3* (goes to $+V_u$). This means that the voltage V_1 now starts raising back.

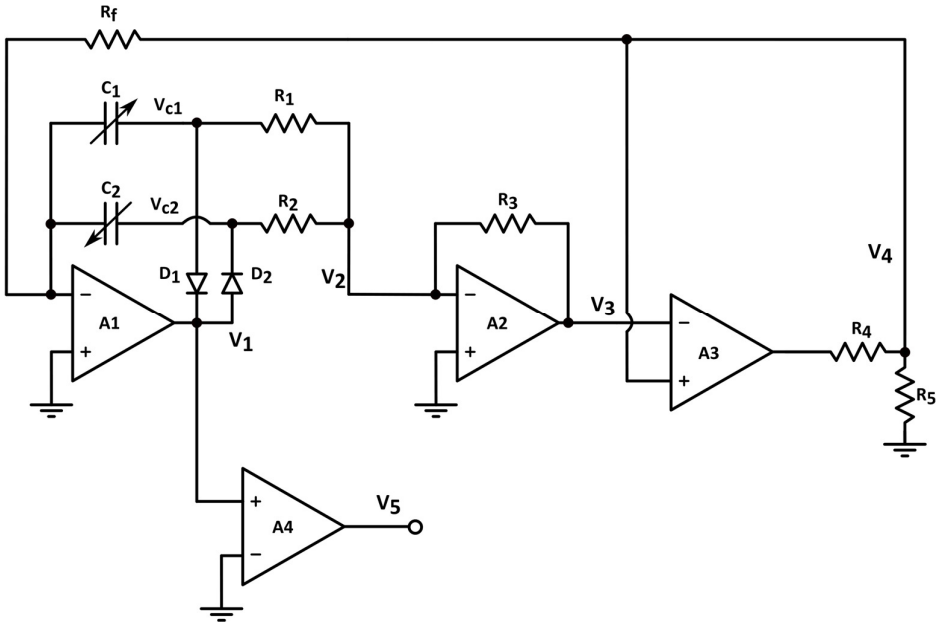


Figure 2.7 Capacitance to time relaxation oscillator based interface [21].

These are the starting conditions for T_3, where D_1 is still conducting. This phase concludes when V_1 reaches $0\ V$ and the two diodes toggle their states. Time T_3 is equal to:

$$\boldsymbol{T_3 = C_1 R_t \frac{V_u}{V_d}} \tag{2.22}$$

The last phase, T_4, returns all the signals back to the starting conditions: V_4 is negative so the output of $A1$ keeps on raising until V_3 reaches the threshold voltage of $A3$. This phase lasts for a time given by:

$$\boldsymbol{T_4 = C_2 R_t} \tag{2.23}$$

From here, this cycle keeps on repeating indefinitely. To evaluate the measurand, it is possible to measure the duty cycle (D) of V_5:

$$\boldsymbol{D = \frac{T_{high}}{T_{high} + T_{low}} = \frac{T_1 + T_3}{T_1 + T_2 + T_3 + T_4} = } \\ \boldsymbol{= \frac{C_2}{C_1 + C_2}\left(1 + \frac{C_1 - C_1\frac{V_u}{V_d}}{\frac{C_1 V_u}{V_d} + C_2}\right)} \tag{2.24}$$

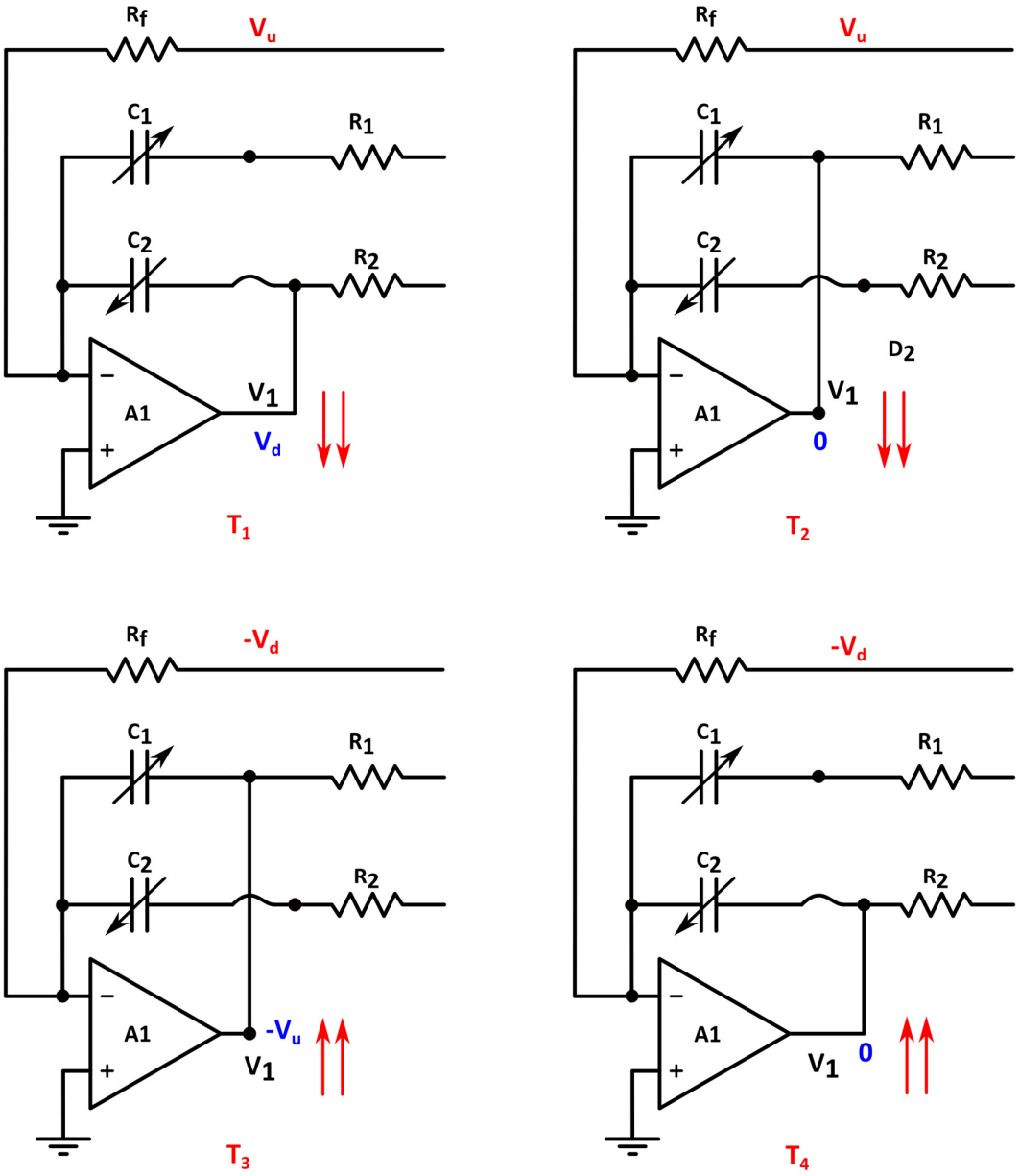


Figure 2.8 Circuit configuration based on diodes conditions: in blue the starting condition for V1, the red arrows show the tendency of V1 during each phase.

As visible from Eq. 2.24, the main error source for the readout is the mismatch between V_u and V_d. Moreover, with respect to switched capacitors circuits, the interface under analysis has a high number of passive elements which makes it weak with respect to their mismatches, and also makes it complicated to integrate into a chip.

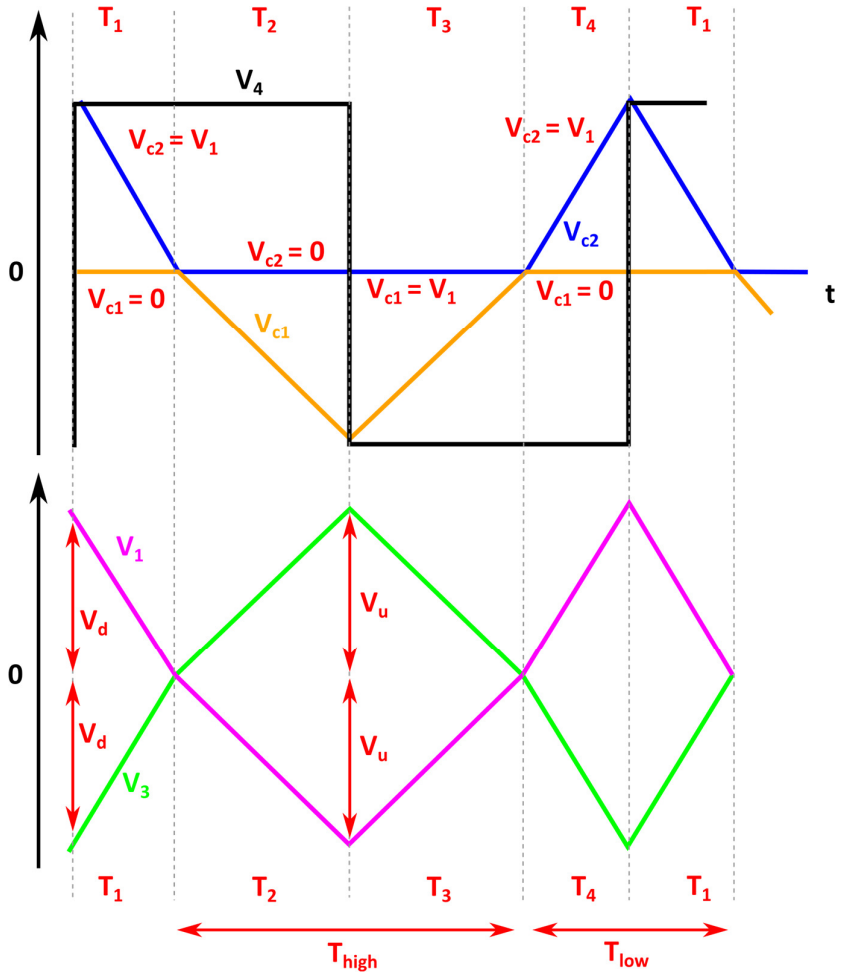


Figure 2.9 Time domain behavior of the interface signals [21].

A similar, yet modified approach is proposed in [22] (shown in Fig. 2.10). This interface still makes use of a relaxation oscillator, but instead of relying on diodes to dynamically adjust the feedback of the integrator, it uses multiple feedbacks to sustain the oscillation. Since the output stage of the interface is a mixer, it allows to incapsulate the differential capacitive readout on both its frequency and its duty cycle. The circuit is formed by three Op-Amps, which employ an integrator and two variable reference comparators. Passive elements play a crucial role since they allow to set sensitivity, resolution and range of the interface, other than fixing the initial oscillation of the interface together with sense capacitors.

The working principle is shown in Fig. 2.11 and can be analyzed as follows. Let us impose as starting condition for the phase 1 that the output of the integrator V_{int} is at V_{high} (which represents the peak value for its output). Let us also impose that the voltage that feeds the integrator, V_1, is high (i.e. V_{comp2} is equal to V_{dd}). V_1 is a square

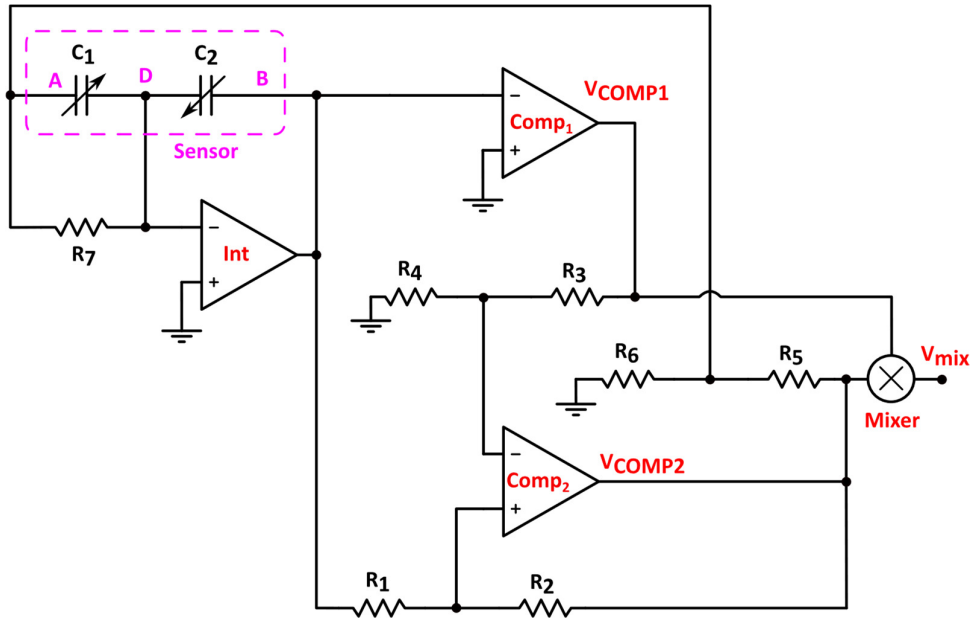


Figure 2.10 Multiple feedback C to T interface [22].

wave whose amplitude is a portion of V_{dd}. To complete the definition of the initial state, it is enough to impose that $V_{int} > V_1$ and $V_3 > V_2$ therefore $V_{comp1} = V_{dd}$.

All these conditions are set through the resistive dividers of the interface. From this state, the voltage V_{int} starts lowering linearly, and the same does V_3. This condition lasts as long as V_{comp1} toggles to V_{ss}. For this to happen, it is necessary that:

$$\frac{R_6}{R_5 + R_6} > \frac{R_4}{R_3 + R_4} \tag{2.29}$$

Since, however, V_{comp2} is still at V_{dd}, the voltage at the integrator output during phase 2 continues lowering. Once it reaches a level so that V_3 becomes lower than V_2, V_{comp2} toggles to V_{ss} and V_{int} starts raising again from the minimum value V_{low}.

The raising of V_{int} starts with phase 3. It is the same as described during phase 1: V_{comp1} and V_{comp2} remain low while V_{int} lowers, until V_{int} becomes greater than V_1 so forcing V_{comp1} to switch to V_{dd}. During the last phase of the cycle, V_{int} reaches back V_{high} closing a full period of V_{int} when V_{comp2} raises to V_{dd}.

The overall output of the interface, V_{mix} has a frequency which is twice doubled respect to its inputs (indeed a multiplication produces also the sum of the input frequencies at its output); it changes according to the polarity of its inputs V_{comp1} and V_{comp2}, therefore during phase 1 and phase 3 it is positive, while it is negative during the other two.

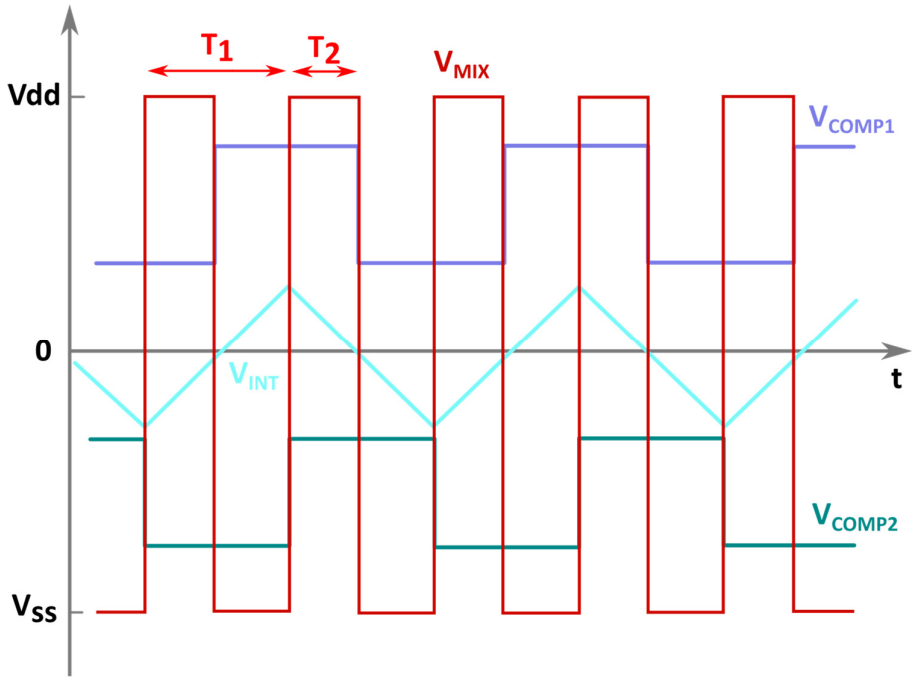


Figure 2.11 Time domain behavior of the analyzed interface (V_{COMP1} and V_{COMP2} suitably scaled for a better view) [22].

By then evaluating the two times T_1 and T_2 representing the period and the pulse width of V_{mix} respectively, it is possible to evaluate C_1 and C_2 as follows:

$$C_1 = \frac{1}{R_7}(T_2 - T_1)\alpha - \frac{1}{R_7}\frac{T_1}{2}$$
$$C_2 = \frac{1}{R_7}(T_2 - T_1)\beta \tag{2.30}$$

where:

$$\alpha = \left(\frac{\frac{R_1}{R_1+R_2} + \frac{R_4}{R_3+R_4}}{\frac{R_6}{R_5+R_6}\frac{R_1}{R_2+R_1} - \frac{R_2}{R_2+R_1} - \frac{R_4}{R_4+R_3} - \frac{R_6}{R_5+R_6}} \right)$$
$$\beta = \left(\frac{\left(1 + \frac{R_1}{R_1+R_2}\right)\frac{R_6}{R_5+R_6}}{\frac{R_6}{R_5+R_6}\frac{R_1}{R_2+R_1} - \frac{R_2}{R_2+R_1} - \frac{R_4}{R_4+R_3} - \frac{R_6}{R_5+R_6}} \right) \tag{2.31}$$

Like mentioned before, from the moment that passive elements have the task to adjust parameters like sensitivity and resolution and at the same time the working baseline frequency (readout speed), it can be necessary a compromise between

them. Due to the readout technique this interface is inherently robust with respect to low frequency noise, common mode disturbs and parasitic capacitances but results extremely weak with respect to mismatches between resistors which are responsible for generating switching thresholds.

2.3 Switchless capacitance to voltage converters

The same approach based on a relaxation oscillator is often utilized to produce a voltage as output magnitude as well [23-24] as visible from Fig. 2.12.

A1 and *A2* are the comparator and the integrator, respectively, that implement the relaxation oscillator, which is the core of the interface. In order to produce a voltage output, however, a differentiator (*A3*) and an inverting amplifier (*A4*) are added to the circuitry. The differential capacitance transducer is involved both in the integration (C_1) and the differentiation (C_2) stages.

The working principle is the following. As visible, the voltages V_1 and V_2 are weighted by R_7 and R_8. Let us suppose that when the sum of the weighted V_1 and V_2 (represented by V_c) is negative, the output of *A1* is positive; vice versa, when V_c is positive, the output of *A1* is negative (see Fig. 2.13).

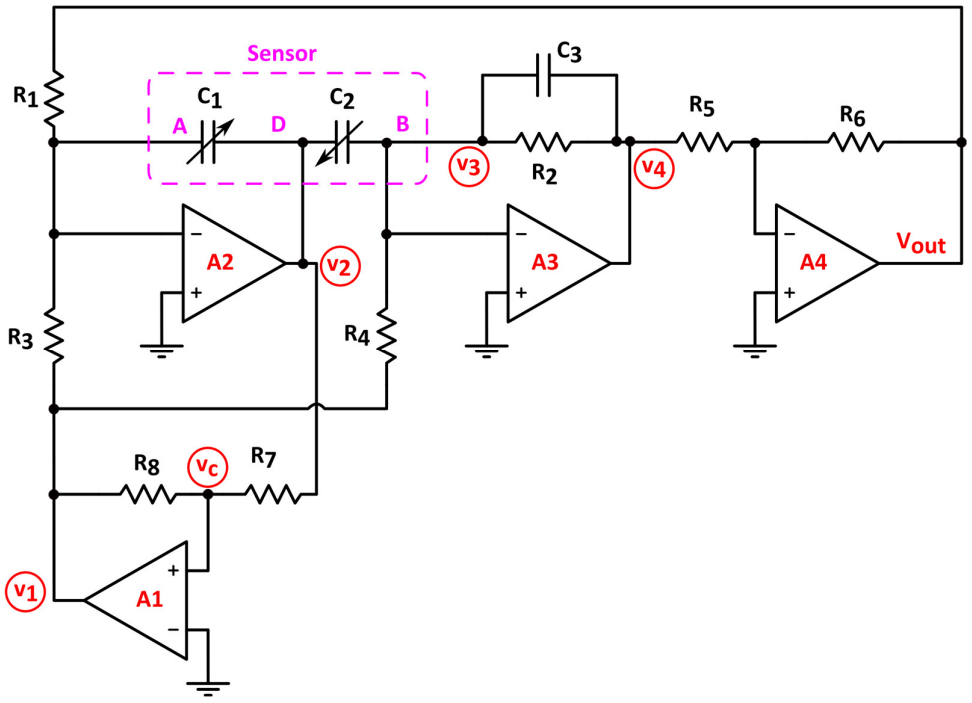


Figure 2.12 Relaxation oscillator based C to V interface [23].

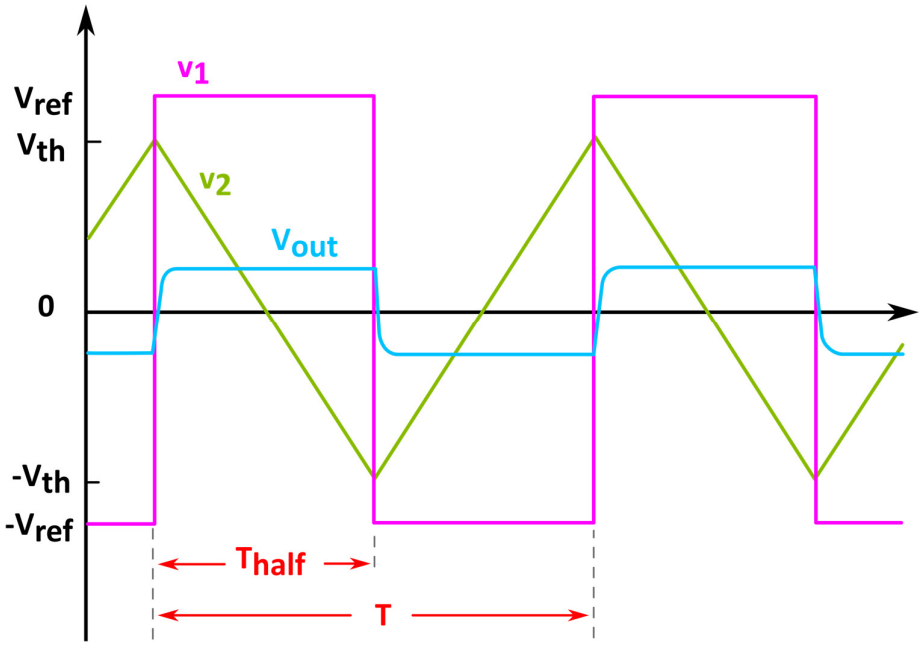


Figure 2.13 Time domain behavior of the analyzed interface [23].

We can write that:

$$V_1 = V_{ref}\, sgn[V_c] \tag{2.32}$$

being:

$$V_c = V_1 \frac{R_7}{R_7 + R_8} + V_2 \frac{R_8}{R_7 + R_8} \tag{2.33}$$

Since the input of the integrator is a square wave, its output increases and decreases linearly with a triangular shape, while V_3 is a square wave.

Since C_3 is added for stability purposes, it can be neglected in the calculation of the interface output voltage. Considering all the Op-Amps as ideal, it is possible to write:

$$V_{out} = \frac{C_1 \frac{R_2}{R_4} - C_2 \frac{R_2}{R_3}}{C_1 \frac{R_5}{R_6} + C_2 \frac{R_2}{R_1}} V_{ref}\, sgn[V_c] \tag{2.34}$$

Eq. 2.34 can be further simplified assuming that $R_3 = R_4$ and $R_1R_5 = R_2R_6$:

$$V_{out} = V_0\, sgn[V_c] \tag{2.35}$$

$$V_o = \frac{R_1}{R_3}\frac{C_1 - C_2}{C_1 + C_2}V_{ref} = kxV_{ref} \tag{2.36}$$

Therefore, the interface is capable of converting the x value into a linearly proportional voltage. Noticeably, in the case of linear sensors, the output period is independent of the measurand:

$$T_o = 2(C_1 + C_2)R_3\frac{R_7}{R_8} \tag{2.37}$$

Concerning the accuracy of the interface: there are two main sources of errors, passive element mismatches and non-ideality of the Op-Amps. Both of them can be incorporated in the output expression as non-linear and offset errors.

A different approach is shown in the last interface presented in this section [25]. It is based on the synchronous demodulation technique and takes advantage of the possibility to work in closed loop mode so to increase the output dynamic range (acting on the amplitude of the excitation signal). The overall processing takes place partially in the current domain and partially in the voltage one, but we have inserted in this section because the final demodulation and readout is performed in voltage mode.

The open loop operation, whose schematic is shown in Fig. 2.14, is based on a triangular wave generator, a transimpedance amplifier (TIA) a synchronous demodulator and a low pass filter. Capacitors C_1 and C_2 represent the equivalent sensor. The triangular wave is generated through a clock signal which drives four switches that, in turn, charge and discharge two reference capacitors C_t, as shown in Fig. 2.15. The principle of operation is that the sensor is charged by the reference triangular voltages, while the TIA detects and amplifies the difference between the two currents flowing through the sensor. A switching synchronous demodulator (see Fig. 2.15) is responsible for generating an output square wave where the information about the difference between the two capacitors is translated to the baseband. The demodulator is driven by the same clock signal which produces the reference triangular waves. A low pass filter removes the unwanted high

frequencies from the output spectrum. The output voltage as a function of the frequency is given by:

$$\boldsymbol{V_{out}(s) = 2\Delta C f_c R_f v_{in0} H_{LPF}(s)} \qquad \textbf{(2.38)}$$

where v_{in0} is the amplitude of the reference input signal, f_c its frequency and H_{LPF} the transfer function of the low pass filter at the output.

This interface is capable of working in closed loop mode as depicted in Fig. 2.15. This allows to achieve a high dynamic range. The idea is to evaluate the amplitude of the output signal to suitably tune the amplitude of the reference voltages through a controller module. In particular, this block adjusts the amplitude of the reference triangular signals (V_{tri+} and V_{tri-}) so that the larger capacitor is excited by a lower amplitude (this situation is depicted in Fig. 2.16). The linearity error of the interface mainly depends on the linearity of the amplitude controller. The presence of a switched demodulator makes the interface weak with respect to clock feedthrough at the output, although mitigated by the filter.

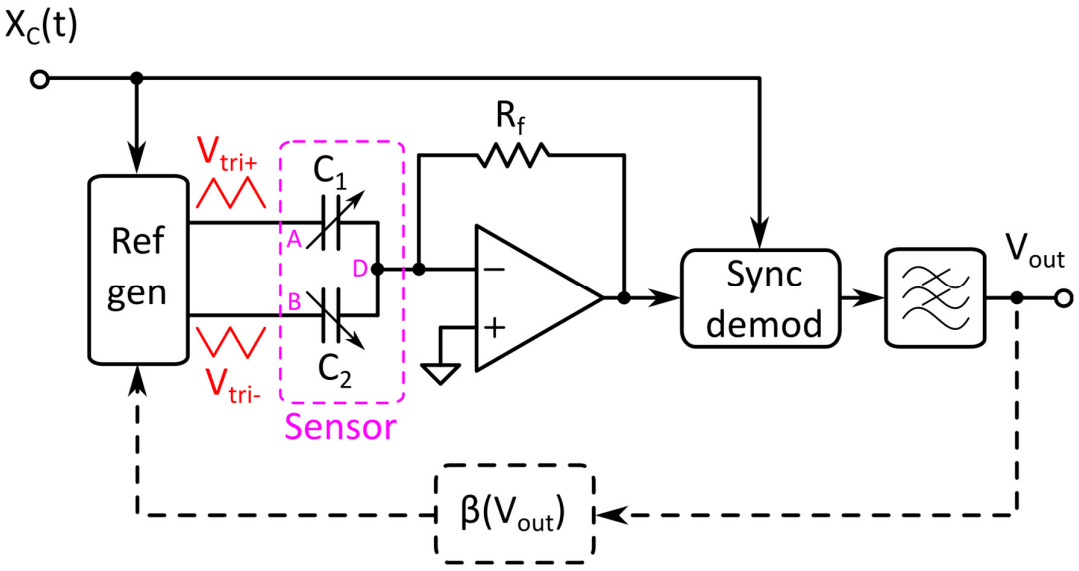


Figure 2.14 Synchronous demodulation C to V interface in open loop conditions [25]

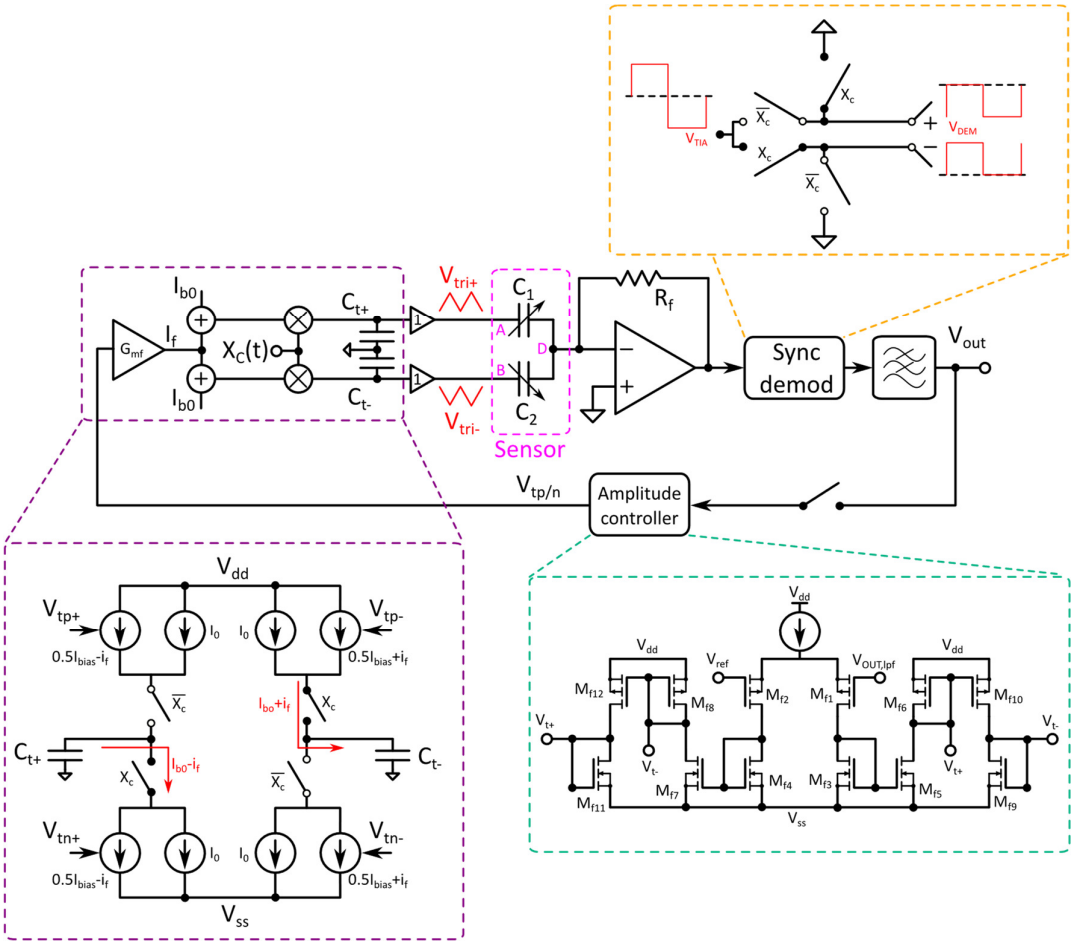


Figure 2.15 Synchronous demodulation C to V interface in closed loop conditions [25].

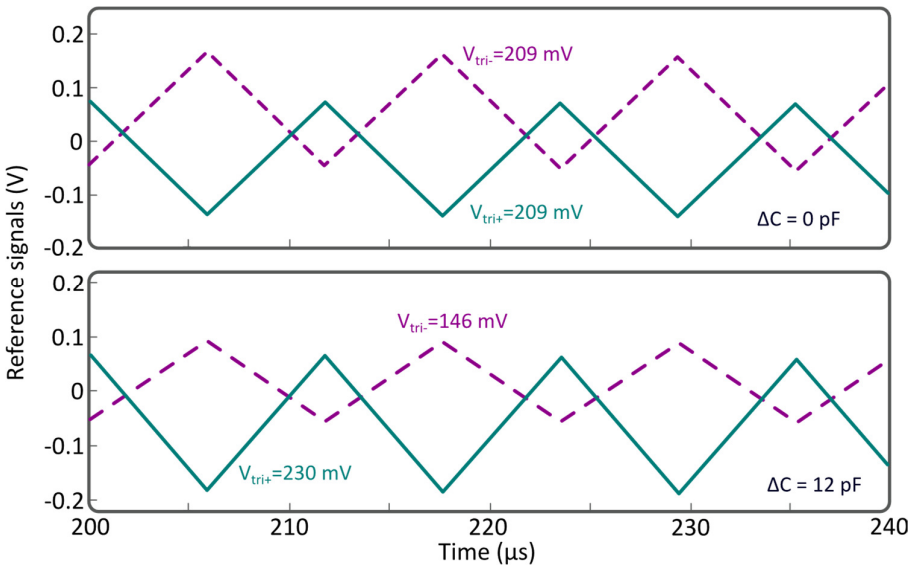


Figure 2.16 Difference between exciting waves during an open loop (top) and closed loop (bottom) operation, supposing that C1 is greater than C2 [25].

2.4 Capacitance to digital interfaces

In the last section of this chapter, two examples will be given on how it is proposed, in the literature, the direct conversion from a differential capacitance to a digital output. The first interface is shown in Fig. 2.17 [26]. In this manuscript, the differential sensor is embedded between two complementary rails (i.e. they cannot be simultaneously active) driven by a reference current I_{bias}. The readout process relies on the linear increment of the voltage V_{bias} caused by the constant current that charges either C_1 or C_2. The time that it takes for the voltage V_{bias} to reach the reference voltage of the comparator, V_{ref}, is counted by the up/down digital counter. Only one of the two rails is active, and this is determined by the phase generator output driving Q_1 and Q_2.

The idea, here, is to count upwards during the charging of C_1, whereas downwards during the charging of C_2. The difference between the charging times allows to evaluate the difference between C_1 and C_2.

In particular, the readout process consists of two stages, and starts when the signal Q coming from the phase generator is logically low (and therefore NQ is logically

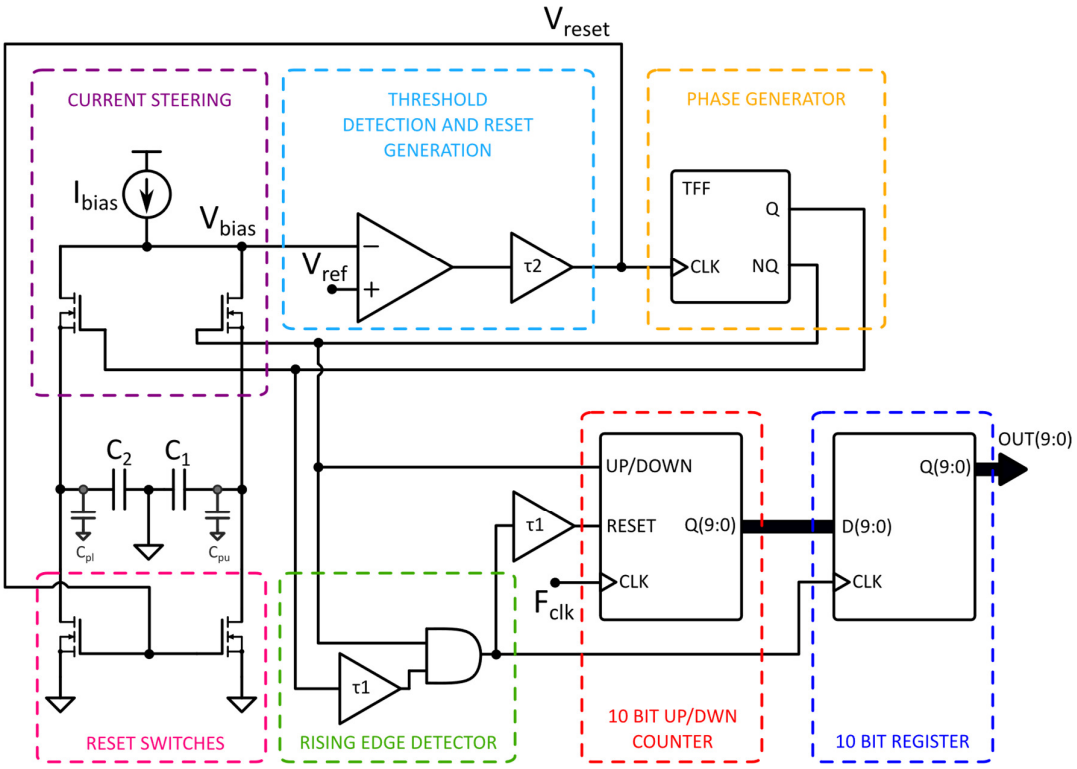


Figure 2.17 Capacitance to digital interface using a digital counter [26].

high). In this condition, the counter increases its digital output by one LSB at each clock cycle, the current I_{bias} starts charging C_1 through Q_2 (which is on) and V_{bias} raises up. This process goes on as long as V_{bias} is lower than V_{ref}. At that time, in fact, V_{reset} is pulled up, the sensor capacitors are discharged, the phase generator toggles its output and the counter is set to count downwards. This transition does not influence the rising edge detector, therefore the counter output is not reset and starts counting backwards from the previous value. The total amount of time taken by this first phase is given by:

$$\boldsymbol{T_1 = \frac{C_1 V_{ref}}{I_{bias}}} \tag{2.39}$$

Capacitor C_2 is charged during the second phase, which, again, lasts until the voltage V_{bias} (which is reverted to the *low* state during the reset pulse) goes higher than V_{ref}. When this condition is reached, the output of the phase generator toggles again restoring the starting condition. The total amount of time taken by the second stage is:

$$\boldsymbol{T_2 = \frac{C_2 V_{ref}}{I_{bias}}} \tag{2.40}$$

At the output of the counter, however, there is a digital code representing the difference between T_1 and T_2:

$$\boldsymbol{T_{out} = \frac{(C_1 - C_2) V_{ref}}{I_{bias}}} \tag{2.41}$$

Since, at the end of the second stage, the signal Q of the phase generator toggles from high to low, the output of the rising edge detector spikes high, resetting the counter and storing the result of the readout process in the register. These two phases repeat indefinitely.

Critical aspects of this approach are related to the reference current stability, that is fundamental for the accuracy of the sensor evaluation. Moreover, the presented design remains susceptible to the effects of parasitic capacitances.

The second approach here described [27-28] uses the microcontroller as a direct interface for the differential capacitive sensor, without adding any external circuitry. The configuration is shown in Fig. 2.18. As visible, the sensor is connected to three

digital terminals of the microcontroller and is represented together with its stray capacitances. Due to the reconfigurability of the pins where the sensor is connected, it is possible to change its boundary conditions, measure a number of different charge and discharge times through the microcontroller internal timers(according to the configuration) and, based on them, extract the value of the sensor itself.

The working principle is the following: by outputting a logical high (V_{dd}), pin 1 charges the total capacitance, C_t, which is a combination of the sensor and parasitic capacitors depending on the status of pin 2 and pin 3, through the resistor R_i. Once the total capacitance is fully charged, pin 1 changes its state to become an input terminal (high impedance) and measures the time that the equivalent capacitor C_t takes to discharge to a predetermined threshold (V_{TL}) through the resistor R_d. To do that, the microcontroller uses its internal Schmitt trigger and counter (see Fig. 2.19).

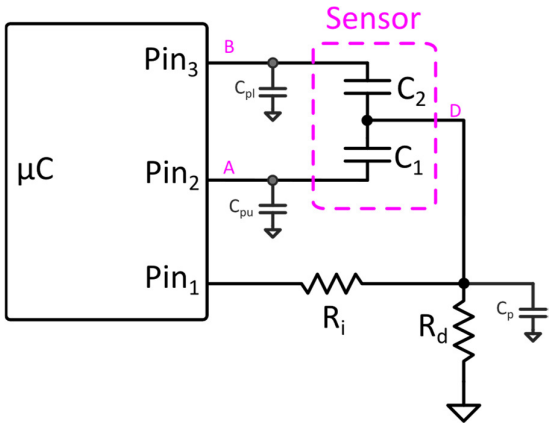


Figure 2.18 Direct microcontroller-based interface [27].

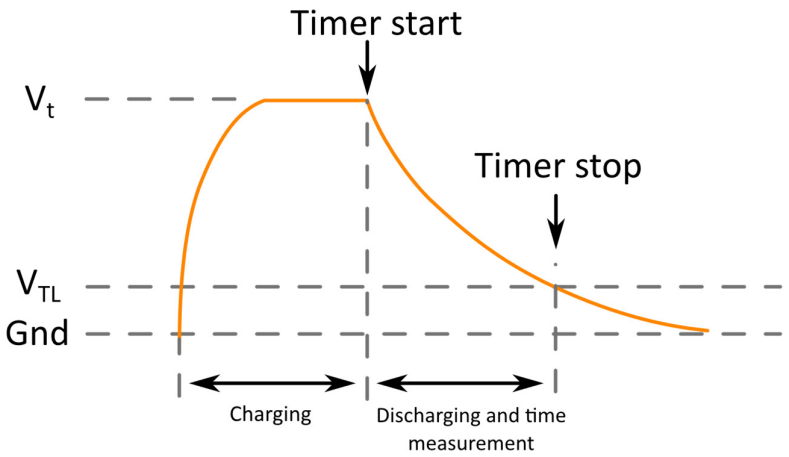


Figure 2.19 Voltage at node 1 during the charge and discharge phases [27].

The procedure described so far is carried out three times, and during each time pin 2 and pin 3 assume a different status. The first measurement is performed by outputting a logical 0 (gnd) on pin 2, while leaving pin 3 as a high impedance. The total capacitance given by this configuration is:

$$C_{t,1} = C_p + C_1 + \frac{C_2 C_{pl}}{C_2 + C_{pl}} \tag{2.42}$$

The discharge time is given by:

$$T_1 = R_d C_{t,1} \ln\left(\frac{V_{dd}}{V_{TL}}\right) \tag{2.43}$$

During the second measurement, the state of pin 2 and pin 3 is inverted, therefore the former is set to high impedance, while the latter to zero. The total capacitance and discharge time can be calculated respectively as:

$$C_{t,2} = C_p + \frac{C_1 C_{pu}}{C_1 + C_{pu}} + C_2 \tag{2.44}$$

$$T_2 = R_d C_{t,2} \ln\left(\frac{V_{dd}}{V_{TL}}\right) \tag{2.45}$$

The last measurement is carried out with both pin 2 and pin 3 set to high impedance. Therefore we can write that:

$$C_{t,3} = C_p + \frac{C_1 C_{pu}}{C_1 + C_{pu}} + \frac{C_2 C_{pl}}{C_2 + C_{pl}} \tag{2.46}$$

$$T_3 = R_d C_{t,3} \ln\left(\frac{V_{dd}}{V_{TL}}\right) \tag{2.47}$$

Once these three steps are concluded, the microcontroller performs the following operations to evaluate the sensor:

$$x = \frac{T_1 - T_2}{T_1 + T_2 + T_3} \tag{2.48}$$

Indeed, by substituting Eq. 2.43, Eq. 2.45 and Eq. 2.47 into Eq. 2.48 we can write:

$$x = \frac{C_1\left(1 + \frac{C_{pl}}{C_2}\right) - C_2\left(1 + \frac{C_{pu}}{C_1}\right)}{C_1\left(1 + \frac{C_{pl}}{C_2}\right) + C_2\left(1 + \frac{C_{pu}}{C_1}\right)} \tag{2.49}$$

As visible, the Eq. 2.49 is independent from V_{dd}, V_{TL} and R_d and, therefore, the interface is insensitive to variations in these parameters. It is also noticeable that the capacitance C_p does not affect the readout, while C_{pl} and C_{pu} do not constitute an error source only if C_2 and C_1 are much greater than them, making the interface unsuitable for low baseline sensors.

3 AUTOBALANCED BRIDGE, SYNCHRONOUS DEMODULATION BASED DIFFERENTIAL CAPACITIVE SENSOR INTERFACES

In this chapter it is presented how, during these years of Ph.D., we have applied the autobalanced technique in a impedance bridge to the readout of a differential capacitive sensor.

The reason that brought us to try and use this technique with differential capacitive sensors is that it allows to expand the performances of a basic bridge structure, i.e. high accuracy, high common mode disturbs rejection and excellent resolution making it suitable for unknown baseline sensors evaluation (uncalibrated interface) and allowing it to host widely variable sensors (for instance hyperbolic differential capacitance sensors, that corresponds to consider a wider range of capacitive values).

After an introduction about the working principles of the autobalanced bridge technique, in the first part we will show a non-linear readout circuit, as well as its linearization. In the second part, it is shown how we developed a methodology based

on a secondary feedback loop that, working as a parallel structure with respect to the actual interface, can be employed in this scenario to mitigate the effects of parasitic capacitances.

3.1 The autobalanced bridge

Fig. 3.1 shows a simple impedances bridge, excited by a sinusoidal reference voltage having an amplitude equal to V_{ref}. The equations that define the balance condition in such a structure are, as known:

$$\begin{cases} |\boldsymbol{Z_1}||\boldsymbol{Z_3}| = |\boldsymbol{Z_2}||\boldsymbol{Z_s}| \\ <\boldsymbol{Z_1}> + <\boldsymbol{Z_3}> = <\boldsymbol{Z_2}> + <\boldsymbol{Z_s}> \end{cases} \tag{3.1}$$

where the upper and the lower identities indicate the balance condition for the magnitude and the phase (indicated as $<\cdot>$) of the impedances, respectively.

Once that Eq. 3.1 is verified, the bridge stays at the balance condition and the output voltage is equal to zero:

$$\boldsymbol{V_{out} = V_a - V_b = 0} \tag{3.2}$$

From a designer perspective however, a sensible solution to achieve this condition, disregarding for a moment the phase constraints, is to set all the elements equal in magnitude. Indeed, by doing this, it is ensured that the amplitude of the signals V_a and V_b at each bridge branch, at the steady state, is at half of the reference voltage amplitude V_{ref}. This ensures to have the maximum readout dynamic range (see Fig. 3.2).

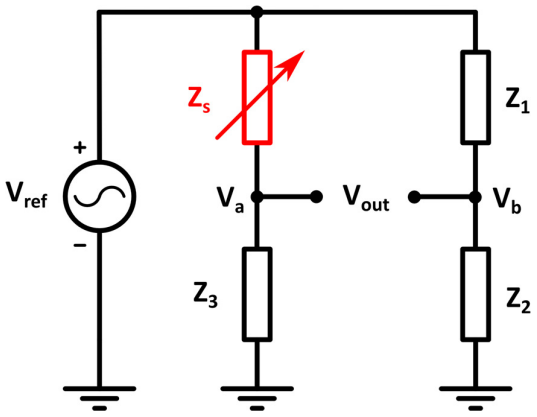


Figure 3.1 Generic impedance bridge.

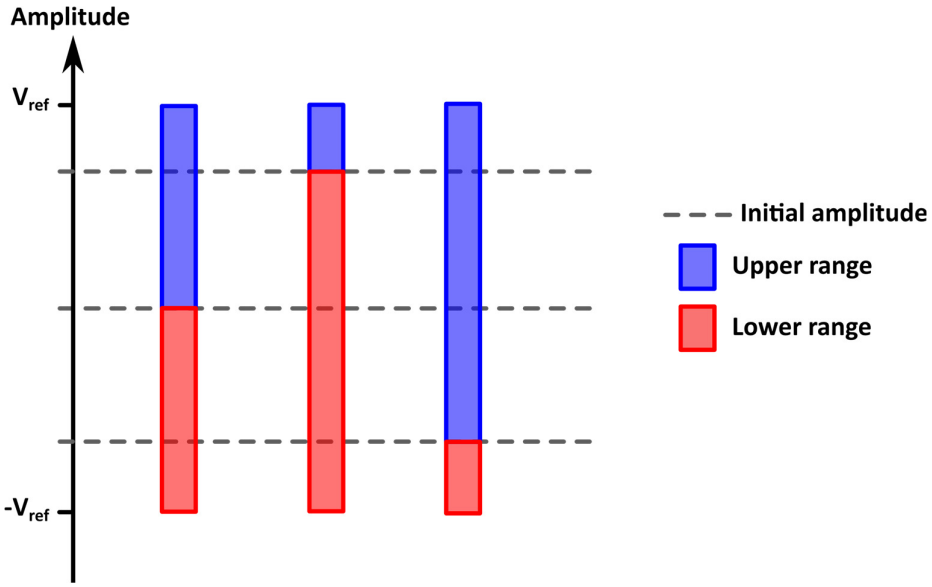


Figure 3.2 Dynamic ranges available at different values of impedances: all equal value (left); Z3<Zs and Z2<Z1 (center); Z3>Zs and Z2>Z1 (right).

Then, it evidences two issues: first, to implement the condition coming from the previous lines, it is fundamental the knowledge of the sensor baseline, from which it is possible to choose the other bridge components. This means that in order to work adequately, the bridge has to undergo to a calibration phase. Note that sometimes shifting V_a and V_b to a value different from $V_{ref}/2$ is something wanted, for instance, if the sensor magnitude raises or lowers only. Nonetheless, it is required the knowledge of the sensor baseline.

The second issue is that even if properly calibrated, a bridge-based interface remains unsuitable for a largely variable measurand due to the fact that, being V_a or V_b (according to the position of the sensor) free to vary, if the sensor varies too much, the one or the other voltages inevitably saturates. Moreover, the actual differential amplifier that produces the difference between the voltages V_a and V_b must have tight constraints like for instance high input and output dynamic range, in order to perform an accurate readout at any conditions.

Adding the autobalance feature to the bridge [29-34] allows to mitigate all the aforementioned issues: the basic method to implement such a structure is to add some circuitry to the bridge so to implement a negative feedback, whose aim is to maintain V_a equal to V_b (and therefore V_{out} equal to zero) at any given measurand value.

Taking Fig. 3.3 as a reference, the bridge is balanced through a voltage controlled impedance that varies according to the sensor to maintain V_a fixed and equal to V_b. By doing so, as long as the voltage controlled impedance is capable of assuming the value that balances the bridge, it is possible to obtain the following advantages.

The first and very important one is that there is no need to know the sensor baseline, indeed the bridge, due to the negative feedback, self-calibrates to the reference voltage given by the fixed branch (V_b in Fig. 3.3) according to the values of Z_1 and Z_2, making the user able to perform the readout as long as the relationship between the control voltage and the voltage controlled impedance value is known (obviously). The second advantage is that the voltage V_a is fixed to the value of V_b (which in turn is fixed at the value desired by the designer), avoiding its saturation to one extreme of the supply voltage. In other words, the span of the sensor that the interface is capable of reading is determined by the variation of the voltage controlled impedance itself and not anymore by the voltage saturation. The actual topology of the bridge and how to implement a voltage controlled impedance depend on the designer and is going to be analyzed in the following pages. The remaining part of the feedback produces the voltage to drive the voltage controlled impedance, voltage that is also the actual output of the interface. Since that a synchronous demodulation process can be used to extract it from the difference (error signal) $V_a - V_b$, an autobalance bridge interface also enjoys the inherent advantages coming from that procedure (noise reduction and offset error mitigation).

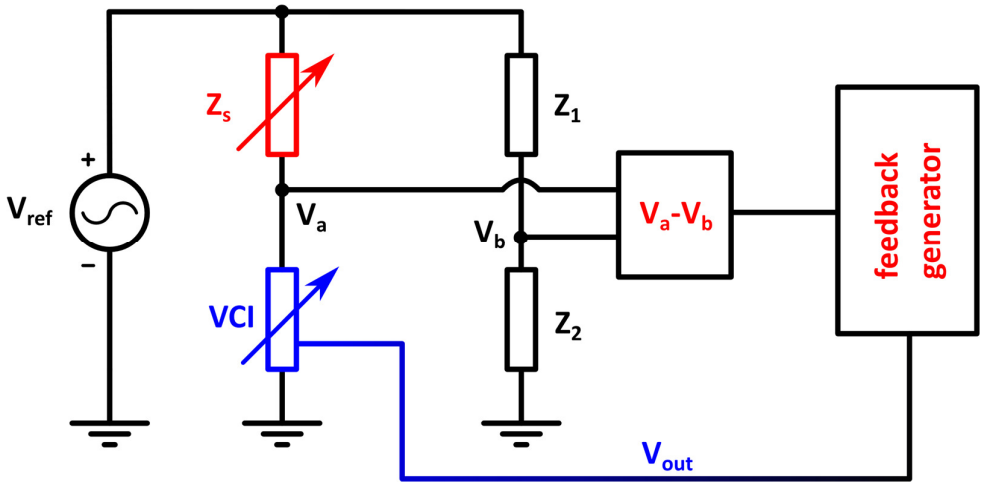


Figure 3.3 Block diagram of an autobalanced bridge.

3.2 Non-linear output interface

3.2.1 Discrete version

3.2.1.1 Theory of operation

The block diagram of the first proposed interface is shown in Fig. 3.4. As visible, the impedance bridge is arranged so that its left branch is formed by the differential capacitive sensor itself (C_1, C_2) while the right one by a fixed resistance (R) and a Voltage Controlled Resistance (VCR, named R_{vcr}) which is responsible for maintaining the bridge at its equilibrium by changing its value according to the differential capacitive sensor variation. This particular placement of the components allows to disregard the phase contribution in case of bridge unbalancing since both V_a and V_b are always in phase with V_{ref}.

The feedback path is composed by a differential amplifier, which allows to extract the difference between Va and Vb (ΔV) and by an analog multiplier which, together with the integrator, have the dual task of performing the synchronous demodulation and generating the actual output voltage V_{ctrl}, that, in turn, is also the driving signal for the VCR.

Differential capacitive variations change V_b value in the left branch of the bridge. As a consequence, through the feedback loop, V_{ctrl} level is varied and R_{vcr} changes its value so to force the bridge to be in equilibrium.

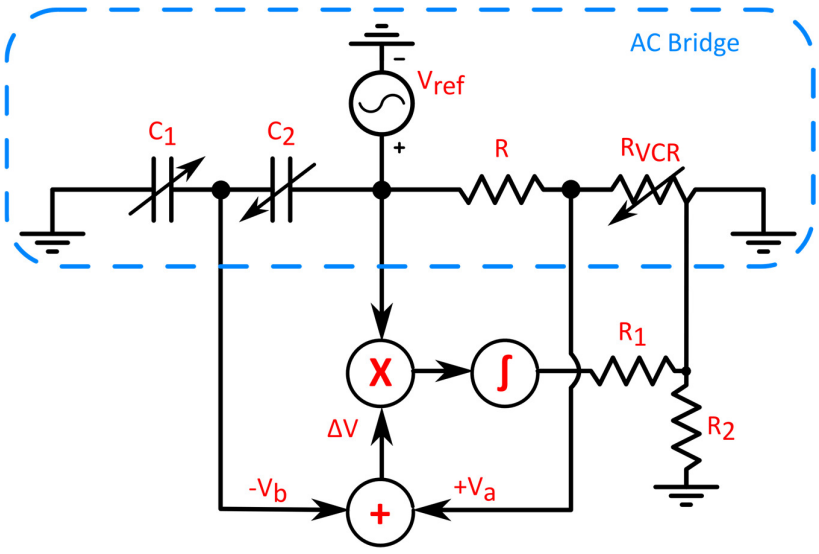


Figure 3.4 Autobalanced bridge interface proposed in [35].

*The work presented in this section was published by the authors in [35-36].

Noticeably, the signal ΔV, in a configuration like this, represents the "error signal" of the feedback architecture: the overall system indeed makes sure that it remains equal to zero.

To fully understand the working principle of the interface, its electronic implementation (Fig. 3.5) has to be analysed. A possible way to implement a voltage-controlled resistor is given by the use of an analog multiplier in the so-called Zhong configuration (see Fig. 3.6). Supposing to use an AD633 as multiplier device, the overall resistance vs. voltage relationship is given by:

$$\boldsymbol{R_{VCR} = \frac{10R_f}{10 - V_{ctrl}}} \tag{3.3}$$

The voltage divider R_1-R_2 is added to ensure that even if the VCR saturates (the bridge cannot reach the balance condition), the control voltage does not exceed the maximum value allowed by the VCR.

Voltages V_a and V_b can be evaluated as:

$$\boldsymbol{V_a = V_{ref} \frac{R_{VCR}}{R + R_{VCR}}} \tag{3.4}$$

$$\boldsymbol{V_b = V_{ref} \frac{\frac{1}{sC_2}}{\frac{1}{sC_1} + \frac{1}{sC_2}} = V_{ref} \frac{C_1}{C_1 + C_2}} \tag{3.5}$$

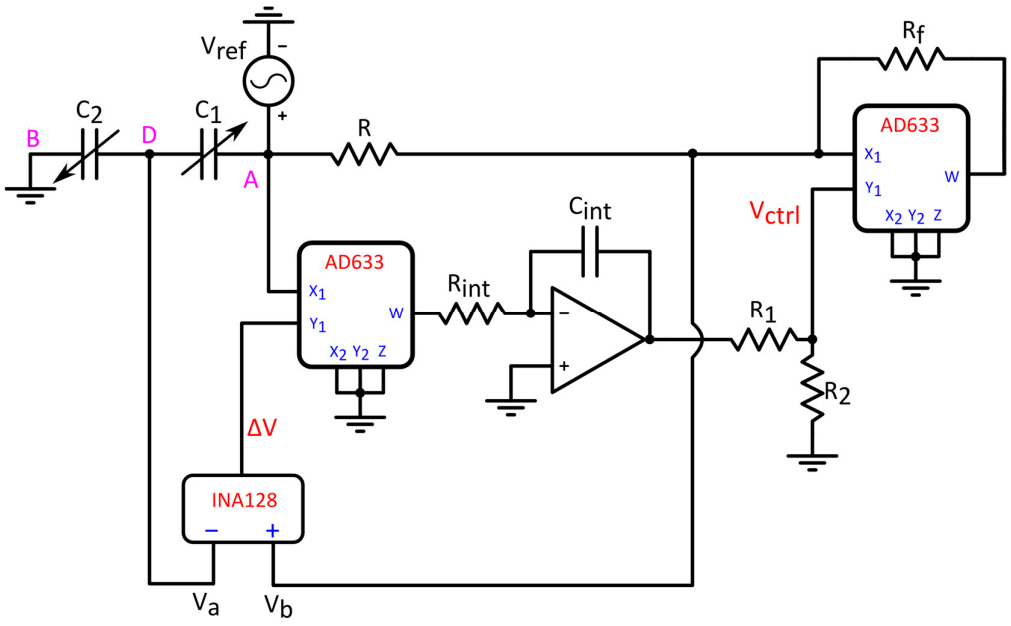


Figure 3.5 Circuital diagram of the interface analysed in [35].

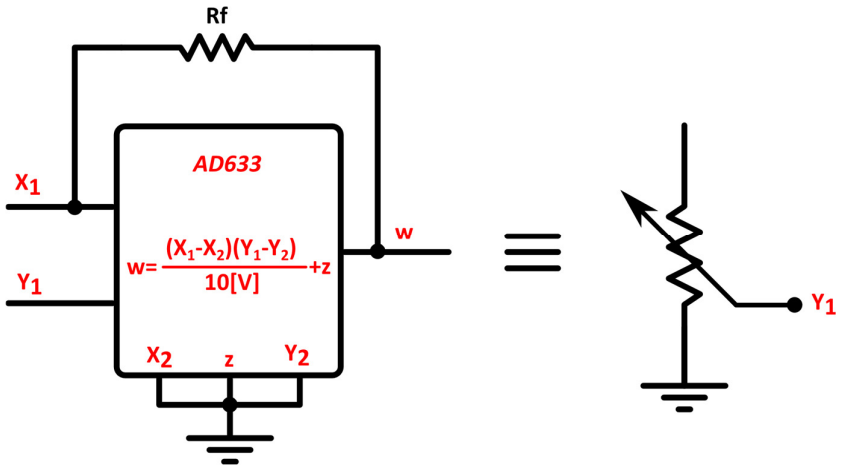


Figure 3.6 VCR implemented by means of a Zhong configuration.

By supposing to substitute to C_1 and C_2 their linear parametrization (Eq. 1.11), it is possible to evaluate the difference ΔV between V_a and V_b as:

$$\Delta V = V_{ref}\left(\frac{R_{VCR}}{R + R_{VCR}} - \frac{1+x}{2}\right) \tag{3.6}$$

Substituting Eq. 3.3 into Eq. 3.6 we have:

$$\Delta V = V_{ref}\left(\frac{10}{10 - V_{ctrl}} - \frac{1+x}{2}\right) \tag{3.7}$$

It is finally possible to manipulate Eq. 3.7 obtaining the following expression of the x parameter as a function of V_{ref}:

$$x = \frac{V_{ctrl}}{20 - V_{ctrl}} - 2\frac{\Delta V}{V_{ref}} \tag{3.8}$$

The equation above is valid for the full range of x variation ($\pm$100 % even if the VCR saturates), indeed it expresses the value of the measurand as a function of ΔV as well. If the VCR is able to guarantee the balance of the bridge, the equation can be reduced to the first term:

$$x = \frac{V_{ctrl}}{20 - V_{ctrl}} \tag{3.9}$$

From Eq. 3.9, it is evident how x can be easily determined only by reading V_{ctrl}. The overall readout speed depends on the settling time of the loop, which, in turn, is determined by the demodulation section. Since it is also the feedback controller, it has to be designed to fulfil the residual ripple constraints on the output signal.

3.2.1.2 Simulation and measurement results

The following values have been considered for the measurement setup: C_{bl}= 400 pF, R= 33 kΩ, R_1 = 2.7 kΩ, R_2=5.6 kΩ, R_{int} = 200 kΩ and C_{in}=2 nF .

The measurand x is determined by reading two values: V_{ctrl} in the autobalancing range (where the bridge is in equilibrium and ΔV=0) and ΔV in "out-of-range" (where V_{ctrl} is at saturation value ± 9.65 V and ΔV is not zero) as acknowledged by Eq. 3.8. Fig. 3.7 depicts this behavior, explicitly indicating the autobalancing boundaries for the configuration given in Fig. 3.5. As previously stated, in the autobalancing range it is possible to use Eq. 3.9 to determine x through the reading of only V_{ctrl} value.

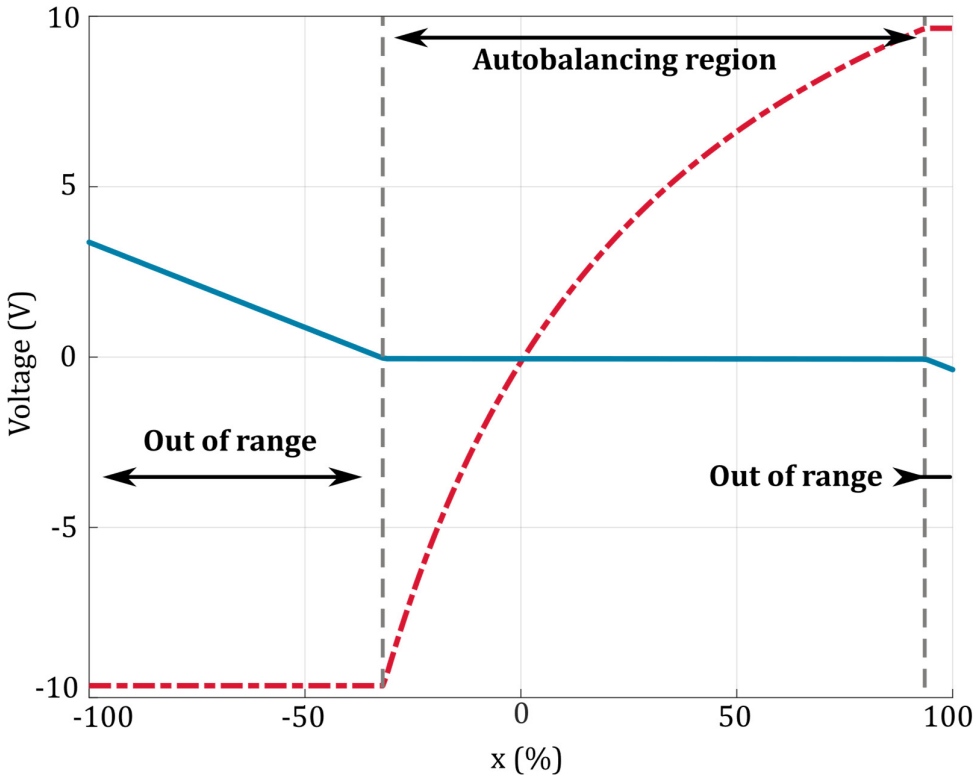


Figure 3.7 Vctrl and ΔV behaviors vs x: simulated results.

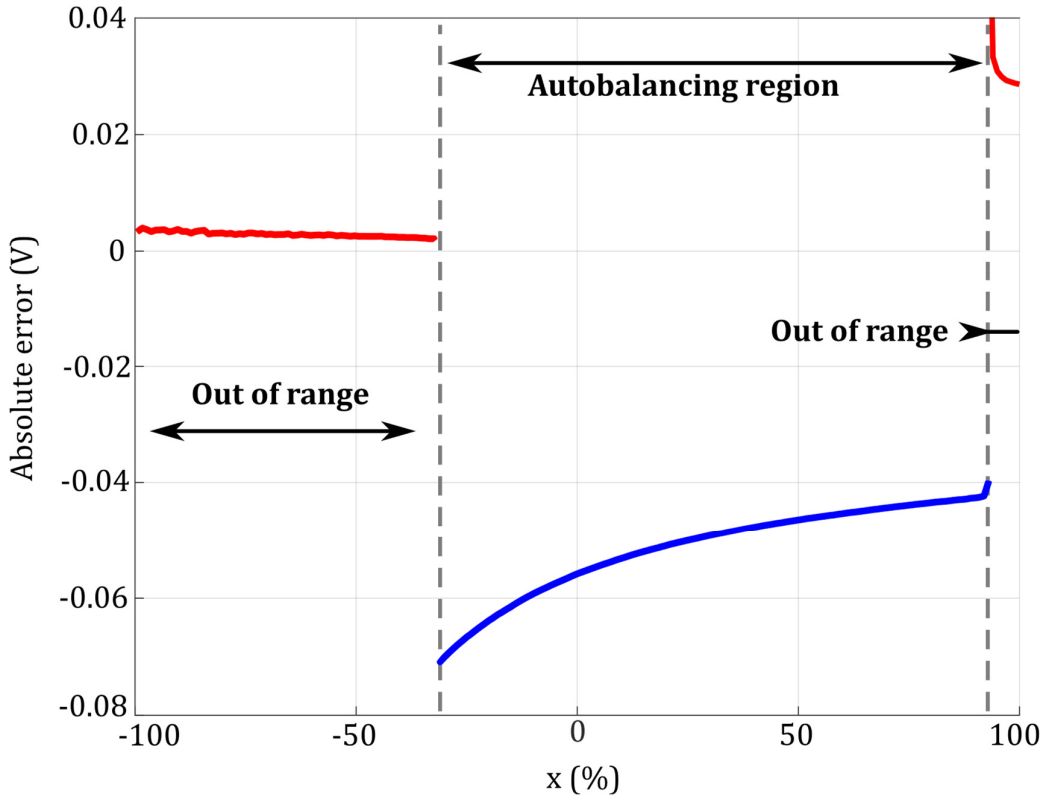


Figure 3.8 Absolute error in "autobalancing" interval and "out-of-range" vs. x%: theoretical vs. simulated results.

The absolute error (defined as in [37]) between theory and simulation vs. x is shown in Fig. 3.8. Its absolute value is lower than 0.07 V in the worst case. Experimental tests have been conducted on a discrete element board, demonstrating the circuit capability to follow the capacitive sensor variations in a full estimation range, as shown in Fig. 3.9. In fact, the percentage error, defined, again, as in [37], is lower than 0.45 %, as visible in Fig. 3.10. A comparison of the interface results, with respect to other solutions reported in the literature, is presented in Table I. The here proposed circuit shows a good accuracy with respect to other approaches, as a peculiarity coming from the closed loop, bridge based approach described in this section.

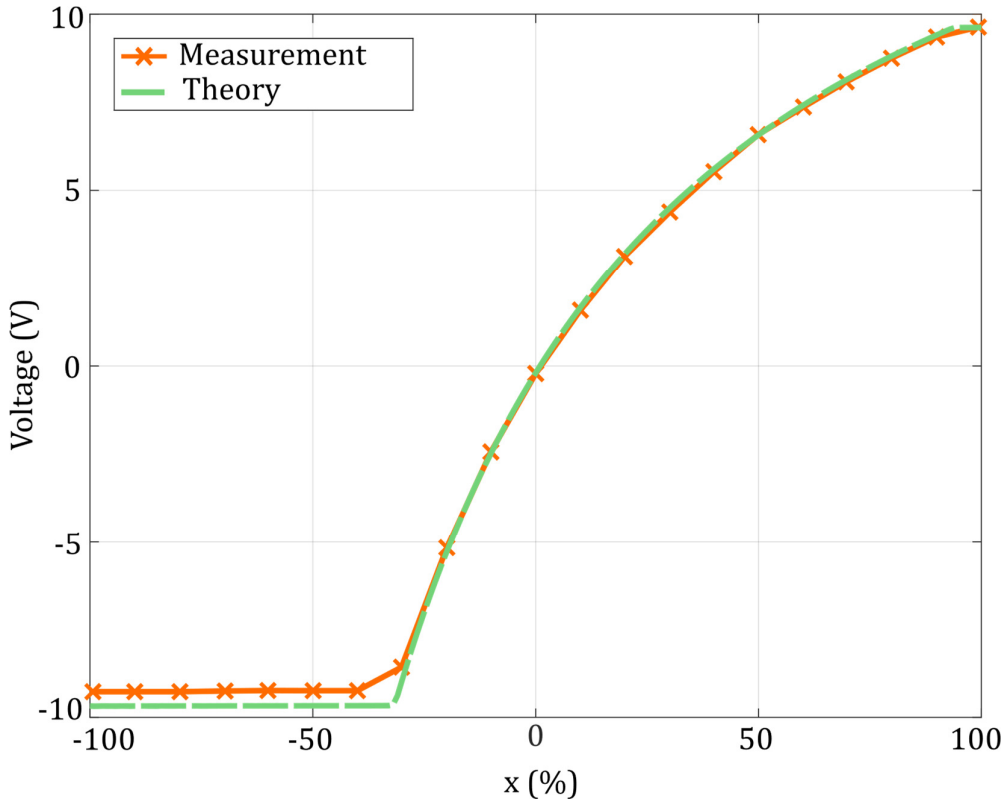


Figure 3.9 Vctrl behavior vs x: theoretical and experimental results

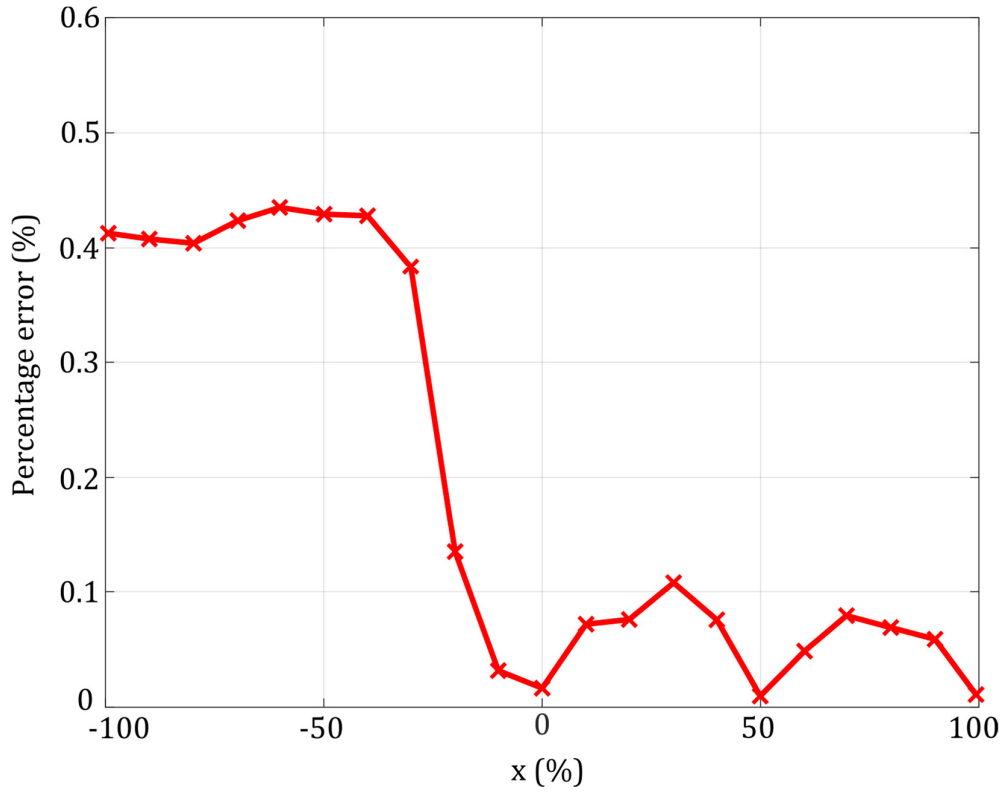


Figure 3.10 Percentage relative error vs. x: theoretical vs. experimental result

Table I Comparison table.

Ref.	Capacitance value[F]	Approach	Circuit topology	Accuracy (error)
[16]	500 p (±50%)	C to V	Discrete	± 0.03 %
[23]	20p (±120%)	C to V	Discrete	1.5 mV
[38]	400 p (±50%)	C to T	Discrete	0.9 %
[39]	200-1200 p	C to V	Discrete	< 6%
[40]	n. a.	C to V	Discrete	10 μV
[41]	25-840 n (±100%)	C to V	Discrete	< 10 %
This work	400 p (±100%)	C to V	Discrete	< 0.45 %

3.2.2 Integrated version

3.2.2.1 Theory of operation

The integrated version of the circuit proposed in the previous paragraph can be easily implemented by using a MOSFET working in linear region as a VCR as shown in Fig. 3.11. Differently from the discrete solution, as visible, it is explicitly put in evidence the DC component of the bridge. Indeed, bridge biasing (V_{bridge}) and resistor R have to be designed to allow the MOS VCR to work in linear region, ideally throughout the entire load line of the transistor, so to maximize the auto-balance range of the interface. It is also possible to suitably choose the transistor dimensions, particularly increasing its length so to guarantee a wider linear region.

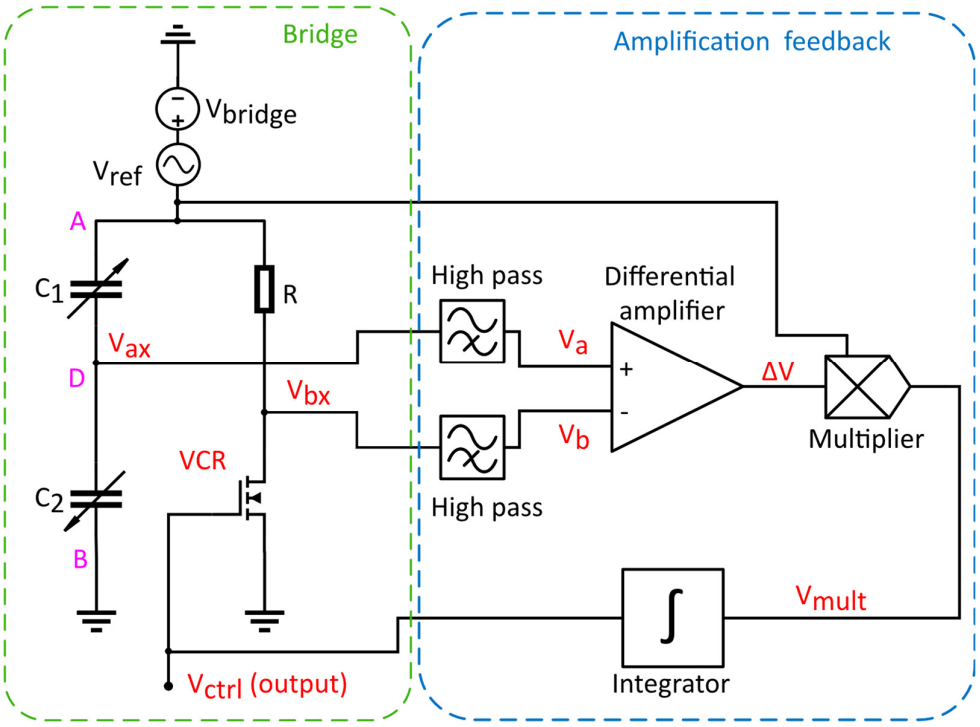


Figure 3.11 Using a mosfets in linear region as a VCR [42]

High pass filters have been also added at the bridge output (refer to Fig. 3.11) so to avoid the DC of the bridge to influence the following stage biasing voltage.

Since the steady state conditions imposed for the discrete interface are still valid, it is worth starting back the analysis from Eq. 3.6. Moreover, considering that the drain-source resistance of a MOSFET working in linear region is equal to:

$$R_{ds} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th} - V_{ds}\right)} \tag{3.10}$$

it is possible to evaluate x as follows:

$$x = \frac{1 - R\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th} - V_{ds}\right)}{1 + R\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th} - V_{ds}\right)} \tag{3.11}$$

Both in Eq. 3.10 and Eq. 3.11, μ_n represents the mobility of electrons in a silicon medium (supposing to use an NMOS), C_{ox} is the capacitance per unit of area for the technology used, W/L the form factor of the transistor and V_{th} is the threshold voltage of the MOSFETS for the specific technology.

*The work presented in this section was published by the authors in [42].

The OTA configuration, reported in Fig. 3.12, has been employed as active block in the whole design of the interface. It consists of a two stage architecture: the input stage, as shown in Fig. 3.12, is a symmetrical OTA. By choosing a proper W/L ratio for transistors Q_5 and Q_6 (B parameter) with respect to Q_3 and Q_4, it is possible to obtain higher slew-rate and GBW values as well as very low offset. In order to increase the total gain, an output stage has been added, formed by a cascoded inverter architecture, which increases the output resistance and consequently the voltage gain of the whole amplifier. Frequency compensation has been performed by means of pole-zero compensation, adding a resistor-capacitor series (R_x, C_x) circuit between V_y and V_{out}. Transistor dimensions (referred to the AMS 0.35 µm technology) are shown in Table II, while main OTA performances are listed in Table III.

Table II OTA transistor dimensions.

Transistor name	*W(µm)*	*L(µm)*
$Q_{1,2}$ *(NMOS)*	200	1
$Q_{3,4}$ *(PMOS)*	2	2
$Q_{5,6}$ *(PMOS)*	30	6
$Q_{7,8}$ *(NMOS)*	50	2
$Q_{9,10}$ *(NMOS)*	5	1
$Q_{11,12}$ *(PMOS)*	10	1

Table III Amplifier parameters.

Feature	*Value*
Power Supply	±1.5V
Open Loop DC gain	100dB
Power consumption	190µW
GainBandWidth	52MHz
Slew Rate	33V/µs
Rx, Cx	40kΩ, 1pF

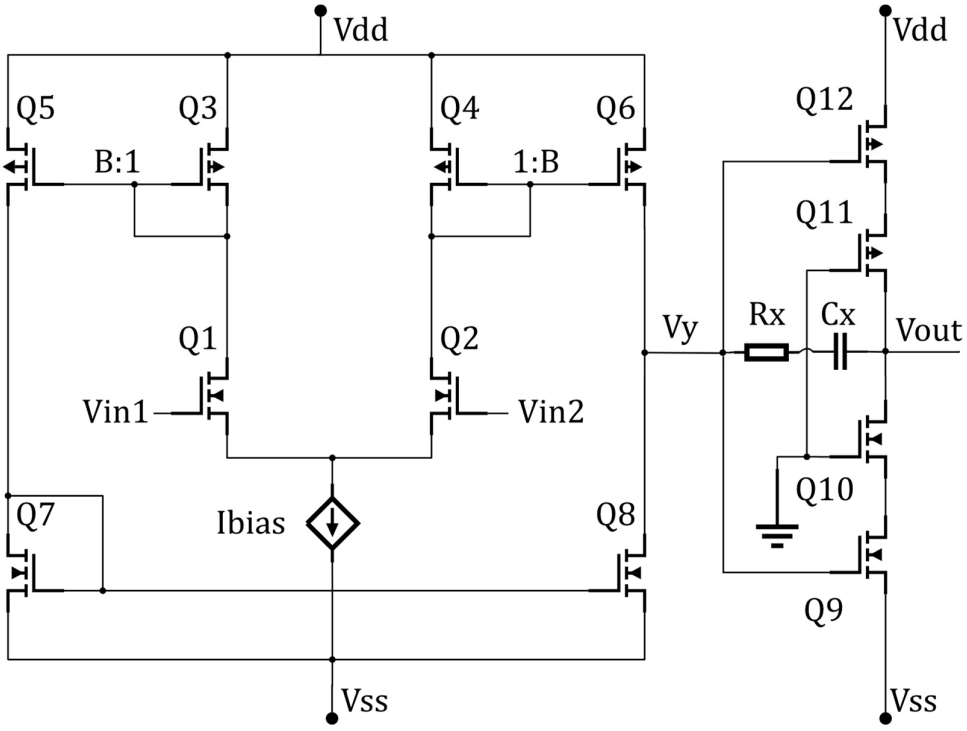


Figure 3.12 Dual stage, symmetrical operational transconductance amplifier.

Concerning the analog multiplier, its core, shown in Fig. 3.13a, is based on the Flipped Voltage Follower (FVF) architecture [43]. Being a differential output architecture, the conversion to single ended output is achieved by using another instrumentation amplifier (gain=32dB) applied to the signals V_{m1} and V_{m2}. An input biasing stage (shown in Fig. 3.13b) ensures that transistors Q_{21} to Q_{24}, as well as Q_{25}, Q_{26}, Q_{28}, Q_{29} are biased in saturation region. This biasing block exploits the voltage translation given by a flipped voltage follower, and, suitably dimensioning a cascade of PMOS FVF and NMOS FVF, adjusts the offset to the desired one. It is important to notice that this biasing method ensures a low output impedance, while keeping an extremely high input impedance. Moreover, by opportunely sizing PMOS and NMOS transistors, it is possible to cover an almost full dynamic range of translation levels. Table IV shows multiplier transistor sizes. These choices guarantee an output linearity that is extended for input signals up to $250mV_{pp}$.

Bridge resistor (named R in Fig. 3.11) and biasing voltage (V_{bridge}) are designed to allow the NMOS VCR to work in linear region as much as possible so to increase the auto-balance range of the interface. A too low V_{bridge} value forces V_{ctrl} (i.e. V_{gs}) to be close to transistor threshold voltage ($V_{th} \approx 0.46V$) when no sensor capacitance

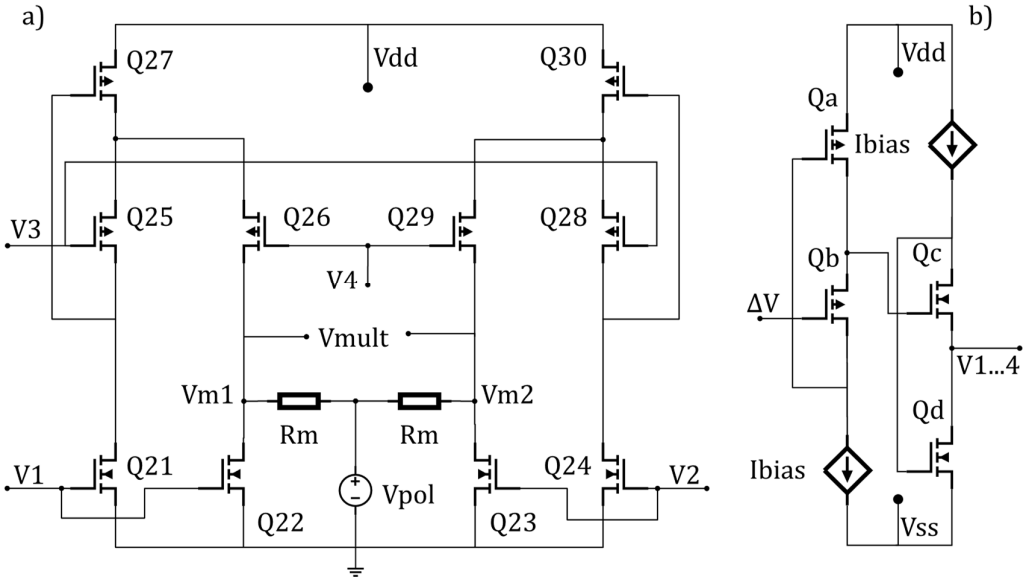


Figure 3.13 a) Multiplier core, b) multiplier biasing circuit

variation occurs, thus reducing the lower V_{ctrl} dynamic. On the contrary, a high V_{bridge} value forces V_{ctrl} to be too high, this means that the transistor would be in saturation for a small sensor variation, so reducing upper V_{ctrl} dynamic.

Table IV Multiplier transistor dimensions and parameter values.

Transistor name			***W(µm)***		***L(µm)***			
$Q_{21,22,23,24}$ *(NMOS)*			1		1			
$Q_{25,26,28,29}$ *(PMOS)*			50		4			
$Q_{27,30}$ *(PMOS)*			300		4			
Input	***Q_a (µm)***		***Q_b (µm)***		***Q_c (µm)***		***Q_d (µm)***	
	W	*L*	*W*	*L*	*W*	*L*	*W*	*L*
V1, V2	0.35	1	1.13	0.35	Not Used	Not Used	Not Used	Not Used
V3, V4	0.35	1	1.8	0.35	50	0.35	0.35	10

Also R has been designed with a suitable trade-off in its resistance value. The best combination found for these two parameters is: V_{bridge}=300mV; R=10kΩ. Transistor width has been chosen equal to 100μm while its length is equal to 10 μm. A long length channel transistor has been adopted since short length channel ones tend to reach saturation region before the usual condition $V_{ds} > V_{gs} - V_{th}$. These setup conditions allow the transistor to have a linear behavior within almost the whole V_{gs} (i.e. V_{ctrl}) available range: from 0.6V (a little higher than transistor threshold voltage) to 1.5V (supply voltage). Fig. 3.14 shows that transistor equivalent resistance, extracted from simulations, matches the R_{ds} deriving from linear region theory well enough. This confirms that the VCR is properly working linearly in the aforementioned voltage range.

3.2.2.2 Simulation results

Fig. 3.15 shows the interface input-output characteristic, determined after a variation in the sensor capacitance, while the steady state value of V_{ctrl} has been read. A comparison of simulation results with theory (Eq. 3.11) is also shown. The absolute error remains lower than 30 mV in a $\pm 50\%$ range of x variations. In the rightmost area of the plot as well as leftmost area the two curves diverge. In the first case, the error is due to the fact that VCR transistor is not anymore in linear region but in saturation, since it shows a high V_{ds} and a low V_{gs}. In the second case, the error depends on the fact that Eq. 3.11 does not take into account the maximum supply value (1.5V). Moreover, the total autobalance range covers a large percentage of the measurand variations ($\pm 90\%$). However, due to the previously justified mismatches, it is desirable to limit the total useful range to the $\pm 50\%$ interval.

Fig. 3.16 shows the interface response with respect to a train of capacitance variations. It is possible to notice that settling time varies from 1ms up to 6ms and depends mostly on both the integrator design (which performs the feedback) and on the amplitude of sensor variation. Table V shows a performance comparison with respect to other capacitive sensor interfaces presented in the literature.

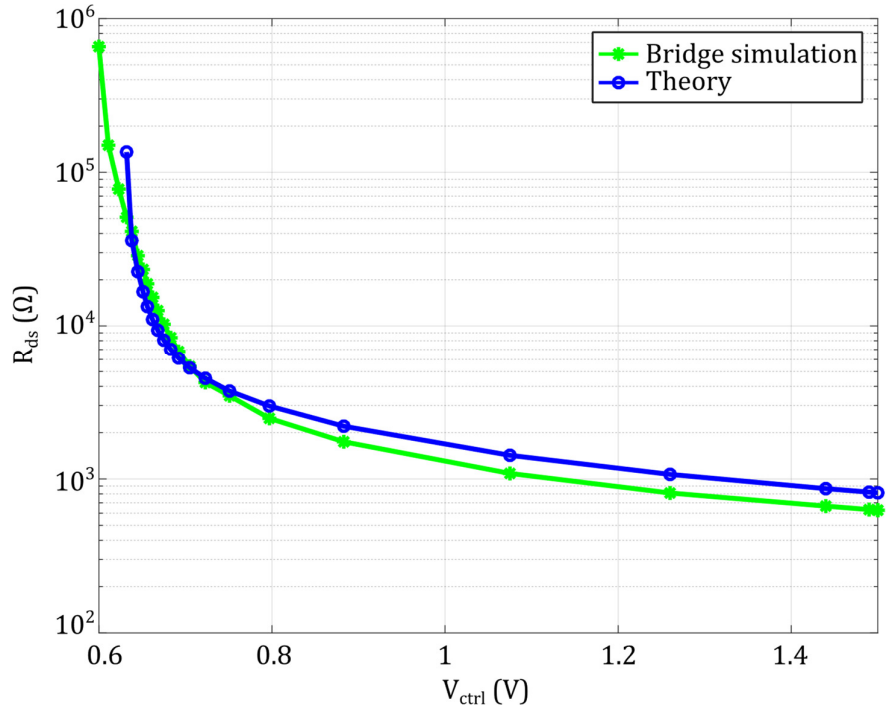


Figure 3.14 Simulated equivalent resistances vs. linear region Rds theory.

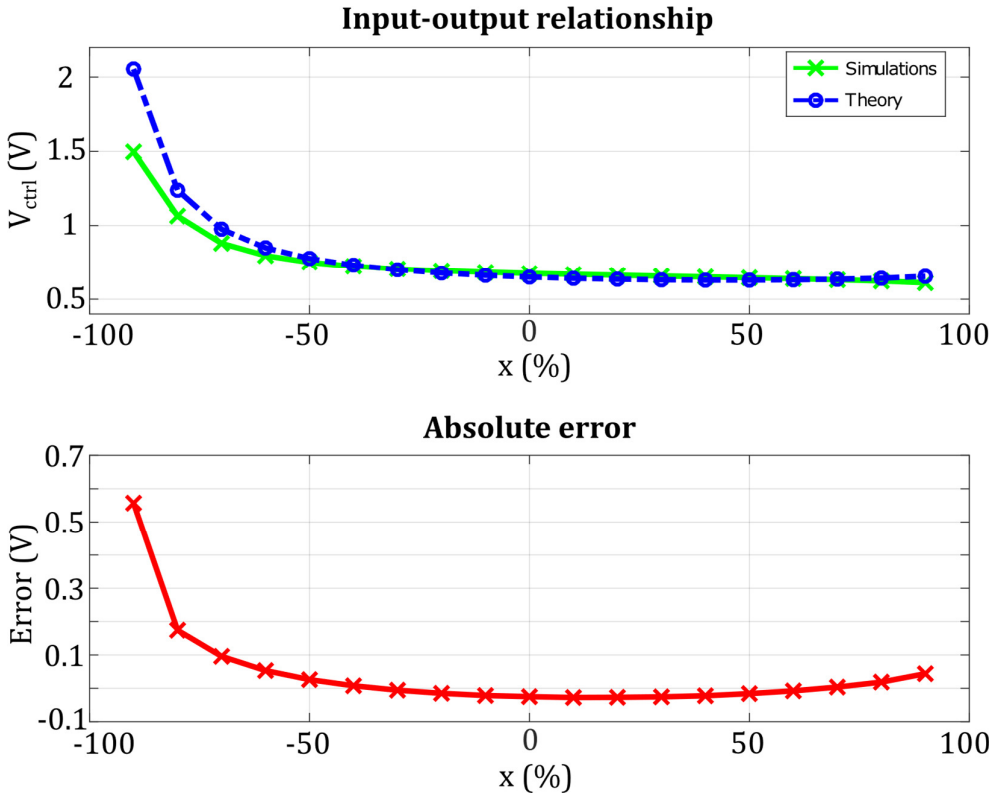


Figure 3.15 Interface static performances.

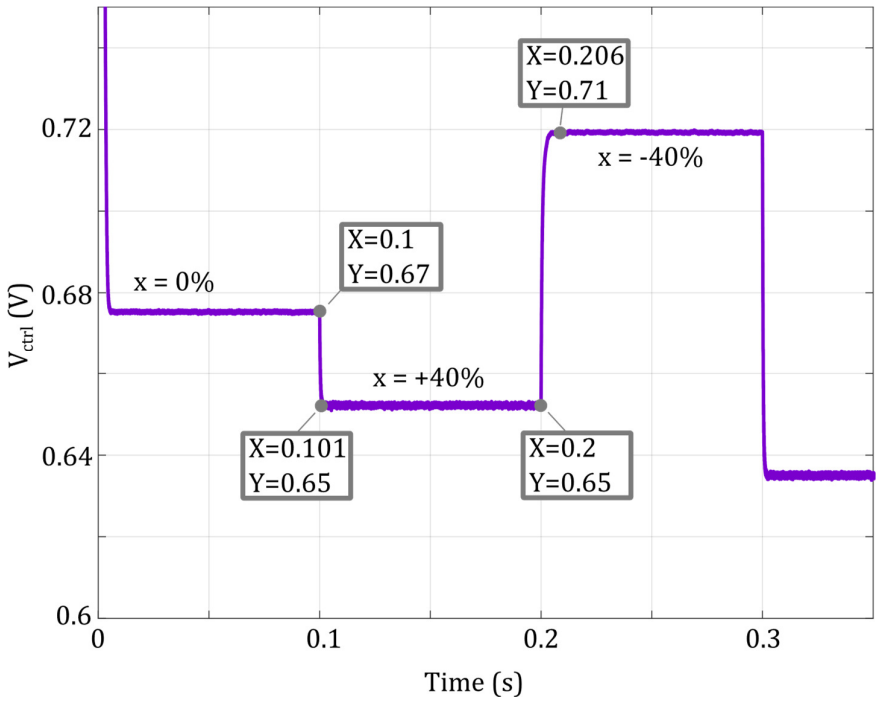


Figure 3.16 Interface dynamic performances.

Table V Comparison table

	[44]	*[45]*	*[46]*	*[47]*	*Section 3.2.1*	*This work*
Capacitive range	5 pF ±10%	690 pF	160 fF	100 pF- 2 nF	400 pF ±40%	100 pF ±50%
Topology	-	CSA*	SC**	Bridge	Bridge	Bridge
Technology	Integr. 180nm	Integr. 90nm	Integr. 350nm	Discr.	Discr.	Integr. 350nm
Supply	1.8 V	1.2 V	±1.65 V	±15 V	±15 V	±1.5 V
Power cons.	10 mW	4 mW	0.6 mW	-	-	< 4mW
Accuracy	-	0.07%	20 mV	< 6 %	< 0.45%	30 mV
Data source***	M	M	S+M	M	S+M	S

*Charge Sensitive Amplifiers ** Switched-capacitor structure *** M = Measurements, S = Simulations

3.2.3 Discussion

Although simulated and experimental results have confirmed the theoretical expectations, allowing the capacitance estimation in its the full variations range with a good accuracy, both the discrete and the integrated versions of the interface respond to a measurand variation in a highly non-linear fashion, which obviously means that the sensitivity of the proposals depends on the actual measurand amplitude. Moreover, in both the cases, the VCR is not capable of maintaining the balance condition through the entire input full-range.

3.3 Linear output interface

In this section we present a new architecture that overcomes the aforementioned limitations of linearity and autobalancing region limitation.

3.3.1 Discrete version

3.3.1.1 Theory of operation

The basic idea is here described: as stated before, the autobalancing strategy can be considered as a negative feedback-based system, whose aim is to minimize or null a certain error signal with the advantage that the input-output relationship only depends on the feedback gain. According to well-known results of the automatic control theory, such a nulling effect can be obtained using a very high open loop gain and integral control strategy. This technique can be used for bandpass signals as well (i.e., when signals of interest are phasors), as shown in Fig. 3.5 and Fig. 3.11, but in order to use the integral control strategy, a baseband signal has to be generated. The solution here described uses therefore a synchronous demodulator in the forward path but unlike Fig. 3.5 and Fig. 3.11 (schematized in Fig. 3.17) introduces a modulator in the feedback path, as depicted in Fig. 3.18, allowing to move from bandpass to baseband domains and vice versa. The intrinsic advantage is that a regular integral control strategy can still be applied on the baseband signal, whereas the VCR action only modifies the amplitude (see Fig. 3.19) of the signal V_b, therefore generating a linear relationship between the control voltage V_{ctrl} and the x parameter. When integral control is applied and both the forward (i.e., $A = G \cdot A_{mod} \cdot s^{-1}$ in Laplace domain) and feedback ($B = A_{dem}$) paths are linear, the closed loop transfer function is given by Eq. 3.12.

*The work presented in this section was published by the authors in [48].

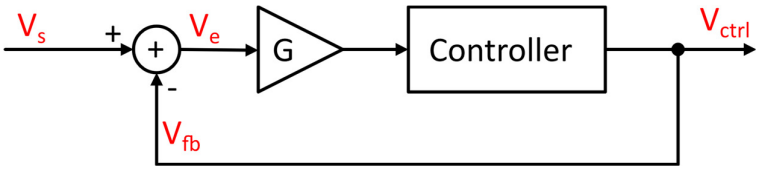


Figure 3.17 Schematic representation of the generic autobalancing system.

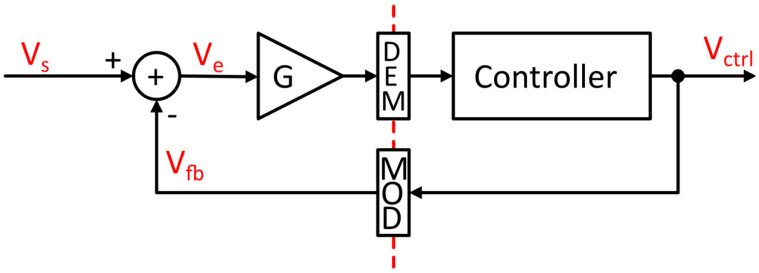


Figure 3.18 Schematic representation of the baseband vs bandpass signals in the interface analysed in [48].

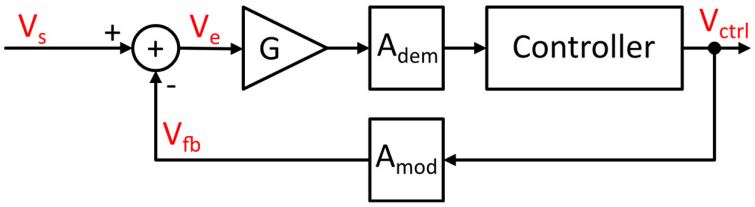


Figure 3.19 Simplification of the analysed interface feedback circuit in the time domain.

$$\boldsymbol{H(s) = \frac{A \cdot \frac{1}{s}}{1 + A \cdot \frac{1}{s} \cdot B} = \frac{1}{B} \frac{1}{1 + s\frac{1}{A \cdot B}}} \qquad \textbf{(3.12)}$$

In other words, the system behaves as a first order low-pass filter whose cutoff angular frequency is $\omega_{C0} = A{\cdot}B$.

The whole interface circuit is shown in Fig. 3.20.

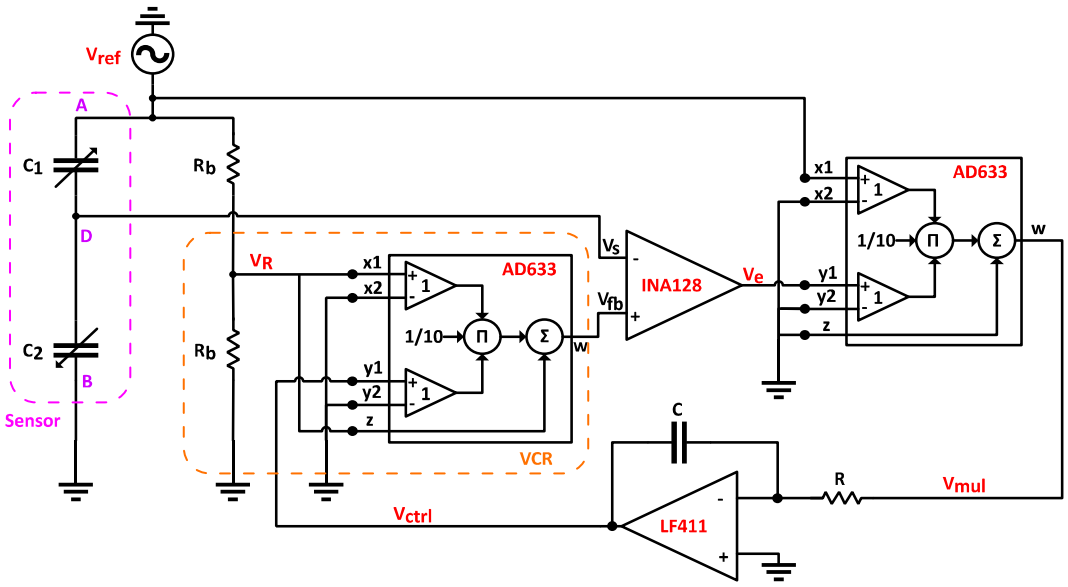


Figure 3.20 Schematic diagram of the proposed interface.

In order to calculate its input-output relationship, assumptions have been made on the actual analog multipliers used in the interface.

The sensor, represented by capacitors C_1 and C_2, constitutes the left branch of the bridge excited by the sinusoidal AC source V_{ref}. At the rest position ($x = 0$), the sensor output is:

$$V_s(t) = \frac{V_{ref}(t)}{2} = V_R(t) \tag{3.13}$$

The VCR in the right branch is controlled in order to generate the V_{fb} signal, following the V_S. The rightmost dashed box of Fig. 3.20 indicates the VCR actual implementation, based on fixed resistor R_b and an analog multiplier AD633.

The feedback signal summing node is implemented by an Instrumentation Amplifier, INA, specifically an INA128, providing buffering as well, being configured for a unitary gain. The synchronous demodulation of the error signal V_e is performed by using another AD633. The multiplier output V_{mul} can be computed as:

$$V_{mul}(t) = \frac{1}{10[V]} \frac{|V_{ref}||V_e|}{2} (1 - cos(2\omega_{ref} t)) \tag{3.14}$$

Signal V_{mul} feeds an inverting integrator V_{ctrl}, as calculated in Eq. 3.15. The final approximation holds when the residual ripple, due to the non-ideal behavior of the

integrator in removing unwanted high-frequency components of the demodulation process, is negligible. However, it can also be removed by further post-processing. The control voltage V_{ctrl} is given by:

$$\boldsymbol{V_{ctrl}(t) = -\frac{1}{RC}\frac{|V_{ref}|}{20[V]}\int |V_e|(1 - cos(2\omega_{ref}t))dt \cong} \\ \boldsymbol{\cong -\frac{1}{RC}\frac{|V_{ref}|}{20[V]}\int |V_e|dt} \tag{3.15}$$

Like for the previous solutions shown in the previous paragraphs, the low-pass behavior of the integrator minimizes the V_{mul} term at $2\omega_{ref}$ and the demodulation process is achieved without any additional low-pass filter.

Finally, the feedback signal V_{fb} is obtained modulating V_{ctrl} by means of another AD633:

$$\boldsymbol{V_{fb} = V_{ref}\left(\frac{1}{10[V]}V_{ctrl} + 1\right)} \tag{3.16}$$

The resulting R_{VCR} value is therefore evaluated as:

$$\boldsymbol{R_{VCR} = R_b\frac{10[V] + V_{ctrl}}{10[V] - V_{ctrl}}} \tag{3.17}$$

As previously stated, when the system is balanced, V_S equals V_{fb} thus the relationship between V_{ctrl} and x is described by the very simple relation:

$$\boldsymbol{V_{ctrl} = 10[V]x,\ \text{i.e. } x = \frac{1}{10[V]}V_{ctrl}} \tag{3.18}$$

Sensitivity $S_{Vctrl,x}$ with respect to x is constant and equal to 10 V. Its value could be modified acting on the gain of the feedback path.

3.3.1.2 Simulation results

Some preliminary simulations have been performed in the MATLAB/Simulink environment in order to evaluate the system dynamic behavior, having considered the first order model previously described (as in Fig. 3.21) in the equivalent phasor representation. In Fig. 3.21 the model is depicted, whereas in Fig. 3.22 simulation

outputs are shown when the measurand varies from the rest position $x = 0$ to $x =$ 90% and then down to x = −90%. Two different circuit configurations are considered, i.e.: 1) V_{ctrl1} @ C = 2 nF and R = 200 kΩ; 2) V_{ctrl2} @ C = 2 nF and R = 20 kΩ. In the former case, the cutoff angular frequency is $\omega_{CO1} \approx 104$ rad/s, whereas in the latter $\omega_{CO2} \approx 1040$ rad/s. The same circuit configurations have been used for PSpice simulations as well. Simulation outputs (shown in Fig. 3.23) perfectly match results provided by the simplified Simulink model, thus confirming that, when the sinusoidal excitation angular frequency is $\omega_{ref} = 2\pi \cdot 10\text{k}$ rad/s, and given the simulation conditions, non-idealities of components can be neglected, and overall system actually behaves as a low-pass filter.

It has to be highlighted that simulations start with different initial conditions, justifying the different behaviors between Fig. 3.22 and Fig. 3.23 in the first 50 ms of simulation.

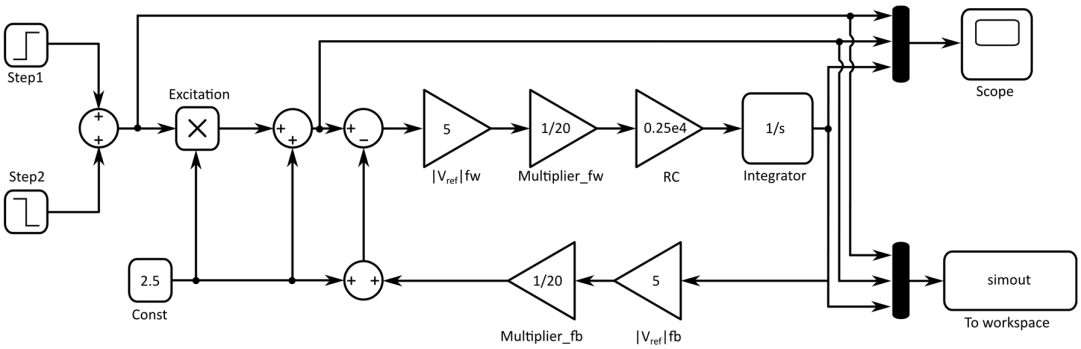


Figure 3.21 Simulink model of the proposed system.

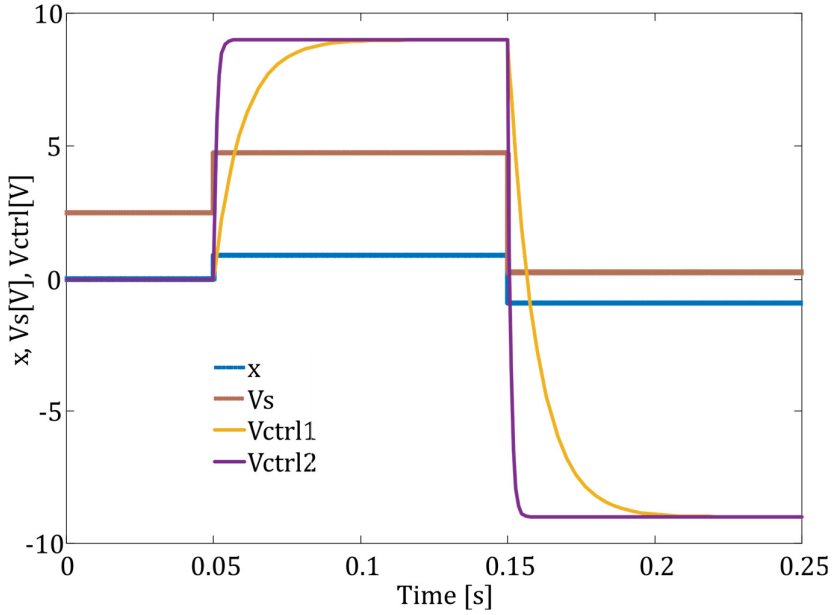


Figure 3.22 Simulink simulation results for different cutoff frequency (V_{ctrl1} @ ω_{C01} ≈ 104 rad/s, V_{ctrl2} @ ω_{C02} ≈ 1040 rad/s). The amplitude of the sinusoidal sensor output V_S is reported as a reference for comparison vs. x.

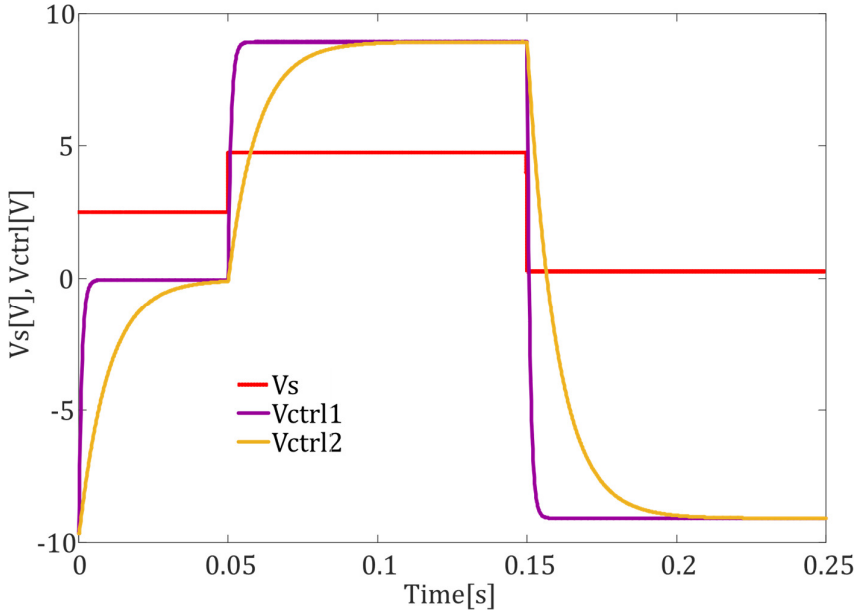


Figure 3.23 PSpice simulation results for different cutoff frequency (V_{ctrl1} @ R = 20 kΩ and C =2 nF, Vctrl2 @ R = 200 kΩ and C = 2 nF). The amplitude of the sinusoidal sensor output V_S is reported as a reference for comparison vs. x.

3.3.1.3 Measurement results

As previously stated, a real-world proof-of-concept prototype has been realized using discrete components. The board is shown in Fig. 3.24a.

In order to finely control equivalent measurand variations, the transducer behavior has been emulated by a set of C_{Si}, $i = 1...14$, i.e., fourteen capacitors connected in series, as shown in Fig. 3.24b. Such a configuration interface mimics the sensor behavior depicted in Fig. 1.11b (i.e., when the measurand influences the distance between plates). All the C_{Si} have the same nominal value $C_S \in [1, 2.2, 4.7, 10, 100]$ nF, so that variations in the value of the measurand have a resolution of $1/7$ in the useful range $x \in [-6/7, 6/7]$.

A set of programmable switches (based on solid-state relay) used for selecting the desired output is shown in Fig. 3.24b. In order to consider possible delays introduced by these switches, a dummy channel connected via a dummy switch is acquired as well, as a temporal reference signal. A digital multimeter (DMM, Agilent 34411A), has been employed for measuring the actual emulated sensor output; in that way, for each position of the cursor N, a more accurate indication of the actual measurand x, is obtained.

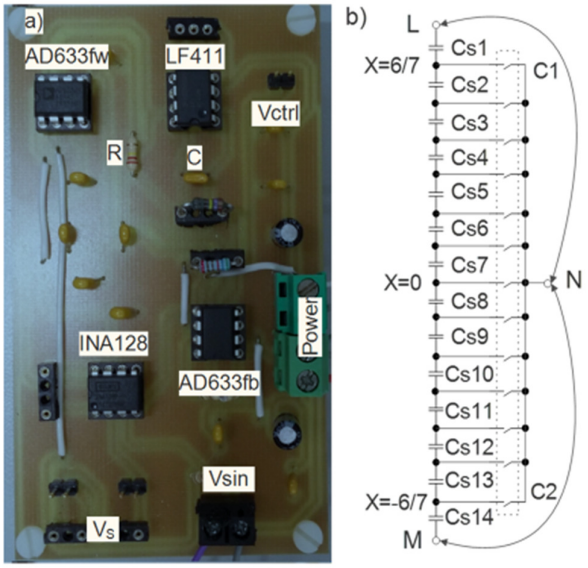


Figure 3.24 a) The PCB of the realized prototype. b) The differential capacitive sensor emulator; L, M and N refers to the scheme in Fig. 1.11b.

3.3.1.3.1 Resolution and linearity evaluation

Experimental tests of the circuit have been carried out using an automated test equipment exploiting National Instruments tools and a software purposely developed under the LabVIEW environment. The experimental setup is shown in Fig. 3.25. A NI Virtual Bench function generator has been employed for providing the excitation signal V_{ref}. Particularly, in agreement with the setup used in the simulations, the excitation signal has a $|V_{ref}| = 10$ V peak to peak amplitude and a $\omega_{ref} = 2\pi \cdot 10$k rad/s angular frequency (implicitly having null phase). The Virtual Bench also drives the bank of switches, using a digital output port. Conversely, the interface output V_{ctrl} reading has been performed by a National Instruments DAQ board NI-6110.

The choice is dictated by the simultaneous sampling capability, adopted for acquiring the analog signal of interest and digital driving signal of the reference dummy switch.

Firstly, static performance is evaluated, considering different measurand x values and acquiring the circuit output V_{ctrl} once it has reached a steady value. For each measurand $x \in$ [-6/7, 6/7], NOBS = 20 acquisitions of the V_{ctrl} output signal have been collected. In particular, each V_{ctrl} value is the average of NS = 125 kSa acquired using a sampling frequency fS = 25 kSa/s. From the average of the NOBS available observations, each one lasting TOBS = 5 s.

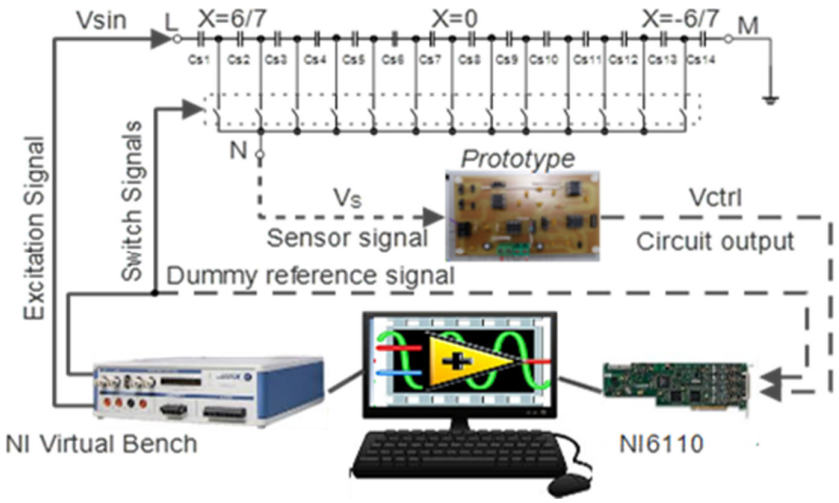


Figure 3.25 The experimental setup.

An estimated value $<x>$ of the measurand x has been obtained by means of Eq. 3.18, resulting in the calibration curve in Fig. 3.26; for this static characterization, we have chosen $C = 2$ nF and $R = 200$ kΩ. The maximum linearity error results in $e_{LIN\_\pm100\%,MAX} = [0.8, 0.7, 0.5, 0.6, 0.6]$%FS for CS ∈ [1, 2.2, 4.7, 10, 100] nF, respectively. If the useful range is limited to x ∈ [-3/7, 3/7], the maximum linearity error decreases down to $e_{LIN\_\pm50\%,MAX} = [0.4, 0.4, 0.3, 0.1, 0.1]$%FS for $C_S \in$ [1, 2.2, 4.7, 10, 100] nF, respectively. As expected, when smaller values of C_S are considered and parasitics have larger effects, non-linearity emerges. As previously highlighted, such a result is mainly imputable to parasitics in the discrete component circuit implementation. Integrating the circuit in a single IC can greatly improve the performance.

In order to evaluate the resolution, NOBS available observations for each reference measurand value x have been reckoned. As stated in the previous sub-section, the worst-case standard deviation is 0.05 and can be considered an indication of the actual resolution.

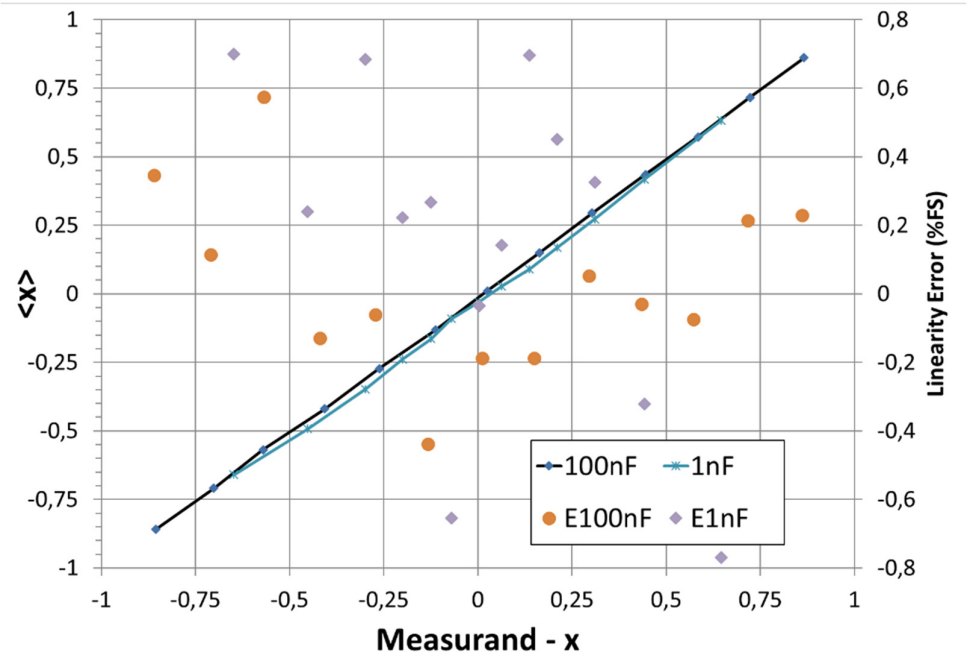


Figure 3.26 The calibration curve and the linearity error for extreme values of the C_S ∈ [1, 100] nF. Linearity errors for other C_S values are in the between.

3.3.1.3.2 Dynamic response characterization

In addition, dynamic performance has been evaluated. In this scenario, the same setups used for the simulations are replicated for the real-world prototype. For sake of simplicity, only a subset of all the possible C_S and measurand x variations has been considered. Subsequently, supposing a first-order low-pass response, a fitting with an exponential function allows to estimate the actual cutoff angular frequency, as resumed in Table VI and *Table VII*. Frequencies similar to the simulated values are obtained. Differences are mainly imputable to tolerances on the nominal value of passive components. In addition, it has to be remembered that, at the integrator output, a residual ripple is observed. Main components are at $2 \cdot \omega_{ref}$, due to the forward multiplier, and at ω_{ref}, due to any offset induced by devices and fed to the multiplier in the forward path. Clearly, the smaller the RC value, the less effecting the filtering action of the integrator. As a concluding remark, if faster circuit response is needed, a comparatively higher excitation frequency ω_{ref} has to be adopted.

Table VI experimental evaluation of the cutoff angular frequency (rad/s) ($C = 2$ NF, $R = 200$ KΩ)

x variations	-6/7 → 6/7	6/7 → -6/7	-1/7 → 1/7	1/7 → -1/7
C_0=100nF/7	78.13	78.13	81.30	81.97
C_0=10nF/7	78.13	78.74	80.65	81.30
C_0=4.7nF/7	79.37	78.74	79.37	81.97

Table VII experimental evaluation of the cutoff angular frequency (rad/s) (C = 2 NF, R = 20 KΩ)

x variations	-6/7 → 6/7	6/7 → -6/7	-1/7 → 1/7	1/7 → -1/7
C_0=100nF/7	657.89	781.25	751.88	810.11
C_0=10nF/7	709.22	787.40	746.27	803.82
C_0=4.7nF/7	645.16	781.25	729.93	805.79

Finally, in this paragraph a comparison with other research works is again proposed in Table VIII. As stated in the previous paragraphs, the proposed circuit suffers from parasitics, but the error is always smaller than 1%FS. Moreover, it has to be highlighted that such an error is evaluated across the full range capacitive variation, differently from other works. The interface integration into a single chip solution can mitigate parasitics effect. Additionally, an active compensation technique can be applied as well.

Table VIII Comparison table

Reference	[23]	[16]	[38]	Section 3.2.1	This work
C_0[F]	20 p	500 p	400 p	400 p	140p÷14n
Variation range [%]	±60	±50	±50	-30 +100	±100
Approach	C to V	C to V	C to Digital	C to V	C to V
Error [%]	<0.1	<0.03	<0.2	<0.45	0.5÷0.8

3.3.2 Integrated version

One of the main limitations of the interface presented in the previous paragraph is its dynamic response, as also highlighted. Part of the problem can be identified in the fact that the integral feedback controller, thanks to its intrinsic low pass behaviour, is used not only to generate the bridge feedback voltage, but also to demodulate the high frequency signal coming from the demodulation multiplier. In this way, the constraints on the control voltage residual ripple lead to design an integrator with a very high group delay which, in turn, leads to a relatively long feedback settling time. The presented work tries to overcome this limitation by splitting the low pass filtering action from the feedback controller action. The design of high-order low pass filters, together with the possibility to add the proportional action to the system controller, has greatly decreased the feedback transient. Moreover, the CMOS implementation of the interface has allowed to reduce its

overall parasitic capacitances hence decreasing the minimum allowable sensor baseline.

3.3.2.1 Theory of operation

The block diagram of the proposed circuit is shown in Fig. 3.27. C_1 and C_2 form the differential capacitive sensor that, excited by a sinusoidal signal V_{ref}, occupies the left branch of the auto-balanced bridge structure. Variations in the position of the sensor movable plate alters the balancing condition, so that the differential amplifier error signal $\Delta V = V_a - V_b \neq 0$. As stated in the previous paragraphs, the feedback loop aims to restore the balance condition $\Delta V = 0$ by acting on the modulator stage, designed around a multiplier fed by a reference sinusoidal voltage, V_{ax} (related to the carrier signal) and a variable DC voltage, V_{ctrl} (the actual modulating signal), which is also the output signal of the proposed interface. The multiplier replaces the MOSFET used as voltage controlled resistor (VCR) in the circuit proposed in Section 3.2.2. By doing this, it has been possible both to remove the DC biasing voltage of the bridge which was used to bias the transistor and to obtain the linearization of the input-output relationship of the interface.

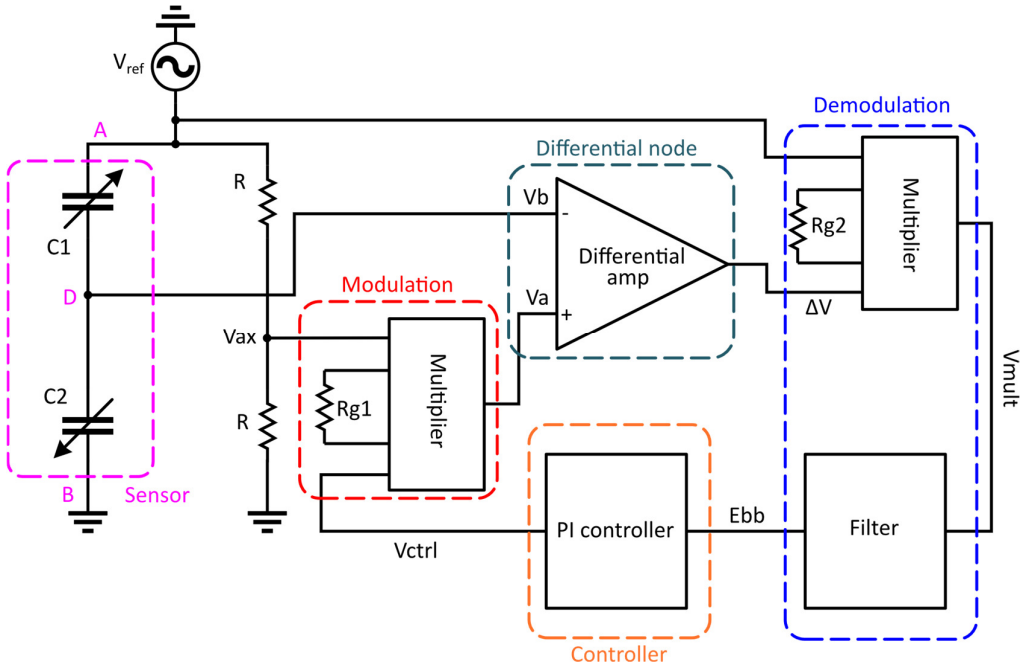


Figure 3.27 Schematic diagram of the interface proposed in [49].

 *The work presented in this section was published by the authors in [49].

The amplitude of the aforementioned (bandpass) error signal ΔV is retrieved by means of the demodulation section. This consists of a multiplier and a low-pass filter, whose output, E_{bb}, feeds the PI (Proportional Integral) controller, closing the feedback negative loop. It has to be highlighted that the presented interface is able to correctly identify a variation of the sensor in its full $\pm$100% range; differently said, a complete dynamic detection is obtained.

Being the autobalance loop a negative feedback and considering the interface in a steady state condition, it is possible to reach a general input output relationship. At the steady state in fact:

$$\Delta \boldsymbol{V} = \boldsymbol{0} \Rightarrow \boldsymbol{V_a} = \boldsymbol{V_b} \tag{3.19}$$

By using the previously introduced differential capacitance sensor relations, and being

$$\begin{aligned} \boldsymbol{V_a} &= \frac{\boldsymbol{V_{ref}}}{\boldsymbol{2}} * \boldsymbol{V_{ctrl}} * \boldsymbol{\alpha} \\ \boldsymbol{V_b} &= \frac{\boldsymbol{V_{ref}}}{\boldsymbol{2}} * (\boldsymbol{1} + \boldsymbol{x}) \end{aligned} \tag{3.20}$$

where $V_{ref} = |V_{ref}| \cdot \sin(\omega t)$ is the sinusoidal excitation signal, whereas α depends on the modulator multiplier implementation and has a dimension of [1/V], we can write Eq. 3.19 as:

$$\boldsymbol{V_a} - \boldsymbol{V_b} = \frac{\boldsymbol{V_{ref}}}{\boldsymbol{2}} * (\boldsymbol{V_{ctrl}} * \boldsymbol{\alpha} - \boldsymbol{1} - \boldsymbol{x}) = \boldsymbol{0} \tag{3.21}$$

From Eq. 3.21 we have an ideal relationship between x and $V_{out} = V_{ctrl}$:

$$\boldsymbol{x} = \boldsymbol{V_{ctrl}} * \boldsymbol{\alpha} - \boldsymbol{1} \tag{3.22}$$

It is visible that thanks to the adjustment of the α parameter, we can obtain a consequent regulation in the interface sensitivity. The exact expression for α depends on the actual transistor-level design of the multiplier which will be provided in the next paragraphs. It is finally important to underline that both multipliers have a variable gain (through R_{g1} and R_{g2}) whose value, even though independently tuneable, should be kept fixed for the interface to work properly.

The proposed interface has been designed in a standard CMOS (AMS 0.35µm) technology with a $\pm$1.5V supply voltage. In the following, main building blocks are described. Fig. 3.28 shows the internal topology developed for the operational

transconductance amplifier. Analogously to what is proposed in Section 3.2.2, it consists of a dual stage architecture. The input stage (*M1*, *M10*, Ibias) is a nMOS symmetrical OTA, (Operational Transconductance Amplifier) in order to guarantee the minimum possible offset voltage. The second stage (*M11-M14*, *Rc*, *Cc*) is a cascoded inverter, whose aim is to increase the overall open loop gain of the amplifier. Table IX evidences the dimensions of each transistor: the input pair has been designed so to have a high W/L ratio to increase the gain of the amplifier as well as reducing both thermal and flicker noise as much as possible. The ratio between *M5* and *M3* dimensions $(W/L)_{M5}/(W/L)_{M3}$ (and similarly for *M6* and *M4*) represents the so called '*B*' parameter. Designing $B \approx 5$ maximizes the gain-bandwidth frequency together with the slew rate (the downside is the increment of the overall power consumption of the input stage).

The total gain A_v of such a topology can be computed as the product of the two stages gains A_{v1} and A_{v2}, respectively:

$$A_v = A_{v1}A_{v2} \tag{3.23}$$

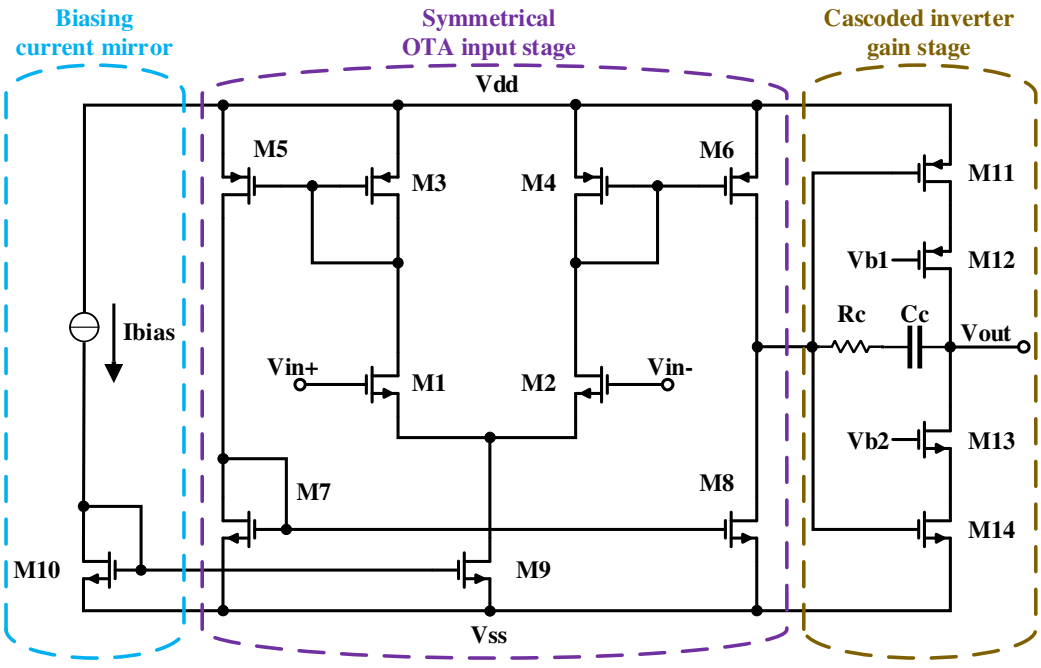


Figure 3.28 Operational transconductance amplifier schematic. From the left: the biasing current mirror, the symmetrical OTA as input stage, the cascoded inverter as gain stage.

It results:

$$A_v = B\frac{gm_{M1}}{gds_{M8} + gds_{M6}}(gm_{M11} + gm_{M14})R_{out} \quad (3.24)$$

being:

$$R_{out} = (gm_{M13} * Rds_{M13} * Rds_{M14})//(gm_{M12} * Rds_{M11} * Rds_{M12}) \quad (3.25)$$

The stability of the dual stage architecture is ensured by the capacitor *Cc* and the resistor *Rc* performing a pole-zero frequency compensation. The values for *Cc* and *Rc* are reported in Table IX, together with the key parameters of the designed OTA.

The presented OTA has been adopted as a building block to implement an instrumentation amplifier (INA) which in turn represents the final shape of the differential amplifier. The circuit is shown in Fig 5. Its voltage gain is:

$$G = 1 + \frac{50000}{R_g} \quad (3.26)$$

and can be set adjusting the value of Rg which is the resistor connected between terminals R_{g_a} and R_{g_b} (see Fig. 3.29).

The analog voltage multiplier shown in Fig. 3.30 relies on the so-called differential flipped voltage follower architecture (DFVF) [43]. It can be logically split into a biasing section, the main core and an output section.

Table IX OTA transistor dimensions and features highlight.

Transistor	*W (µm)*	*L (µm)*	*Type*
M1,2	200.2	1.05	nMOS
M3,4	2.1	2.1	pMOS
M5,6	30.1	6.3	pMOS
M7,8	50.05	2.1	nMOS
M9,10	50.05	1.05	nMOS
M11,12	10.5	1.05	pMOS
M13,14	5.25	1.05	nMOS

Parameter	*Value*

Rc	40kΩ
Cc	1pF
Vb1 = Vb2	Gnd
Open Loop Gain	100dB
Static Power Consumption	200µW
GBW	52MHz
Input offset	300µV

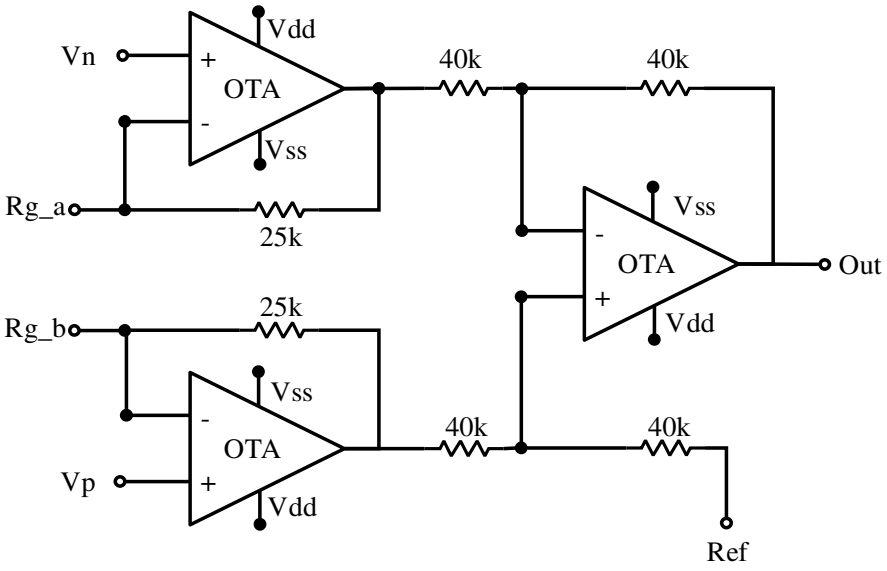


Figure 3.29 Instrumentation amplifier setup.

The biasing section takes advantage of the voltage translation given by a suitably designed FVF buffers cascade (i.e. nMOS FVF and pMOS FVF) to feed the actual core inputs with the sum of the input signal and of the DC biasing voltage.

The multiplier core is analysed in Section 3.2.2. It is composed by common source amplifiers (*M15 - M18*) together with DFVFs (*M19 - M24*).

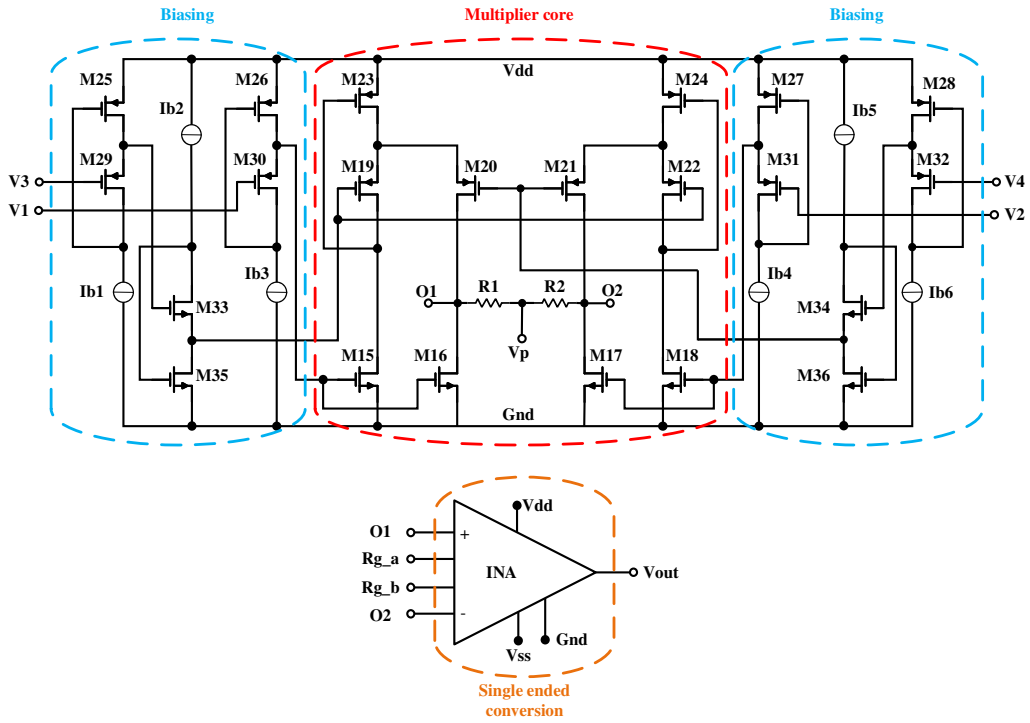


Figure 3.30 Multiplier schematic: dashed blue line highlights the biasing circuits, dashed red line highlights the multiplier core, dashed orange line highlights the output stage which takes O1 and O2 as inputs and performs the subtraction.

To work properly, these transistors have to be biased in saturation region. Under this condition, the output magnitude results as the difference between the two output voltages O_1 and O_2. To perform this operation, a differential amplifier (shown in Fig. 3.30) has been added. In particular, other than performing the subtraction, the INA allows to obtain an amplification to the multiplier output as well. Then we can write the output voltage formula as follows:

$$\boldsymbol{V_{out} = (O_1 - O_2) * G} \tag{3.27}$$

Setting $V_2 = V_4 = Gnd$ we have:

$$\boldsymbol{V_{out} = G * \left(R \sqrt{\mu_n \mu_p C_{ox,n} C_{ox,p} \left(\frac{W}{L}\right)_n \left(\frac{W}{L}\right)_p} \right) * V_1(t) * V_3(t)} \tag{3.28}$$

The ratio $(W/L)_n$ depends on the dimensions of *M15-M18* transistors, which have to be the same. Similarly, $(W/L)_p$ is the ratio between the dimensions of transistors *M19-M22*. The other parameters ($\mu_{n,p}$ and $C_{oxn,p}$) depend on the employed technology. The linearity range is ensured for an input peak voltage that goes from

about -250mV to 250mV. Transistor dimensions and biasing currents of the multiplier are given in Table X.

The task of the demodulation and control sections is to generate the feedback signal V_{ctrl} which, as previously stated, is also the output of the proposed interface. The error signal ΔV (the bandpass error) is fed into a multiplier (acting as a mixer) that

Table X Multiplier transistor dimensions and features highlight.

Transistor	*W (μm)*	*L (μm)*	*Type*
M15,16,17,18	1.05	1.05	nMOS
M19,20,21,22	50.05	4.2	pMOS
M23,24	301	4.2	pMOS
M26,27	0.35	1.05	pMOS
M30,31	1.05	0.35	pMOS
M25,28	0.35	1.05	pMOS
M29,32	1.75	0.35	pMOS
M33,34	50.05	0.35	nMOS
M35,36	0.35	10.15	nMOS

Parameter	*Value*
R1, R2	4kΩ
Ib1, Ib6	7μA
Ib2, Ib3, Ib4, Ib5	6μA

takes the bridge excitation voltage (V_{ref}) as second input. The spectrum of the output voltage of the multiplier, contains both a high frequency component ($2*f_{Vref}$), and a positive or negative DC voltage (the baseband error) which is extracted from a third order active low-pass filter and actually drives the controller. The filter is shown in Fig. 3.31a. It consists of a cascade of two stages: a second order Sallen-Key and a simple first order topology.

The PI controller, schematized in Fig. 3.31b, implements two parallel processing paths. It consists of a non-inverting integrator together with a non-inverting amplifier performing the integral and the proportional actions, respectively. The two contributions are then added by an inverting adder generating the feedback voltage V_{ctrl}. The PI gain tuning has been carried out through the Ziegler-Nichols technique at first and then refined so to smooth the overshoots. The values of the components are reported in Fig. 3.31b.

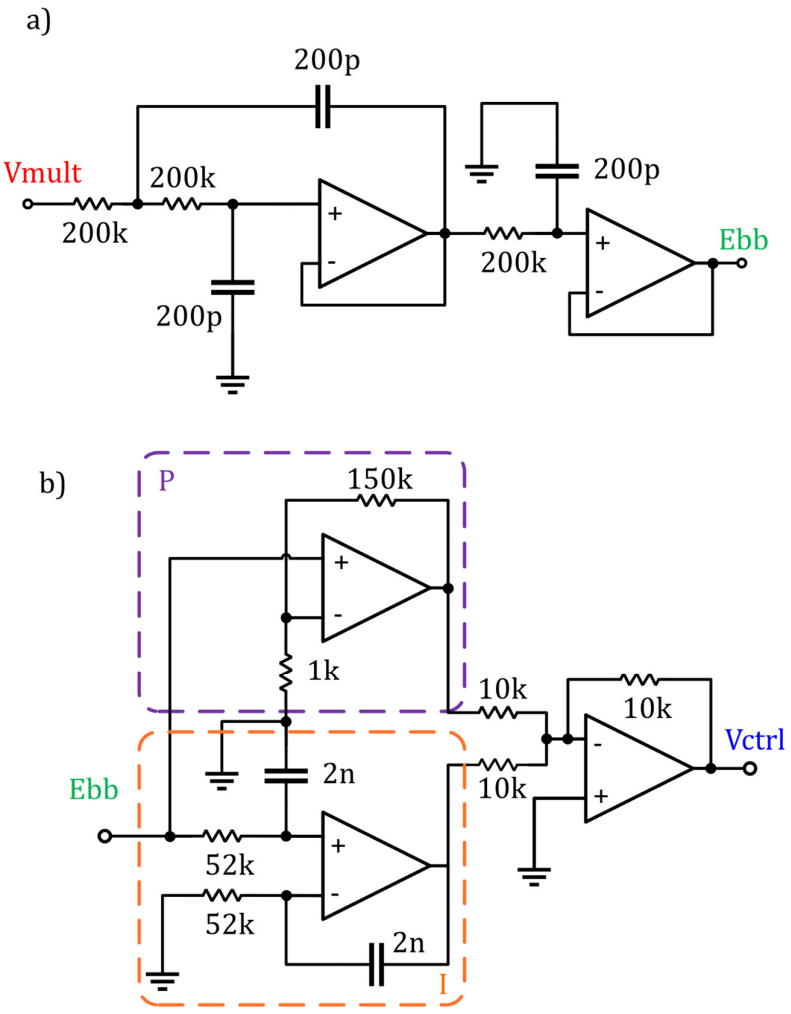


Figure 3.31 a) Demodulation filter schematic, b) proportional and integral controller schematic.

3.3.2.2 Simulation results

The proposed interface was tested in a Cadence PSpice environment. The aim was to evaluate the static response, comparing it with the developed theory, and to test

dynamic performances for obtaining a clear comparison between this work and the existing literature.

The gain of the differential amplifier has been set to 1, while the $k*G$ parameter of both multipliers has been set to 18. Although it was possible to increase the latter obtaining a greater output dynamic range (hence a better sensitivity), the chosen value minimizes the interface linearity error which is indeed acknowledged in Fig. 3.32. The figure shows a parametric sweep analysis conducted in the time domain. The sweeping parameter is the measurand x, the plotted output is the control voltage V_{ctrl}. The steady state data extracted from the same analysis is reported in Table XI. It is obtained averaging control voltage values after the exhaustion of its transient response and as visible, the full scale relative error remains below the 2.5% for a span of measurand variations that ranges from -90% up to 90%, confirming a good agreement between theory and simulations as well as the capability of the interface to perform a correct readout of the sensor in its full range. It is noticeable the fact that the error increases together with the control voltage, confirming that further increments in the interface sensitivity would lead to greater inaccuracy.

Fig. 3.33 shows the dynamic behavior of the circuit under examination. An abrupt variation in the sensor capacitors was forced so to obtain an almost full dynamic step response. The resulting settling time is approximately 1.2ms.

Expressing the sensitivity S with respect to the input capacitance variations $\Delta C = C1\text{-}C2$, where $x = \Delta C/(C1+C2)$, requires the differentiation of Eq. 3.28 leading to:

$$\boldsymbol{S_{\Delta C}^{V_{ctrl}} = \frac{1}{KG(C_1 + C_2)} = \frac{1}{18(C_1 + C_2)}} \qquad \textbf{(3.29)}$$

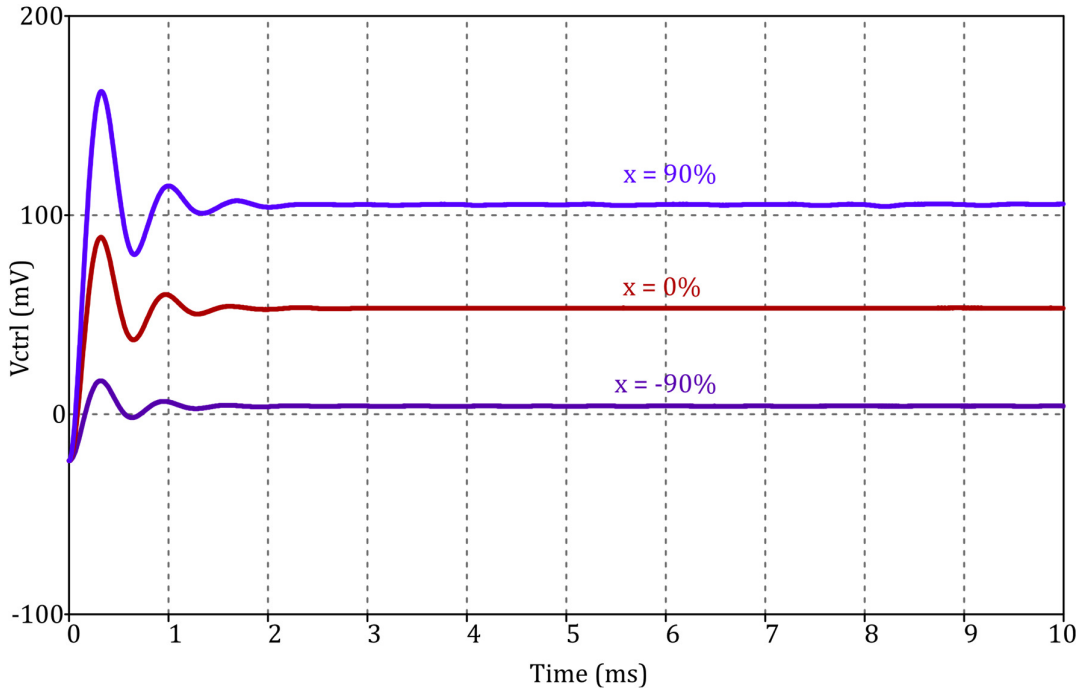


Figure 3.32 Interface time domain behavior for three different x values.

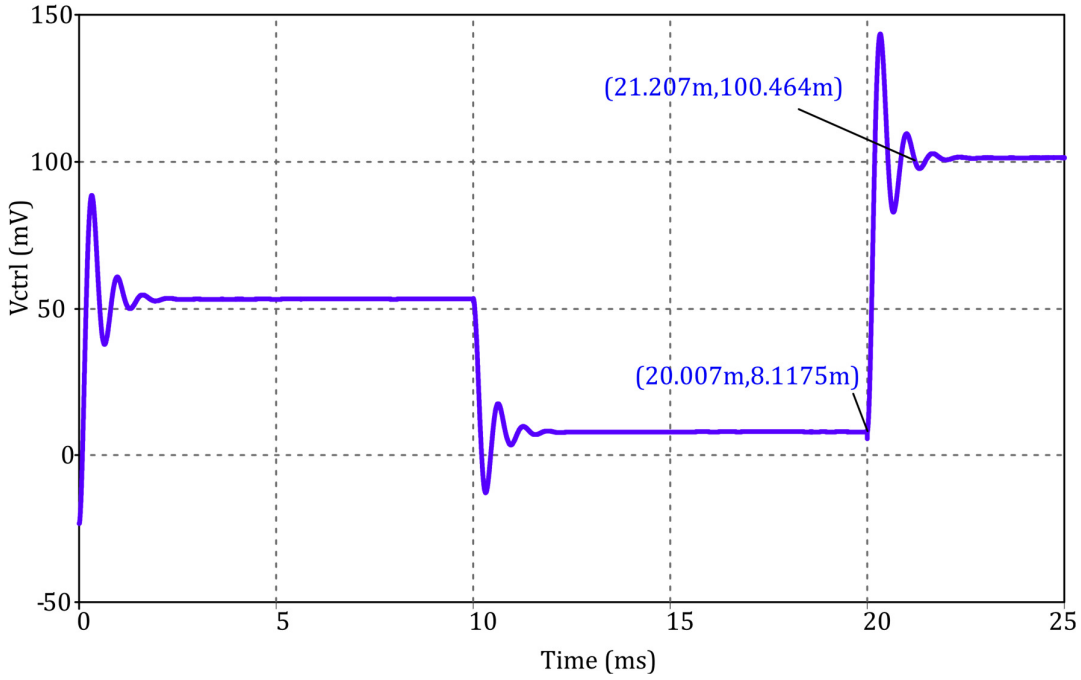


Figure 3.33 Interface dynamic response.

Table XI Comparison between simulated and theoretical input/output characteristic of the interface.

x (%)	*Vctrl (mV)*		*Error (%)*
	Simulations	***Theory***	
-90%	5.48	5.60	2.19%
-80%	10.9	11.1	1.72%
-70%	16.4	16.7	1.87%
-60%	21.9	22.2	1.37%
-50%	27.5	27.8	1.14%
-40%	33.1	33.3	0.71%
-30%	38.6	38.9	0.67%
-20%	44.2	44.4	0.43%
-10%	49.9	50.0	0.14%
0%	55.4	55.6	0.27%
10%	61.4	61.1	0.47%
20%	67.1	66.7	0.53%
30%	72.7	72.2	0.69%
40%	78.7	77.8	1.18%
50%	84.5	83.3	1.45%
60%	90.7	88.9	2.06%
70%	96.5	94.4	2.23%
80%	102	100	2.25%
90%	108	106	2.45%

For the topology depicted in Fig. 1.11a, $C_1+C_2=2C_{bl}$ holds, whereas for the one depicted in Fig. 1.11b it is $C_1+C_2=2C_{bl}/(1-x^2)$, i.e.

$$S_{\Delta C}^{V_{ctrl}} = \frac{1-x^2}{KG(2C_0)} \leq \frac{1}{18(2C_0)} \quad \textbf{applied to Fig. 1.11b}$$
$$S_{\Delta C}^{V_{ctrl}} = \frac{1}{KG(2C_0)} = \frac{1}{18(2C_0)} \quad \textbf{applied to Fig. 1.11a} \qquad (3.30)$$

so that for the former the sensitivity depends on the actual x value, while for the latter it is a constant value. The resolution can be defined as $R = N/S_{\Delta C}^{V_{ctrl}}$, where N is the noise in the useful bandwidth, which simulations estimated to be N = 190 μV.

As a consequence, R depends on x for the sensor implementation shown in Fig. 1.11b, while it is constant for the one shown in Fig. 1.11a.

Being the output of the interface dependent on the actual displacement of the movable plates ($\pm d_{max}$)of the connected sensor, it is worth expressing the sensitivity as a function of this physical magnitude. To do this, the sensor full scale can be redefined as $FS = 2d_{max}$ whereas the measurand as: $x = d/d_{max}$. The sensitivity can then be expressed as:

$$S_x^{V_{ctrl}} = \frac{1}{KG} \tag{3.31}$$

which holds for both configurations in Fig. 1.11.

Using the same topology shown in Fig. 1.11b with square plates (air as dielectric) and choosing $FS = 2\ mm$, we obtain a simulated sensitivity of 58mV/mm, well matching the theoretical one of 56mV/mm. Correspondingly, the resolution is on the order of 3 μm.

3.3.2.3 Measurement results

In order to test the presented solution and to verify the effectiveness of the changes introduced, a discrete board was designed and fabricated (Fig. 3.34), implementing the scheme proposed in Fig. 3.27. The excitation signal is sinusoidal, generated by a Wien oscillator, with a frequency of 9 kHz and an amplitude of 4 V. The power supply is dual-rail ±15V, thus ensuring no saturation occurs in all stages.

Each component has been chosen with the aim of preserving the input/output relationship previously described. For this reason, the differential instrumentation amplifier shown previously was replaced by an INA128, whose gain formula is the same as its integrated counterpart (Eq. 3.27). The chosen multiplier was the AD633. Its output voltage is given by:

$$V_{out} = V_{in1}V_{in2}\frac{1}{10} + V_{offset} \tag{3.32}$$

where 10 is expressed in Volt. It is possible to rewrite the expression that links V_{ctrl} to the measurand x by adjusting it to the new components:

$$x = \frac{1}{10}V_{ctrl} \tag{3.33}$$

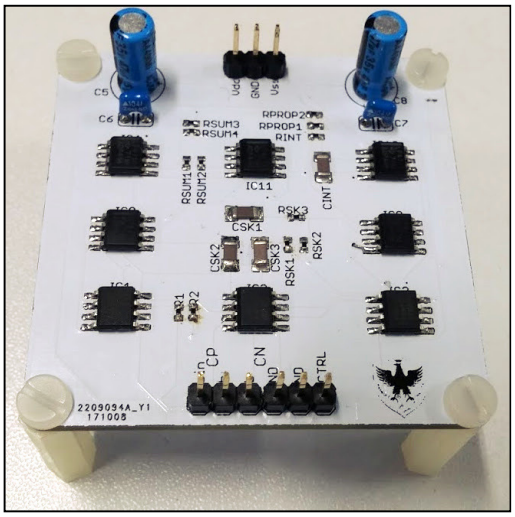


Figure 3.34 Fabricated discrete interface.

It is important to notice that the offset voltage of the modulating AD633 was set so to obtain a translation avoiding V_{ctrl} to saturate to the positive supply.

Measurements have been conducted using a set of reference capacitors emulating the behaviour of the sensor depicted in Fig. 1.11a with a baseline C_{bl} = 200 pF. With the aim of introducing the least number of artefacts to the interface characterization, the measurements have been taken utilizing a Keysight MSOX3054A oscilloscope with the N2843A probe in order for the instrumentation parasitic capacitances to remain very low and well known (about 11 pF). The DC characteristic shown in Fig. 3.35 has been obtained averaging 200 samples per measuring point.

The dotted magenta line represents the raw data extracted from the measurements, while the solid black one is the plot of the theoretical ideal characteristic. As visible the main difference between these two is given by a gain error (slope variation). In particular, we can update the ideal relationship shown in Eq. 3.33 introducing this non-ideality (G_{par}) as follows:

$$x = \frac{1}{10} V_{ctrl} G_{par} \qquad 0 < G_{par} < 1 \tag{3.34}$$

It is possible to easily deal with this problem adding a compensation gain greater than one: the dashed green line in Fig. 3.35 represents the same measurements output to which a gain of 1.04 was applied to counteract the gain error.

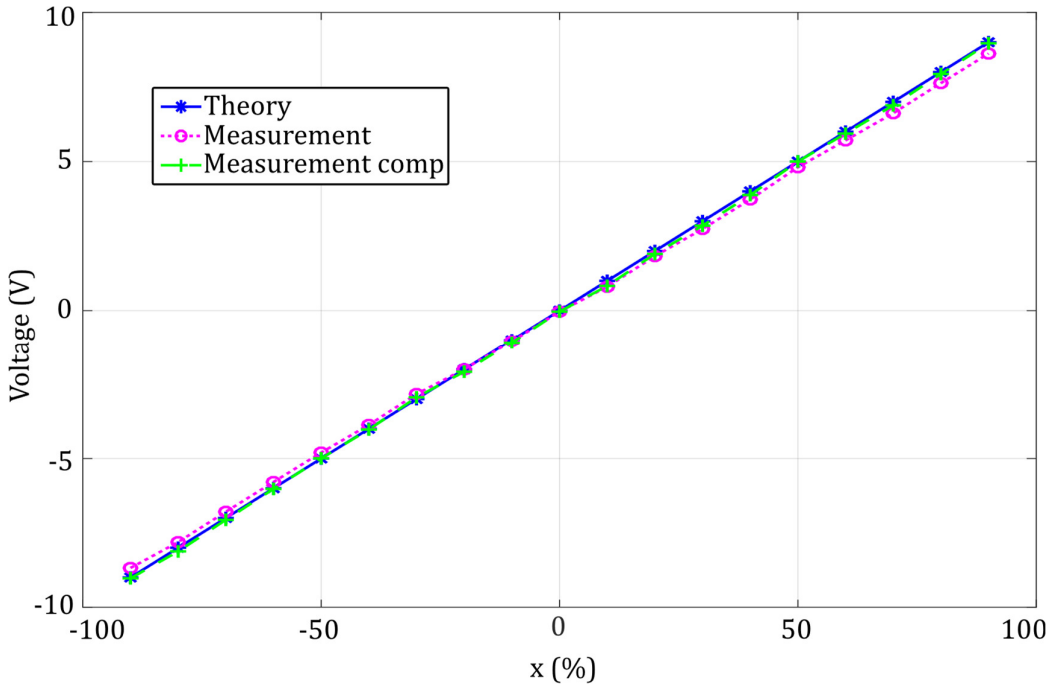


Figure 3.35. Comparison between theoretical and measured interface static behaviour.

It is noticeable the fact that uncertainties coming from parasitic capacitances are still not visible due to the relatively high baseline of the testing equipment emulating the sensor. The relative error between the ideal plot and the compensated measurements one is shown in Fig. 3.36 and remains constantly below 1.5% FS.

A test of the interface in dynamic conditions been performed as well. Switches driven by a microcontroller (ATMega SAMD21G18) were used to connect different combinations of reference capacitors simulating a dynamic step input from x = -70% to x = 80%. The output is shown in Fig. 3.37 (in green) and compared with the interface presented in Section 3.2.1 (in red). As visible, the addition of the proportional component to the controller of the system allowed to reduce the settling time from 70ms down to 6ms.

3.3.3 Discussion

Novel linear analog interfaces performing differential capacitance readout have been proposed in Section 3.3. These works overcome the main issue of a non-linear relationship between the output response and the measurand, providing a direct simple relationship between capacitive variation and output voltage.

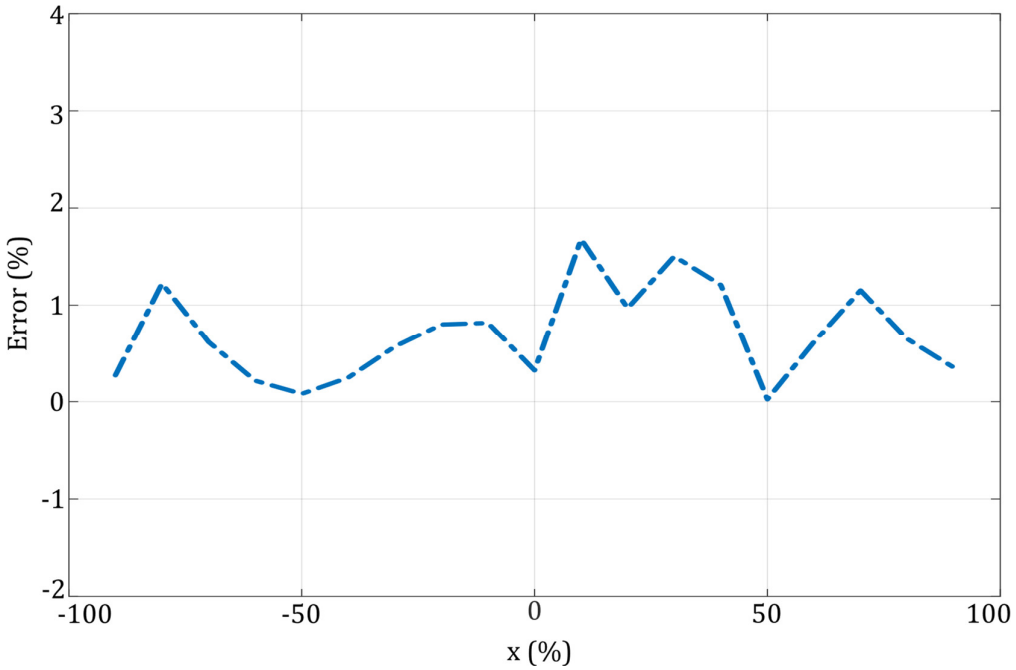


Figure 3.36. Theory vs measurements absolute relative error.

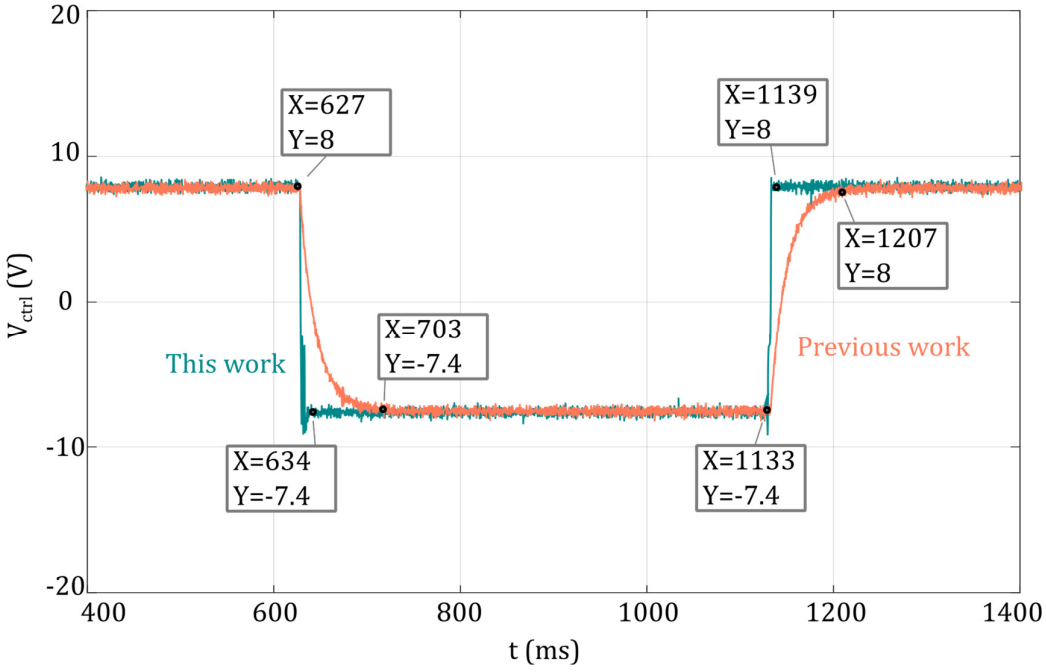


Figure 3.37. Comparison between two measured dynamic responses: the integral response (red) vs the integral and proportional one (green) of the presented work.

Theoretical and simulated considerations have proved the goodness of the proposed approaches. Discrete element board solutions have been tested, showing satisfactory results that confirm the circuit capability to follow the capacitive sensor variations in a full estimation range. The key problem that remain unaddressed by these works is their sensitivity to stray capacitances coming from the sensor itself, limiting the minimum baseline that the interface is able to work with. In this regard we have analysed the issue and proposed an interesting and autonomous solution that can be applied to any of the proposed interfaces (see next paragraph).

3.4 Parasitic compensation in autobalanced bridge differential capacitive sensor interfaces

3.4.1 Theory of operation

Fig. 3.38a recalls the equivalent model of a real-world differential capacitive sensor. There are three main contributions to the overall stray impedances C_{pu}, C_p and C_{pl}.

One of the advantages that inherently comes from an AC driven setup is the mitigation of the effects of both C_{pu} and C_{pl} [8, 28, 47, 51] due to the fact that C_{pl} is fully grounded, while C_{pu} is constantly facing the very low impedance of the signal generator, hence its effects are negligible.

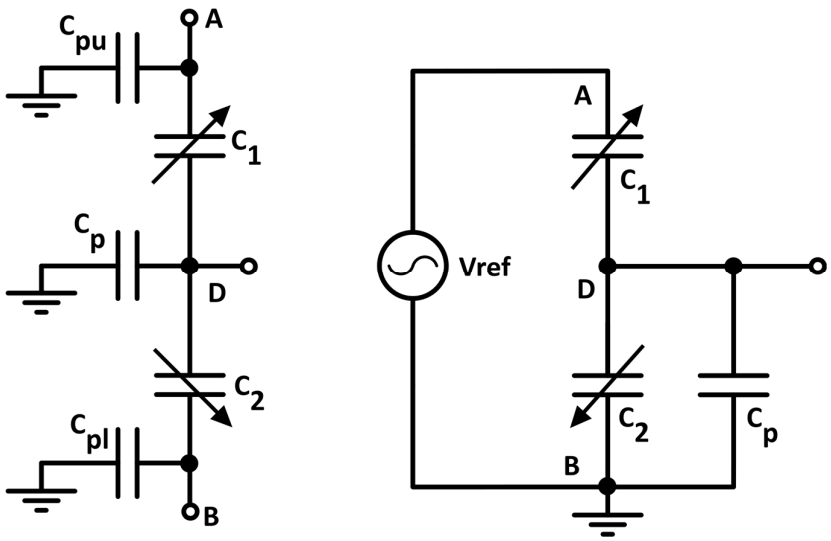


Figure 3.38 Real-world differential capacitive sensor a) equivalent model; b) driven by an AC source.

*The work presented in this section was partially published by the authors in [50].

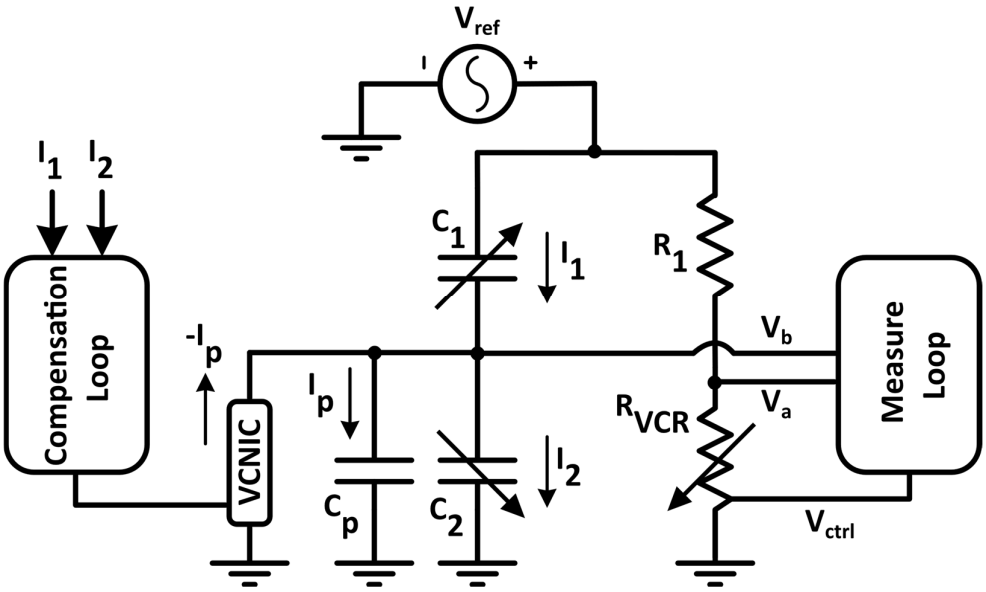


Figure 3.39 Compensation feedback loop applied to an auto-balanced bridge interface [50].

The compensation method which we propose here, is therefore focused on dealing with the effects of C_p only (see Fig. 3.38b) which takes part of the I_1 current (I_p) from I_2 causing a readout error.

The basic idea is to have a secondary feedback circuitry (compensation loop, see Fig. 3.39) acting in parallel with the "main loop" (which corresponds to the actual interface) analyzed in the previous sections, which, once at the steady state, can compensate the presence of the parasitic capacitance C_p.

The compensation is carried out by suitably driving a voltage controlled negative impedance converter (VCNIC) which makes sure to deliver to the parasitic capacitance the suitable portion of current ensuring that I_1 is equal to I_2. The difference between these two current indeed represents the error signal that the secondary feedback aims to nullify.

The architecture of the negative feedback loop is shown in Fig. 3.40. The working principle of the proposed circuit can be summarized as follows. Section A evaluates I_1 and I_2 converting them into proportional voltages and extracting their difference, that is the high frequency error signal ($V_{e,hf}$). Supposing to write these two currents as Eq. 3.35, the equivalent voltage conversion can be expressed as Eq. 3.36.

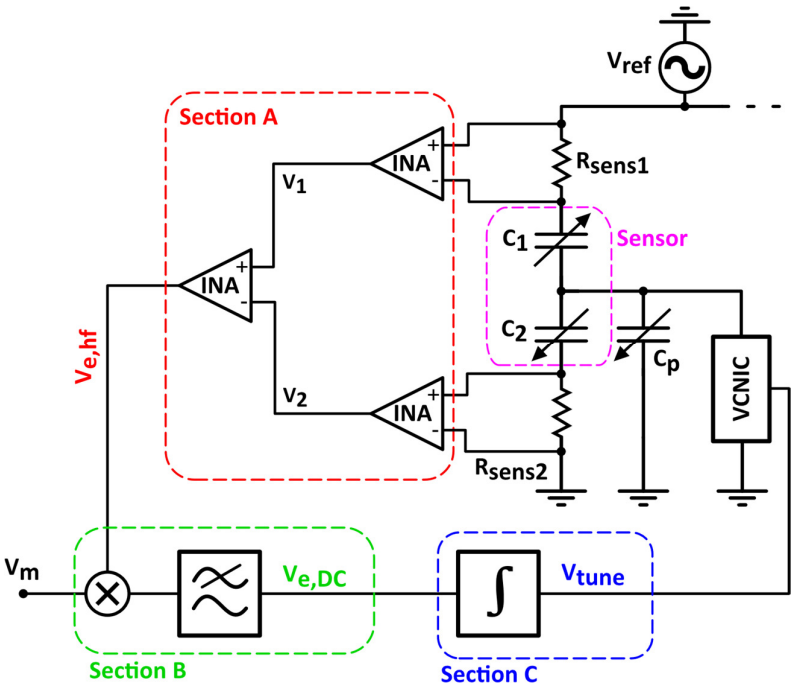


Figure 3.40 The feedback loop schematic diagram [50].

$$I_{1,2} = |I_{1,2}|\sin(\omega t) \tag{3.35}$$

$$V_{1,2} = |I_{1,2}|R_{sense}\sin(\omega t) \tag{3.36}$$

Therefore, the high frequency error $V_{e,hf}$ can be evaluated as:

$$V_{e,hf} = (|I_1| - |I_2|)R_{sense}\sin(\omega t) \tag{3.37}$$

Section B demodulates the high frequency error signal extracting the DC component (Eq. 3.38). This operation is performed by multiplying $V_{e,hf}$ by a known reference voltage, V_m, in phase with I_1 and I_2 and then low pass filtering the resulting signal.

$$V_{e,DC} = \frac{1}{2}(|I_1| - |I_2|)R_{sense}|V_{ref}| \tag{3.38}$$

Lastly, section C is composed by the feedback controller. It integrates the DC error producing the *VCNIC* control voltage V_{tune}:

$$V_{tune} = \alpha R_{sens} |V_{ref}| \int_t (|I_1| - |I_2|) dt \tag{3.39}$$

Once the compensation loop reaches the steady state, V_{tune} can be finally evaluated as:

$$V_{tune} = -10 \frac{|C_{par}|}{C_{nic}} + 10 \tag{3.40}$$

The voltage controlled negative impedance converter is implemented by means of a modified standard NIC (see Fig. 3.41a). The input impedance of such a device can be computed as:

$$Z_{in} = \frac{I_{in}}{V_{in}} = -\frac{1}{j\omega \frac{R_{nic2}}{R_{nic1}} C_{nic}} = \frac{1}{j\omega C_{eq}} \tag{3.41}$$

where C_{eq} is:

$$C_{eq} = -\frac{R_{nic2}}{R_{nic1}} C_{nic} \tag{3.42}$$

In order to obtain its voltage-controlled equivalent, it is possible to change the R_{nic2}/R_{nic1} ratio through a suitable VCR obtained by implementing R_{nic1} through a Zhong-connected AD633 as shown in Fig. 3.41b. Therefore, by substituting Eq. 3.3 into Eq. 3.42 (considering that V_{ctrl} in this situation corresponds to V_{tune}), it is possible to link the VCNIC equivalent capacitance and the control voltage V_{tune}, as follows:

$$C_{eq} = -R_{nic2} C_{nic} \frac{10 - V_{tune}}{10 R_f} \tag{3.43}$$

Choosing R_{nic2} equal to R_f, Eq. 3.43 becomes:

$$C_{eq} = -C_{nic} \frac{10 - V_{tune}}{10} \tag{3.44}$$

As it comes out from this analysis, there is a linear relationship between the negative capacitance and the tuning voltage V_{tune}. The actual span for the VCNIC is dependent both from the feedback capacitance C_{nic} and from the control voltage full-scale. A comparison between the theorized approach and other common approaches available in the literature is offered in Table XII. As visible, the presented work

inherits all the advantages of its competitors, with the only downside being in the increased circuitry needed for the *compensation loop*.

Table XII Main compensation techniques comparison

Method	Pros	Cons
Shielding [52-53]	• Adaptive compensation • Simple implementation	• Generation of positive feedbacks leading to instability • No compensation for interface stray capacitances
Static compensation [54]	• Active compensation (negative impedance converter)	• Necessity to know the exact value of Cp • No compensation for Cp variable in time
Phase compensation [56]	• Adaptive compensation • Ability to compensate for both sensor and interface parasitic capacitances	• Clock signals to drive the switches • Sequential process: addition of time to the actual measurement
This work	• Adaptive compensation • Ability to compensate for both sensor and interface parasitic capacitances • Parallelism between compensation and actual measurement	• Addition of extra circuitry

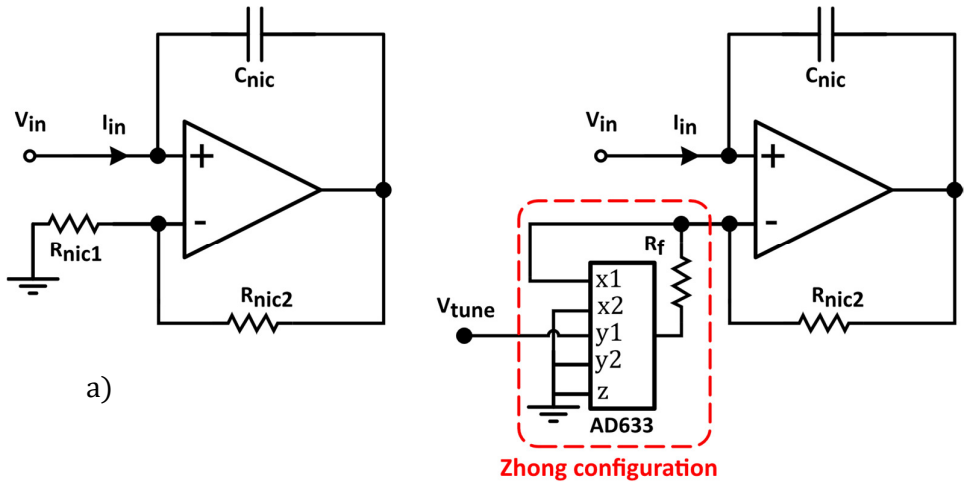


Figure 3.41 a) The utilized negative impedance converter; b) The complete VCNIC.

3.4.2 Simulation results

The most critical choice for a proper feedback operation is the $R_{sense1,2}$ value and what kind of differential current sensing amplifier must be employed. To this aim, a simple analysis on the current signals I_1 and I_2 has been done. Considering the peak value of the V_{sin} voltage ($|V_{sin}|$) as fixed at 5V and supposing the sensor baseline ranging from units of pF to hundreds of pF, it is possible to evaluate the amplitude of the currents from about 1 to hundreds of μA. Consequently, by choosing $R_{sense1,2}$ = 1kΩ, it is possible to obtain a voltage drop equal to 1 mV/μA without affecting bridge behavior at the working frequency of 10 kHz (we suppose that neither amplitude changes nor phase changes are introduced to the signal V_b thanks to the capacitive impedance being still dominant with respect to the resistive one). The chosen amplifier is an instrumentation amplifier (AD8422), that is able to ensure a maximum input offset voltage of 25μV and a peak-to-peak input noise of 0.15μV. The gain has been set to 100 V/V, hence the amplitude of V_1 and V_2 ranges between around 100 mV up to 10 V, so taking advantage of the full amplifier output dynamic range. The integrated multiplier is the AD633 device, while the low pass filter is a third-order Bessel type.

Simulations have been carried out in two different scenarios.

In the first one, the capability of the feedback loop was tested to compensate the bridge for different stray capacitance values while keeping the differential sensors

to its baseline. Fig. 3.42 shows the simulation results: it is possible to notice that even though the system reaches its steady state in about 15 ms, the final values of V_{tune} do not match with those given by the Eq. 3.40 obtained by considering the simulated C_p value; this behavior confirms the presence of other parasitic capacitances introduced by the electronic circuitry added to create the feedback, but, in particular, endorses that the feedback itself is able to compensate all of them. In the second scenario, a set of simulations combining many different real working conditions has been carried out and allows to understand whether the V_b value, which gets corrupted due to parasitic capacitance action, is properly restored by the compensation feedback.

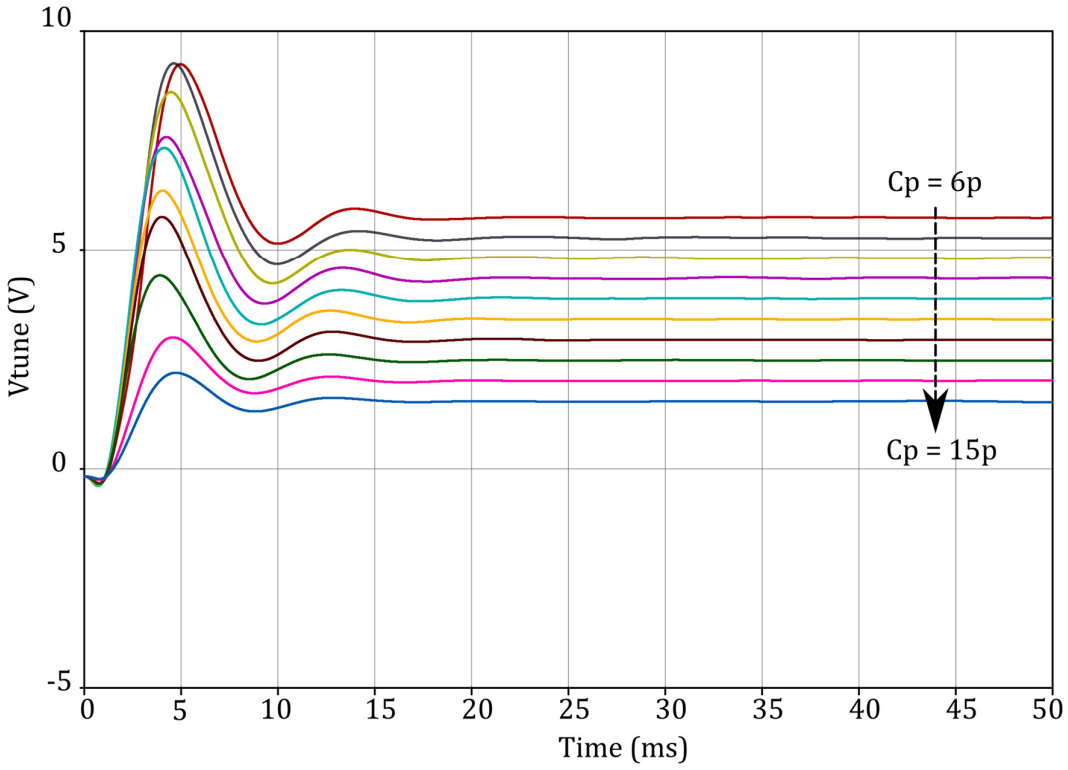


Figure 3.42 Dynamic response of the simulated compensation loop at different values of Cp.

Table XIII Simulated results comparing ideal, compensated and uncompensated Vb voltage. Sensor baseline is equal to 10 pF, parasitic capacitance to 6.25 pF.

x	Vb_{id}/V_{sin}	Vb_{sim}/V_{sin}	Vb_{uc}/V_{sin}	Eid_{uc}	Eid_{sim}
-90%	0.05	0.046	0.039	**22.88%**	**8%**
-70%	0.15	0.144	0.11	**23.04%**	**3.52%**
-30%	0.35	0.33	0.27	**23.07%**	**4.08%**
0%	0.45	0.44	0.35	**23.09%**	**2.77%**
30%	0.65	0.64	0.45	**23.10%**	**1.63%**
70%	0.85	0.84	0.65	**23.10%**	**0.97%**
90%	0.95	0.94	0.73	**23.11%**	**0.69%**

In Table XIII a representative case is reported, where the stray capacitance has been chosen equal to 30 pF to stress out the effectiveness of the circuitry. The table reports the values of V_b in the ideal conditions Vb_{id}, under the action of the presented system Vb_{sim} and uncompensated Vb_{uc} (that is without the action of the feedback). In the same table, it is also shown the percentage absolute error between simulation results and ideal values, Eid_{sim}, and the same error between ideal values and uncompensated ones, Eid_{uc}. As it comes from these error columns, thanks to the compensation feedback, the error with respect to the uncompensated bridge is significantly reduced.

3.4.3 Measurement results

To evaluate the effectiveness of the proposed stray capacitance compensation system, two sets of experimental tests have been carried out. Similar to the simulation setup, in the first one, the ability of the compensation circuit of mimicking a capacitance with value equal and opposite to the stray capacitance Cp has been demonstrated. In the second one, the increased performance of the overall

readout system has been evaluated. An emulated differential capacitive sensor and discrete component prototypes implementing the proposed compensation system and the considered sensor interface have been employed for this purpose. The experimental setup is shown in Fig. 3.43; an Agilent 34411A digital multimeter has been used to acquire the outputs of the controller output two circuits, i.e., the V_{tune} and V_{ctrl} signals, for the first and second test, respectively. In the following, more details about the actual implementation of the experimental setups and obtained results will be illustrated and commented.

3.4.3.1 The emulated DFVF

Since the proposed compensation system is not tied to a specific differential capacitive sensor, a sensor emulator realized with discrete components has been adopted. In such a way, it is possible to easily control the value of the (emulated) measurand x, as well as to vary the overall stray capacitance C_p, thus emulating different operating conditions.

The schematic of the realized emulated sensor is shown in Fig. 3.44. It is composed of a set of ten capacitors (C_{e0} - C_{e9}) connected in series, where a terminal of C_{e0} and a terminal of the C_{e9} one are used as the excitation signal input (sensor terminals A and B). The sensor output (terminal D) is derived from one of the nine capacitors' connection nodes, by means of a proper selector. In such a way, it is possible to emulate the behavior of a hyperbolic sensor (see Fig. 1.11b), where variations of the measurand x are obtained by changing the selector position.

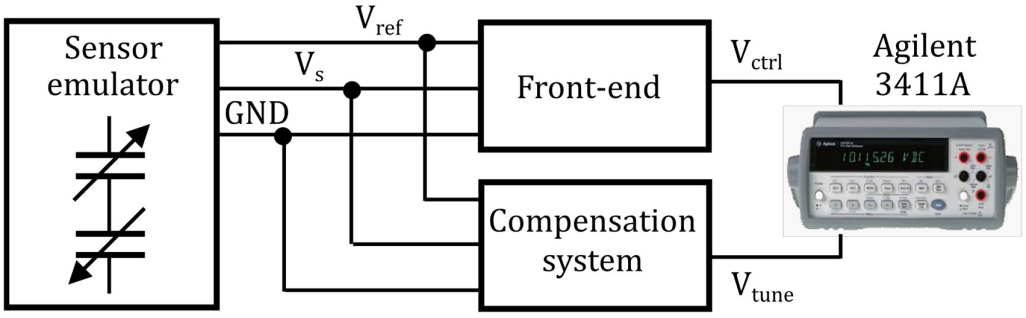


Figure 3.43 The block scheme of the employed experimental setup.

For sake of completeness, the stray capacitance C_p, from a physical perspective, can be considered as the parallel of the three parasitic components C_{pc}, C_{pi} and C_{pw},

which are the sensor parasitic capacitance at node D, the parasitic contribution due to the readout electronics and the connection between the sensor and the interface, respectively. The value of these components is usually unknown and difficult to be estimated. In order to facilitate the evaluation of the proposed system with different values of stray capacitance, an additional component to C_p has been added, by means of a capacitor C_{pe}, placed between the (emulated) sensor output and ground (see Fig 3.44). In such a configuration, when the emulated sensor is connected to the readout interface, C_{pe} is in parallel with the previously-defined C_{pc}, C_{pi} and C_{pw},

Defining $C_{p0} = C_{pc} + C_{pi} + C_{pw}$ as the baseline stray capacitance, the overall stray capacitance C_p can now be obtained as $C_p = C_{p0} + C_{pe}$. This relationship implies that C_{p0} is invariant; this can be considered true if the experimental tests have a relatively short duration, with respect to environmental changes.

The emulated sensor has been implemented by means of a simple printed circuit board (PCB); to minimize the parasitic capacitive effects, the selector has been realized with multiple solder jumpers. The value of the capacitors has been chosen to cover most of the sensor operating range ($-1 < x < 1$); in particular, the first and last capacitors have a value of 2.2 nF, whereas the other ones of 1 nF. In that way, the set of possible emulated values for x is $\{0, \pm 0.22, \pm 0.45, \pm 0.67, \pm 0.90\}$ and the sensor baseline C_{bl} is about 225 pF.

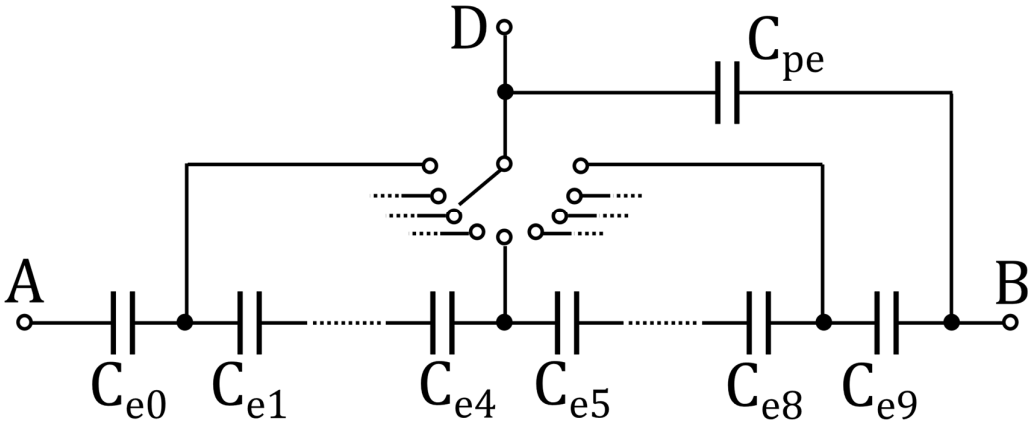


Figure 3.44 Schematic of the emulated differential capacitive sensor.

The employed capacitors have a tolerance on the nominal value of 10%; to limit the effect of uncertainty on nominal values, which reflects on uncertainty on the measurand x, a system calibration procedure has been accomplished by means of a least mean square (LMS) interpolation, as will be detailed in the next subsections.

3.4.3.2 Discrete components prototypes

As previously stated, a real-world proof of concept prototype of the compensation circuit has been realized using discrete components. It has to be highlighted that the proposed architecture can be easily integrated in a single chip solution, since only well proved and well known function blocks are adopted. Thus, the use of a discrete component solution allows to estimate performance obtainable with an integrated implementation.

Referring to the scheme in Fig. 3.40, three AD8421 INAs from Analog Devices, two AD633 analog multipliers from Analog Devices, and four LF411 operational amplifiers from Texas Instruments (one for the VCNIC, one for the integrator and two for the third order low-pass filter blocks) have been employed. Since $R_{feed} = R_{nic2}$, as stated in subsection 3.4.1, the relationship between the equivalent negative capacitance and the control voltage V_{tune} of the VCNIC becomes as Eq. 3.44.

Similarly, the discrete component interface shown in subsection 3.3.2 has been used as the autobalancing sensor interface for the experimental tests.

A dual $\pm$15 V power supply has been used for both the prototypes.

3.4.3.3 Performances evaluation of the compensation circuit

In this experimental test, the sensor emulator is configured in the central position, i.e., $x = 0$; different values of C_{pe} are then employed, to evaluate different scenarios of parasitic capacitance C_p. As visible in Eq. 3.44, the theoretical maximum absolute value of C_{eq} is about 2.5 times the NIC feedback capacitor C_{nic}. In practice, this value is not reachable, since the employed components are not rail to rail. Once the range of the parasitic capacitance to be compensated has been determined, the value of C_{nic} should be chosen accordingly. In this test, two values of C_{nic} have been adopted, i.e., C_{nic} = 20 pF and C_{nic} = 47 pF. The autobalancing sensor interface has been connected to the setup to provide the sensor excitation signal; however, the front end output V_{ctrl} has not been evaluated in this test. The multimeter has been used to acquire the steady value of the compensator controller output V_{tune}, which allows to

compute, by inverting Eq. 3.44, $<C_{eq}> = <C_{eq}>(V_t)$, i.e., an estimation of the equivalent capacitance C_{eq} that the NIC is mimicking. Since in steady conditions C_{eq} should be equal and opposite to C_p, the absolute value of $<C_{eq}>$ is used to evaluate the capability of the proposed circuit of compensating the stray capacitance C_p. It should be noticed that the value of the baseline stray capacitance component Cp0, as defined in subsection 3.4.3.1, is generally unknown, but invariant; an estimation of C_{p0} can be obtained by considering the absolute value of $<C_{eq}>$, when $C_{pe} = 0$. For the two considered scenarios, i.e., $C_{nic} = 20$ pF and $C_{nic} = 47$ pF, the estimated values of C_{p0} is $<C_{p0}> \approx 31.9$ pF and $<C_{p0}> \approx 29.9$ pF, respectively. Table XIV and Table XV show the employed values of C_{pe} (nominal values), the emulated stray capacitance estimation $<C_p>$, the measured V_{tune} values (average of 20 measurements) and the related estimations $<C_{eq}>$ of C_{eq}. The compensation relative error, defined as in Eq. 3.54, where FS stands for Full Scale, is also reported; this parameter is considered as a metric to evaluate the compensator performance.

$$\boldsymbol{Err_c = 100\frac{< C_p > -|< C_{eq} >|}{FS} = 100\frac{< C_{p0} > + C_{pe} - |< C_{eq} >|}{FS}} \qquad \textbf{(3.45)}$$

As visible from the tables, the proposed circuit has been able to mimic the value of the parasitic capacitance C_p with a relative error of about 1% FS over all the working range, which is approximately two times the value of the NIC feedback capacitor C_{nic}. This result is in agreement with the tolerance of the discrete capacitors employed for C_{pe}, which is 5%.

Table XIV Performance of the proposed compensation circuit with NIC feedback capacitor C_{nic} = 20 pF; estimated baseline stray capacitance is C_{p0} ≈31.9 pF.

C_{pe} [pF]	$<C_p>$ [pF]	V_{tune} [V]	$<C_{eq}>$ [pF]	Err_C
2.2	34.1	-6.95	-33.9	0.4%
3.3	35.2	-7.48	-35.0	0.5%
4.7	36.6	-8.33	-36.7	-0.2%
5.6	37.5	-8.76	-37.5	-0.1%
6.8	38.7	-9.37	-38.7	-0.1%
8.2	40.1	-9.93	-39.9	0.5%
10	41.9	-10.90	-41.8	0.2%
12	43.9	-11.71	-43.4	1.0%

Table XV Performance of the proposed compensation circuit with NIC feedback capacitor C_{nic} = 47 pF; estimated baseline stray capacitance is C_{p0} ≈29.9 pF.

C_{pe} [pF]	$<C_p>$ [pF]	V_{tune} [V]	$<C_{eq}>$ [pF]	Err_C
10	39.9	1.44	-40.3	-0.3%
22	51.9	-1.15	-52.4	-0.5%
32	61.9	-3.36	-62.8	-0.8%
47	76.9	-6.44	-77.2	-0.3%
69	98.9	-11.23	-99.8	-0.9%

3.4.3.4 Performance evaluation of the overall readout system

In this test, the effectiveness of the proposed compensation system when employed in combination with the sensor front-end is evaluated. In particular, performance improvement on the sensor readout achieved by the stray capacitance compensation will be demonstrated. For this reason, the first step in this test is the performance evaluation of the considered autobalancing front-end, with different values of stray capacitance and without the use of the compensation system.

The capacitance compensation circuit in Fig. 3.43 has been disconnected from the setup; the Agilent 34411A digital multimeter has been used to acquire the front-end output signal V_{ctrl}, thus allowing to reckon an estimation $<x>$ of the sensor measurand by means of Eq. 3.33. As previously mentioned, a calibration procedure has been accomplished to limit the effect of nonidealities and components' tolerance. A first set of measurements with all the emulated measurand x values and with $C_{pe} = 0$ is performed and the computed $<x>$ data set, together with x, has been used to perform an LMS interpolation. The slope m_i and offset q_i parameters obtained by the linear regression are used to adjust the computed $<x>$ values, thus obtaining a linearized version of the measurand estimation $<x>_{lin} = m_i<x> + q_i$.

The behavior of $<x>_{lin}$ with respect to the emulated sensor measurand x, with different values of C_{pe}, is shown in Fig. 3.45. The negative effect of the parasitic capacitance is evident; in particular, the system linearity has worsened, in good agreement with the theory developed in the previous sections. The relative linearity error Err_l, with respect to the full scale of the measurand x (i.e., 2) has been computed as $Err_l = (<x>_{lin} - x)/2$. The worst case happens when $x = 0.45$; Err_l varies from about 0.5% to about 7.9% with increasing values of C_p.

The second step of this test consists of repeating the previous measurements with the complete setup of Fig. 3.43, i.e., with the proposed stray capacitance compensation system in action. Table XVI shows the obtained values of relative linearity error Err_{lin}. It can be noticed that the worst case happens again for $x = 0.45$; the linearity error is quite uniform over all the considered C_p range and it has a maximum value of 2.2%, thus significantly improving the previous value of 7.9%. Unfortunately, for lower values of C_p, the compensation system has worsened the system performance, since Err_{lin} has become more than 2%, starting from about 0.5% without compensation. In fact, the $<x>_{lin}$ has been computed using an LMS calibration performed on the setup without the compensation system. The compensation system has some negative side effects on the setup, i.e., a distortion of the emulated sensor behavior, due to the presence of the shunt resistors R_{sense} (see Fig. 3.40).

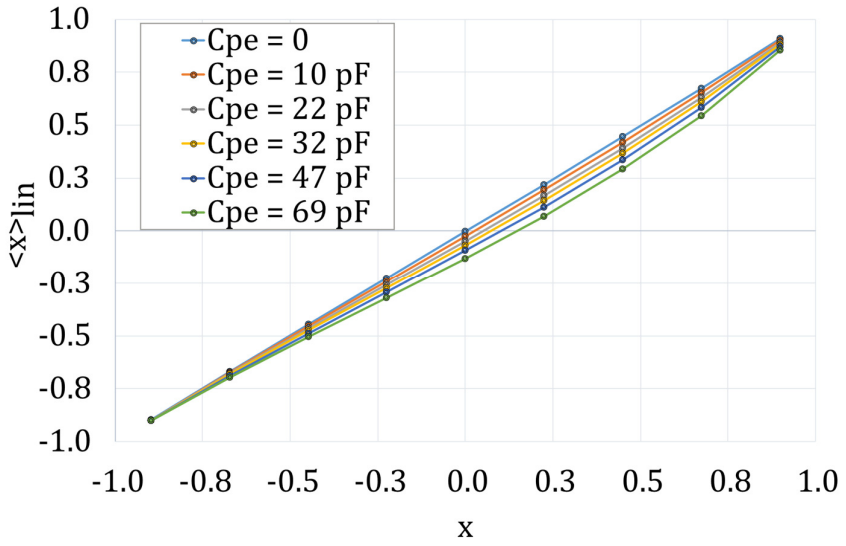


Figure 3.45 The estimated linearized sensor measurand <x> versus the emulated value x, with different scenarios of Cpe values.

Table XVI Relative linearity error of the readout system including the stray capacitance compensation. Linearization is performed on the system without compensation.

	C_{pe} [pF]					
x	**0**	**10**	**22**	**32**	**47**	**69**
0.90	1.4%	1.4%	1.4%	1.4%	1.3%	1.3%
0.67	2.0%	2.0%	1.9%	1.9%	1.9%	1.9%
0.45	2.2%	2.2%	2.2%	2.2%	2.1%	2.1%
0.22	2.1%	2.1%	2.1%	2.1%	2.1%	2.0%
0.00	1.9%	1.9%	1.9%	1.9%	1.8%	1.8%
-0.22	1.6%	1.6%	1.6%	1.6%	1.6%	1.6%
-0.45	1.3%	1.4%	1.4%	1.4%	1.4%	1.4%
-0.67	1.0%	1.0%	1.0%	1.0%	1.0%	0.9%
-0.90	0.2%	0.2%	0.2%	0.2%	0.2%	0.1%

These effects are dominant with lower values of C_p, whereas with larger values of C_p are negligible with respect to the beneficial action of the capacitance compensation.

However, a new calibration procedure by means of LMS and considering the experimental data from the complete setup can be performed. Similarly to the previous case, the new values of $<x>$ with $C_p = 0$ have been considered for the linear regression, obtaining the new parameters m_{i+c} and p_{i+c} to be used to compute $<x>_{\text{lin}} = m_{i+c} \cdot <x> + q_{i+c}$.

Table XVII reports the values of relative linearity error Err_{lin} obtained with the new linearization process. It is evident that a general improvement, with respect to the situation without the compensation system, has been achieved, over all the measurand x range as well as considered parasitic capacitance C_p. In particular, a linearization error better than 1% has been obtained, thanks to the proposed approach.

Table XVII Relative linearity error of the readout system including the stray capacitance compensation. Linearization is performed on the system with compensation.

	C_{pe} [pF]					
x	0	10	22	32	47	69
0.90	0.8%	0.8%	0.8%	0.8%	0.8%	0.8%
0.67	0.1%	0.1%	0.1%	0.1%	0.1%	0.1%
0.45	0.4%	0.3%	0.3%	0.3%	0.3%	0.3%
0.22	0.4%	0.4%	0.4%	0.4%	0.4%	0.3%
0.00	0.3%	0.3%	0.3%	0.3%	0.3%	0.3%
-0.22	0.3%	0.3%	0.3%	0.3%	0.2%	0.2%
-0.45	0.1%	0.2%	0.2%	0.2%	0.2%	0.2%
-0.67	<0.1%	<0.1%	<0.1%	<0.1%	<0.1%	0.1%
-0.90	0.6%	0.6%	0.6%	0.5%	0.6%	0.6%

3.4.4 Discussion

Capacitive sensors are widely used due to the many advantages they offer, including simple integration with the readout circuit. Differential configuration is often adopted to minimize common mode noise. Unfortunately, no matter the readout circuit, stray capacitances can adversely affect performance. In this paragraph, a novel approach aimed to ideally nullify the effects of ground-referred parasitic capacitances is presented. The system is designed around an automatic feedback loop, which drives a voltage-controlled negative impedance converter, continuously counteracting the estimated parasitic capacitance. An experimental setup has been purposely designed to test feasibility and effectiveness. In particular, using an emulated sensor, it has been possible to improve its performance from a worst-case relative linearity error of 7.9% down to less than 1%. (with sensor baseline C_{bl} of about 225 pF and parasitic capacitance on the order of tens of picofarads). As a concluding remark, the proposed solution is not limited to capacitive sensors, but can be applied all those situations where AC-excited differential sensors are employed.

4 CURRENT MODE DIFFERENTIAL CAPACITIVE SENSOR INTERFACES: STATE OF THE ART

In analogy with chapter 2, here we analyze the state of the art about how it is possible to interface a differential capacitance sensor with an analog interface based on a current mode approach. Unlike for the voltage mode, where the meaning of the definition was broader, there are not many works in the literature concerning current mode readout techniques, and almost all of them can be reconducted to a basic theory which will be introduced in the following pages.

Nevertheless, current mode operation has many benefits with respect to the voltage mode, specifically it allows to achieve good dynamic range maintaining very low voltage levels, current mode circuits are inherently simpler than voltage mode ones allowing a better integration and higher readout frequencies. One of their main drawbacks is the sensitivity to parasitic capacitances that, indeed, is addressed in the interfaces that are analyzed in the following pages.

This chapter will consider both 'standard' devices solutions, which are typically integrated solutions, since operations with currents at integrated level are relatively simple thanks to current mirror structures and 'non-standard' approaches based on

active devices like second generation current conveyors (CCIIs). Note that the definition standard and non-standard is only used to diversify the approaches.

4.1 Current mode theory

Let us take into consideration Fig. 4.1. It depicts the ideal configuration to approach a differential capacitive sensor in a current mode fashion. C_1 and C_2 represent the differential capacitive sensor, while I_{ref} is a constant reference current injected into the sensor itself. The injected current will be split into two portions I_1 and I_2 which depend on the actual value of C_1 and C_2. By the performing the subtraction between the two currents, it is possible to evaluate the ratiometric parameter x as follows:

$$I_1 - I_2 = \frac{C_1}{C_1 + C_2} I_{ref} - \frac{C_2}{C_1 + C_2} I_{ref} = I_{ref} x \tag{4.1}$$

Noticeably, a peculiarity of the current mode approach is that the sensitivity of the interface can be easily tuned by adjusting the reference current itself. This obviously has a drawback: an increment in the sensitivity of the interface comes at the expenses of an increased power consumption. Fig. 4.2 depicts a more realistic picture of this same approach. As visible, other than the sensor and the reference current, parasitic capacitances have been added.

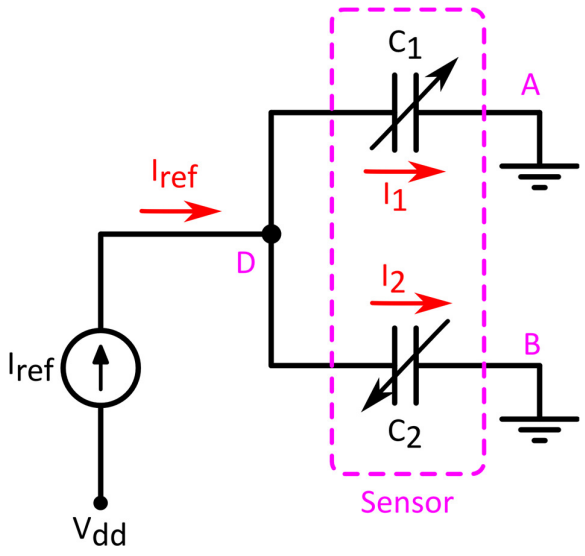


Figure 4.1 Ideal current mode approach.

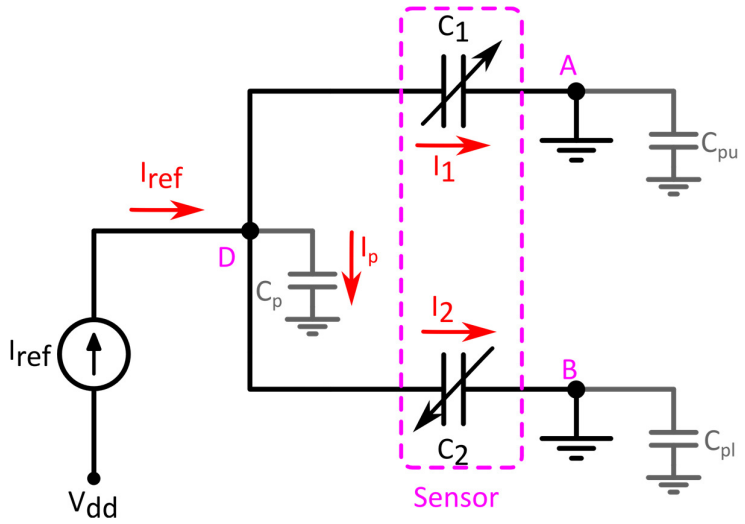


Figure 4.2 Current mode approach in presence of parasitic capacitances.

C_{pu} and C_{pl} are negligible for this analysis given that they are grounded (the actual interface has to guarantee this condition in order for this analysis to be valid).

As a consequence, it is necessary to rewrite currents I_1 and I_2 as:

$$I_1 = \frac{C_1}{C_1 + C_2 + C_p} I_{ref}$$
$$I_2 = \frac{C_2}{C_1 + C_2 + C_p} I_{ref} \quad (4.2)$$

Therefore, their difference results equal to:

$$I_1 - I_2 = \frac{C_1}{C_1 + C_2 + C_p} I_{ref} - \frac{C_2}{C_1 + C_2 + C_p} I_{ref} =$$
$$= I_{ref} \frac{C_1 + C_2}{C_1 + C_2 + C_p} x \quad (4.3)$$

Recalling from chapter 1 that the sum of the actual values of C_1 and C_2 for linear sensors remains constant regardless of the measurand:

$$C_1 + C_2 = 2C_{bl} \quad (4.4)$$

where C_{bl} represents the baseline (or standing value) of the sensor, and noticing that, although function of the measurand, the sum of C_1 and C_2 for hyperbolic sensors can be expressed as:

$$C_1 + C_2 = \frac{2C_{bl}}{1 - x^2} \tag{4.5}$$

we can rewrite Eq. 4.3 as follows:

$$I_1 - I_2 = \frac{I_{ref}}{1 + \frac{C_p}{2C_{bl}}} x \tag{4.6}$$

$$I_1 - I_2 = \frac{I_{ref}}{1 + (1 - x^2)\frac{C_p}{2C_{bl}}} x \tag{4.7}$$

Eq. 4.6 stands for linear sensors, while Eq. 4.7 for hyperbolic. The conclusions given in chapter 1 are also valid for the current mode approach: the presence of a parasitic capacitance at the terminal D of the sensor determines a constant reduction in the reference current for linear sensors (loss of sensitivity), while a reduction that is a function of the measurand itself, in the case of hyperbolic sensors (with consequent distortion in the input-output relationship).

These effects can be negligible for high baseline sensors (thousands of pF, where $C_p/2C_{bl} \rightarrow 0$) but greatly affect the readout for small baseline sensors (few pF or fF range).

4.2 Standard device interfaces

The first current mode interface proposed in this chapter is shown in Fig. 4.3 and analysed in [55]. Although sensitive to parasitic capacitances, it is designed to remain extremely low in complexity and symmetrical so to ensure high readout speeds, low power consumption and rejection common mode disturbs and to switching error.

It is composed by two switches placed in parallel with the actual sensor and an analog block which performs the subtraction of the two currents I_1 and I_2. The injection of a constant reference current I_{ref} causes an indefinite increment of the voltage at the D terminal of the sensor, inducing its saturation.

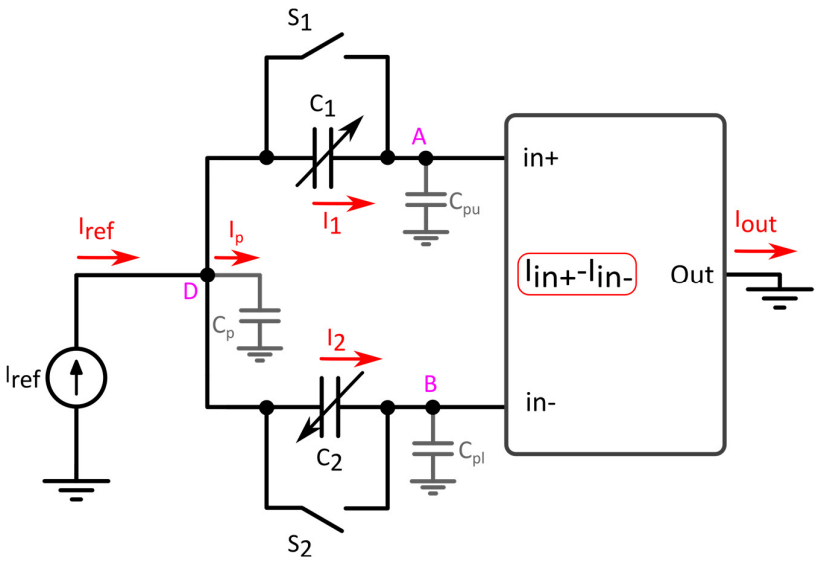


Figure 4.3 Block diagram of the proposed interface [55].

Switches are therefore activated by an external clock signal in order to provide a continuous discharge of the sensor between each measurement. For this reason, the actual measurement consists of two phases: the discharge phase (T_D) and the readout phase (T_M). During the discharge phase, S_1 and S_2 are closed, so to provide the discharge of the sensor and a zero current at the output; whereas once the switches are opened, the exact subtraction shown in Eq. 4.3 is performed.

During the measuring phase, the voltage at the D node can be expressed as:

$$\boldsymbol{V_D = \frac{I_{ref}}{C_1 + C_2 + C_p} T_M} \qquad \textbf{(4.8)}$$

From this equation, it comes that it is possible to tune T_M and I_{ref} according to the values of the sensor capacitors and the parasitic equivalent capacitor C_p.

The actual implementation of both the subtracting section and the switching one are proposed in Fig. 4.4. Starting from the current subtracting section, the improved solution consists of a cascoded unitary current mirror $M_{1a,b}$, $M_{2a,b}$ whose DC voltage is set through the biasing voltage V_B. Fixed current sources I_{B1} and I_{B2} have the same value. Given the negative feedback employed by M_{1a}, the virtual ground at the negative input is strong, whereas the same is not verified at the positive terminal. Therefore the overall reference current has to remain below the bias current to preserve the virtual ground at that node.

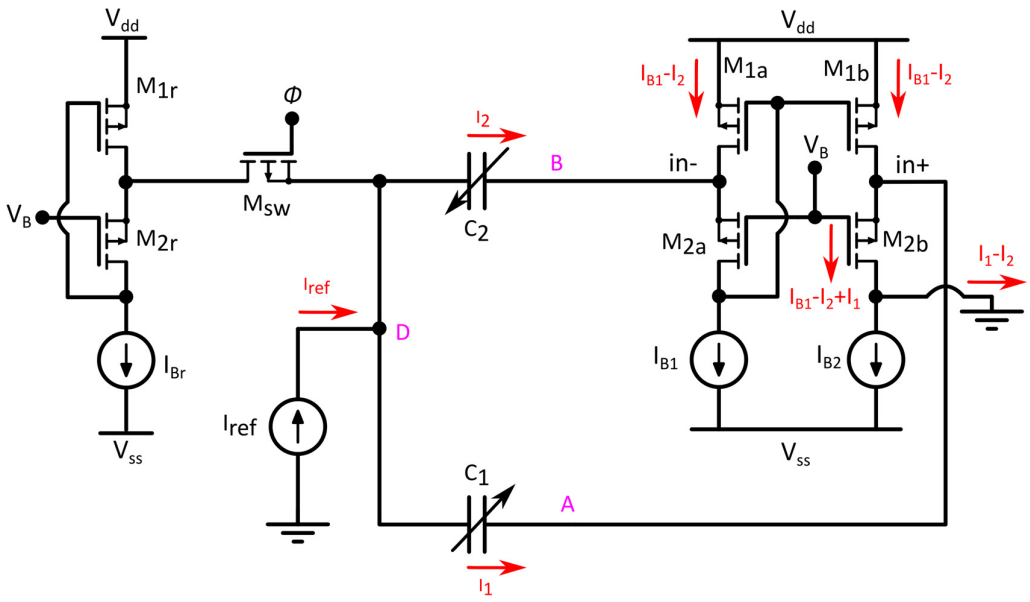


Figure 4.4 Actual implementation of the interface under analysis [55].

The switching section is composed by a single pass transistor M_{sw} and a common gate section M_{2r} and M_{1r} offering low input impedance and mirroring M_{2a} and M_{1a}. In this way, when C_1 and C_2 are discharged, the charge stored in C_p is not transferred to the output, unlike how shown in Fig. 4.3.

Both clock feedthrough and charge injection can be neglected: the first one, as already stated in chapter 3, depends on the ratio between the overlap capacitance of the switching transistors and the total capacitance seen by the switching transistors themselves. The former obviously depends on technology parameters, but in general, being here a single switch solution, the overlap capacitance of M_{sw} is considerably lower than the sum of C_1, C_2 and C_p. Therefore, clock amplitude transferred to the sensor tends to zero. Charge injection can be neglected because, during switching phases, injected charges are drained by the low impedance M_{1r}, M_{2r} path. The overall main inaccuracy source is given by mismatches between paired transistors. This interface can be profitably used for linear sensors where the gain error is constant regardless of the measurand, or in high baseline hyperbolic sensors where the effects of stray capacitances can be neglected a priori.

A more advanced interface capable of dynamically compensate parasitic capacitances is given in Fig. 4.5 [56]. It can be thought of as a direct evolution of the previous one [55]. As visible, the sensor is again depicted together with the parasitic capacitance at terminal D, and it is connected to a fully analog processing block, that,

thanks to its low input impedance, provides a virtual ground at its inputs, ideally nullifying stray capacitances at nodes A and B of the sensor. The analog block has two high impedance outputs where the sum and the subtraction of the input currents is produced.

The transconductance amplifier is demanded to generate a current which, once fed back to the sensor, provides a compensation for that portion of the reference current that is 'stolen' from C_p to the actual sensor itself.

There are three switches driven by two different clocks (Φ_1 and Φ_2, see Fig. 4.7). Both the clocks share the same frequency ($1/T$) but different duty cycles. According to the switches status, the sensor readout is carried out in three steps, namely discharge (T_D), autotune (T_A), measure (T_M); the overall period of the reference signal is therefore $T=T_D+T_A+T_M$.

During the discharge phase, switches are all closed. This ensures that the sensor is fully grounded (hence gets discharged), and that the transconductance amplifier output is equal to zero due to the fact that both its inputs are grounded as well. In other words this is a reset state and makes sure that at each cycle (T), the starting condition remains unchanged.

The autotune phase (evidenced Fig. 4.6) starts when switches S_1 and S_2 turn open. Current starts flowing through C_1, C_2 and C_p. Ideally ($C_p = 0$), the sum of I_1 and I_2 is equal to I_{ref}, but due to the presence of C_p, part of this current is absorbed by that capacitance. By looking then at the summing output, and by choosing I_{comp} equal to I_{ref}, if $I_1 + I_2$ is different from I_{comp}, the voltage across R_0 changes accordingly. This value is stored in C_H. The inputs of the transconductor (feedback controller) become of different values and a current proportional to the 'error signal' starts flowing from its output towards C_p.

The measure phase starts when the switch S_3 opens. The resulting voltage coming from the autotune phase is held by C_H while the total amount of current that drives the sensor is equal to:

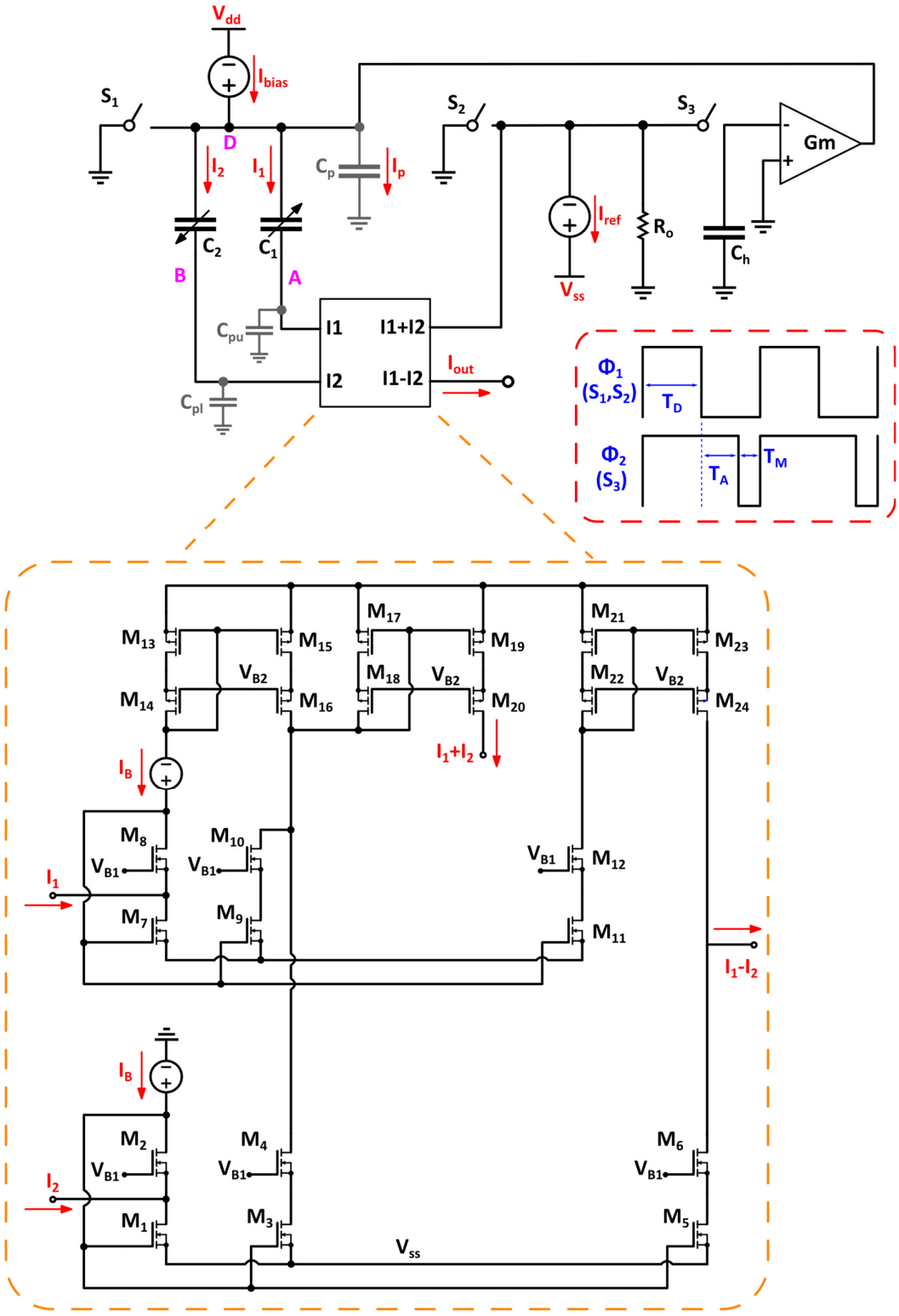


Figure 4.5 Block diagram of the interface proposed in [56] and a focus on the summing subtracting block and clock signals timings.

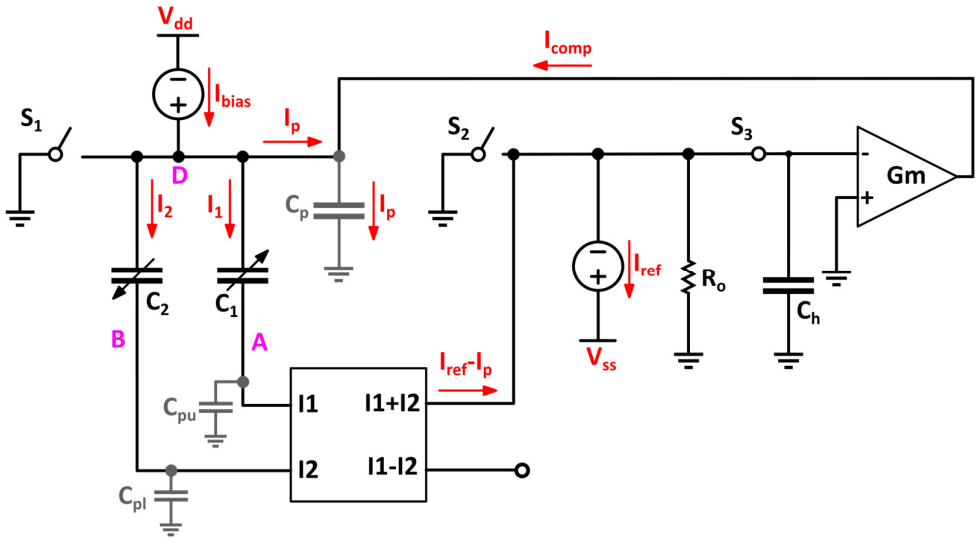


Figure 4.6 Block diagram of the interface during the autotune phase [56].

$$I_{TOT} = I_{ref} + G_M R_O (I_{COMP} - I_1 - I_2) \tag{4.9}$$

Currents I_1 and I_2 can be expressed as follows:

$$I_1 = \left(I_{ref}(1 + A) - A(I_1 + I_2)\right)\frac{C_1}{C_T} \tag{4.10}$$

$$I_2 = \left(I_{ref}(1 + A) - A(I_1 + I_2)\right)\frac{C_2}{C_T} \tag{4.11}$$

where, in the previous equations, I_{COMP} is replaced by I_{ref}, $C_1+C_2+C_p$ is equal to C_T and A is equal to $G_M R_O$.

Since the sum of I_1 and I_2 can be uniquely expressed as:

$$I_1 + I_2 = I_{ref}\frac{(1 + A)(C_1 + C_2)}{C_T + A(C_1 + C_2)} \tag{4.12}$$

their difference can be consequently calculated (by using equations 4.10-4.12 and 4.4) as:

$$I_1 - I_2 = \frac{I_{ref} 2C_{bl}}{\frac{C_T}{1 + A} + 2C_{bl}} x \tag{4.13}$$

for linear sensors, while (using equations 4.10-4.12 and 4.5) as:

$$I_1 - I_2 = \frac{I_{ref}}{1 + (1 - x^2)\frac{C_p}{2C_{bl}(1+A)}} x \tag{4.14}$$

for hyperbolic ones. In both the cases, when A tends to infinite, the equation tends to the ideal one (Eq. 4.1).

The frequency of the clock signal as well as the amplitude of the reference current can be set according to the maximum voltage that the designer wants the node D to reach, in particular:

$$V_D = \frac{I_{ref} + I_{GM}}{C_1 + C_2 + C_p} T_M \tag{4.15}$$

Obviously, for a higher reference current, the measurement can be faster. Increasing the reference current improves also the resolution of the interface, at expenses of power consumption which for this topology has to take into account also the comparison current I_{COMP}.

4.3 CCII based interfaces

In this we will examine how it is possible to approach differential capacitance sensors interfacing by using the second generation current conveyor (CCII) as the main active block. Although the constitutive relationships are given in the following lines, Chapter 6 will give a better overview about this active current mode block, putting also in evidence novelties that we have introduced in this field during this Ph.D.

A CCII based interface is shown in Fig. 4.7 [57]. The input-output relationship of such a device is given by the following matrix [58-59]:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & 0 & 0 \\ 0 & \pm\beta & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{4.16}$$

Parameters α and β should be close to unity, so that the voltage on the Y terminal is conveyed to the X terminal, while the current on the X terminal is conveyed to the Z terminal. According to the verse of the currents on X and Z, it is possible to identify positive and negative current conveyors, that is why β has a sign.

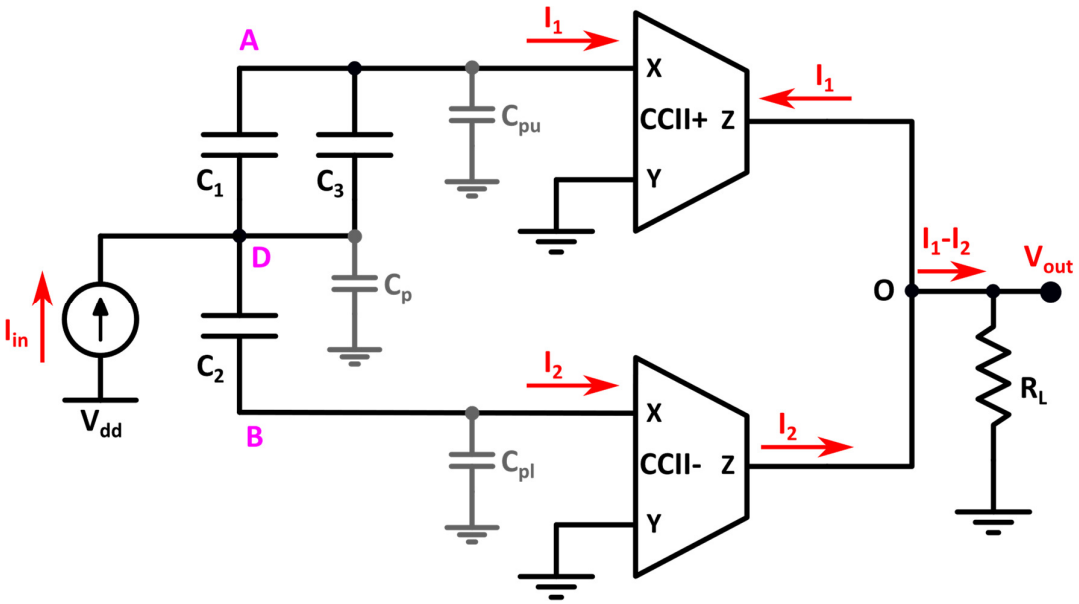


Figure 4.7 CCII based differential capacitive sensor interface [57].

The interface is composed by a CCII+ and a CCII-, while the differential capacitive sensor is connected to the low impedance *X* terminal of the active devices. An oscillating current source drives the common terminal *D* of the sensor. Given the conveying action between *Y* and *X* terminals, connecting the former to ground theoretically nullifies parasitic capacitances C_{pu} and C_{pl}, while C_p remains uncompensated. The difference at node *O* is automatically carried out thanks to the inversion of I_2 current which is given by the CCII- (refer to Fig. 4.7). Capacitor C_3 adds an overall offset to the output signal so that, if suitably dimensioned, allows to translate the input-output relationship to positive voltages even for negative values of *x*.

The output is given in form of a voltage across the resistor R_L and, supposing ideal CCIIs can be expressed as:

$$V_{out} = R_L I_{in,pp}\left(\frac{C_1 + C_2}{C_1 + C_2 + C_3}x + \frac{C_3}{C_1 + C_2 + C_3}\right) \qquad (4.17)$$

The properties of the CCII can be profitably exploited to use an oscillating voltage rather than current in order to produce the reference signal, as shown in Fig. 4.10. As visible, a third CCII is added. At its *Y* terminal, the reference voltage is connected; it is converted into a current at *X* terminal thanks to the resistor R_1, and finally, it is conveyed to the *Z* terminal for the readout.

The input-output relationship can be written as:

$$V_{out} = \frac{R_L V_{in,pp}}{R_1}\left(\frac{C_1 + C_2}{C_1 + C_2 + C_3}x + \frac{C_3}{C_1 + C_2 + C_3}\right) \tag{4.18}$$

Noticeably, since a negative CCII can be implemented by a pair of positive CCIIs (Fig. 4.9), at the expenses of an increment in area occupation, the interface can be implemented using a single active block.

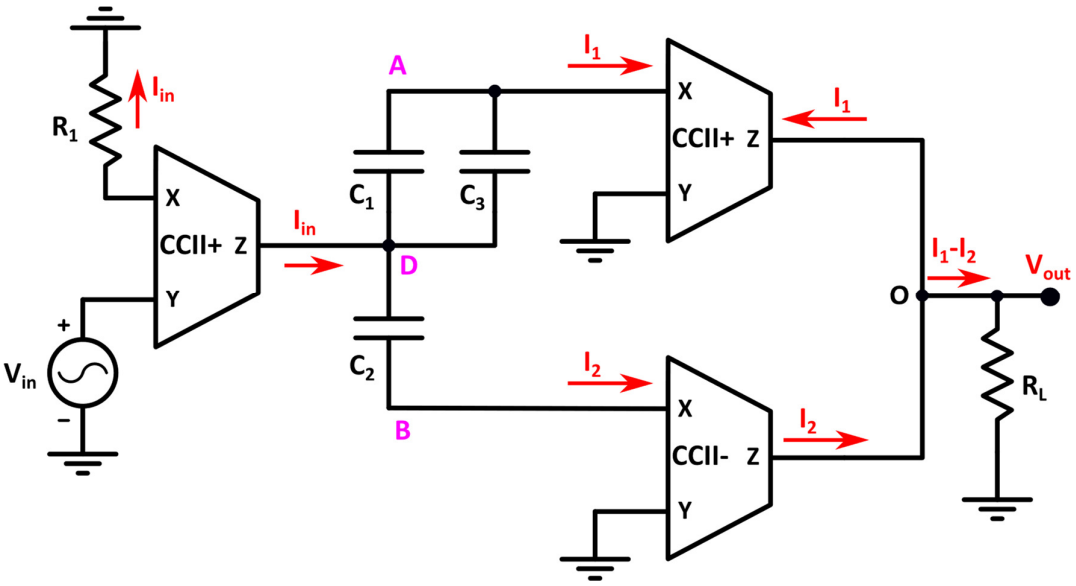


Figure 4.8 CCII based interface with a reference voltage generator [57].

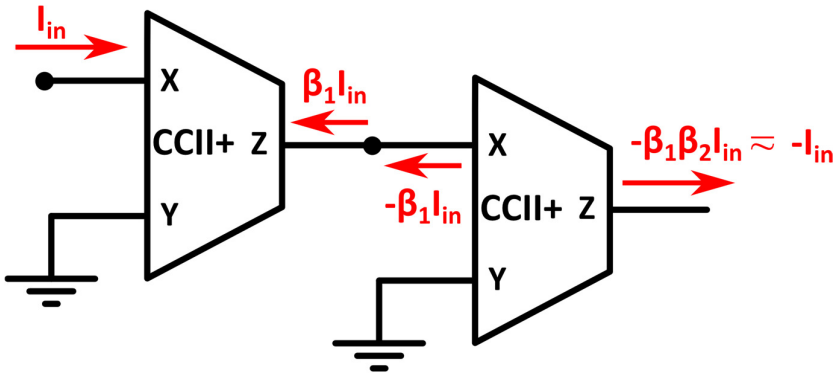


Figure 4.9 A negative CCII implemented by means of two positive CCIIs; it is supposed that the β parameter is close to unity so that can be neglected in the input-output relationship.

5 VCII BASED STRAY INSENSITIVE INTERFACE

In this chapter we will show the results of the research conducted during the last part of the Ph.D. degree, on the current mode approach for interfacing differential capacitive sensors. In particular, rather than relying on common approaches such as ones shown in the previous chapter, we tried to theorize and synthesize a novel current mode active block, the VCII, detailed in Chapter 6, which then we employed with the aim of designing a natively parasitic insensitive, current mode interface for differential capacitive sensors.

5.1 Introduction on the VCII

As the dual device of the CCII, a second generation voltage conveyor is a three terminals device, whose input-output relationships can be extracted from the following matrix [60-62]:

$$\begin{bmatrix} \boldsymbol{i_x} \\ \boldsymbol{v_y} \\ \boldsymbol{v_z} \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \pm\boldsymbol{\beta} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{\alpha} & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{v_x} \\ \boldsymbol{i_y} \\ \boldsymbol{i_z} \end{bmatrix} \tag{5.1}$$

The α and β parameters (ideally unity) share the same meaning respect to the CCII block, so they represent the ratio between voltages and currents respectively. However, for a VCII the current mirroring action is carried out between the Y and X

*The work presented in this chapter was published by the authors in [63].

terminals, $I_X = \pm\beta I_Y$, while the voltage at the X terminal is conveyed to the output Z terminal $V_Z = \alpha V_X$. The Y terminal, due to its very low input impedance can be considered at virtual ground ($V_Y = 0$).

From a designer perspective, a voltage conveyor results more versatile with respect to current conveyors.

5.2 Theory of operation

The presented interface, other than the readout of the sensor, aims to dynamically compensate node D parasitic capacitance (C_p) by using a time continuous current feedback approach.

The circuit (see Fig. 5.1) can be divided into three parts: the *first part* is a VCII-based current summing-subtracting block composed of $VCII_1$–$VCII_2$ and a current source equal to I_{ref}. The sensor input is excited by a current source equal to $2I_{ref}$. Reference currents are square wave signal. By this solution, the charging and discharging of capacitors are automatically performed without any need to use switches. Virtual ground and low impedance at Y terminal of VCII keep the sensor second terminal to ground allowing the mitigation of C_{pu} and C_{pl} stray capacitances.

In this section, the sum of I_1 and I_2 is produced and the result is subtracted from I_{ref} to obtain I_{fb} (error signal), which, suitably integrated, generates the current taken by C_p (I_{out} tends to $-I_p$).

The *second part* is the control section, which feeds I_{fb} to the sensor input. As it is shown in Fig. 5.1, it is a VCII-based current-input current-output integrator composed of the two VCII blocks, a resistor, and a grounded capacitor.

In the *third part* (output stage), the difference between I_1 and I_2 is produced and converted to a proportional voltage signal. This operation is performed by three VCII blocks ($VCII_3$–$VCII_5$) and resistor R_g.

Currents I_1 and I_2 can be written, respectively, as:

$$\boldsymbol{I_1 = \lambda(2I_{ref} - I_p)} \qquad \textbf{(5.2)}$$

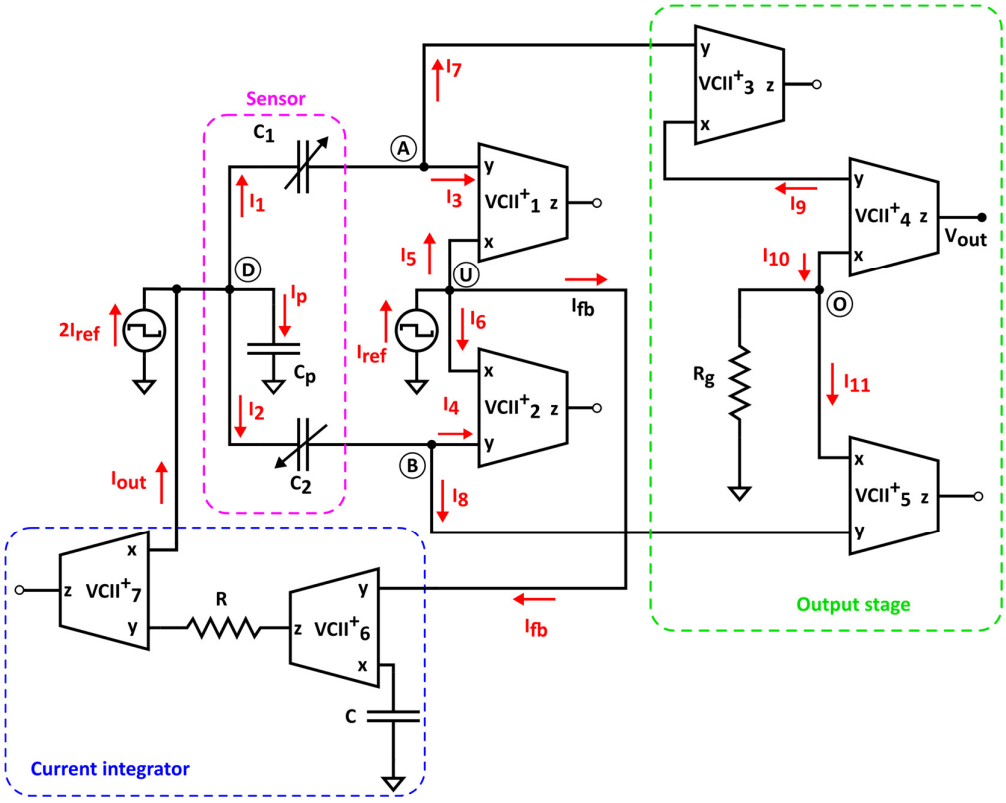


Figure 5.1 The proposed VCII based interface with automatic parasitic compensation [63].

$$I_2 = (1-\lambda)(2I_{ref} - I_p) \tag{5.3}$$

Therefore, currents I_3, I_4, I_7 and I_8 can be expressed as:

$$I_3 = I_7 = \frac{I_1}{2} = \frac{\lambda}{2}(2I_{ref} - I_p) \tag{5.4}$$

$$I_4 = I_8 = \frac{I_2}{2} = \frac{1-\lambda}{2}(2I_{ref} - I_p) \tag{5.5}$$

At node U it is possible to write that:

$$I_{ref} = I_5 + I_6 + I_{fb} \tag{5.6}$$

Since $I_5 = \beta_1 I_3$ and $I_6 = \beta_2 I_4$, using equations 5.4-5.6 it is possible to conclude that:

$$I_{ref} = \beta_1 \frac{\lambda}{2}(I_{ref} - I_p) + \beta_2 \frac{(1-\lambda)}{2}(2I_{ref} - I_p) + I_{fb} \quad (5.7)$$

If β_1 and β_2 are equal to unity, Eq. 5.7 suggests that I_{fb} is equal to $I_p/2$.

In fact, at node U, a current comparing action is performed. As long as the sum of I_5 and I_6 is not equal to I_{ref} (i.e., $I_1 + I_2$ is not equal to $2I_{ref}$), a non-zero compensation current (I_{fb}) is produced. This current is fed to the input node by the controller circuit, which is a VCII-based current integrator. By assuming virtual ground at Y port of VCII, the relationship between the input and output currents of the integrator can be expressed as:

$$I_{out} = \alpha_7 \beta_7 \beta_8 \frac{1}{sRC} I_{fb} \quad (5.8)$$

Once the feedback circuit reaches the steady state (hence compensating the effects of C_p), the output voltage can be simply calculated as:

$$V_{out} = \alpha_4 V_B = \alpha_4 R_g (I_{10} - I_{11}) \quad (5.9)$$

But since I_{10} and I_{11} are, respectively, equivalent to:

$$I_{10} = \beta_4 I_9 = \beta_3 \beta_4 I_7 = \beta_3 \beta_4 \frac{I_1}{2} \quad (5.10)$$

$$I_{11} = \beta_5 I_8 = \beta_5 \frac{I_2}{2} \quad (5.11)$$

assuming the involved α and β parameters equal to unity, it is possible to conclude that:

$$V_{out} \approx \frac{R_g(I_1 - I_2)}{2} = R_g I_{ref} x \quad (5.12)$$

The sensitivity of the circuit can be adjusted by acting either on I_{ref} and on R_g:

$$S_{\Delta C}^{Vout} = \frac{dV_{out}}{d\Delta C} = \frac{d\left(R_g I_{ref} \frac{\Delta C}{C_0}\right)}{d\Delta C} = \frac{R_g I_{ref}}{C_0} \left[\frac{V}{F}\right] \quad (5.13)$$

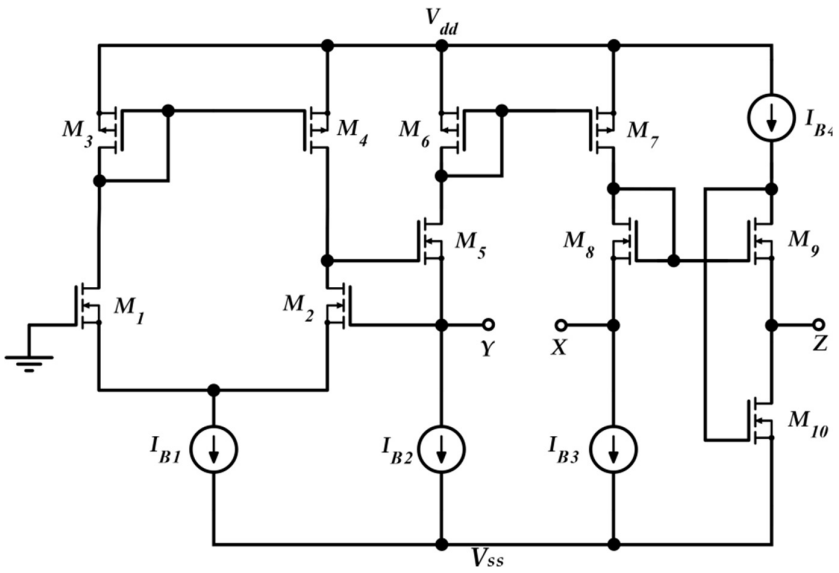
The design of the integrator (and, in general, of the feedback controller) determines the readout speed of the interface. In particular, its time constant RC must be sufficiently smaller than the half-period of the reference current I_{ref}, ensuring that the loop reaches the steady state before the reference signal changes polarity, consequently, completing an effective measurement.

5.3 Simulation results and measurements

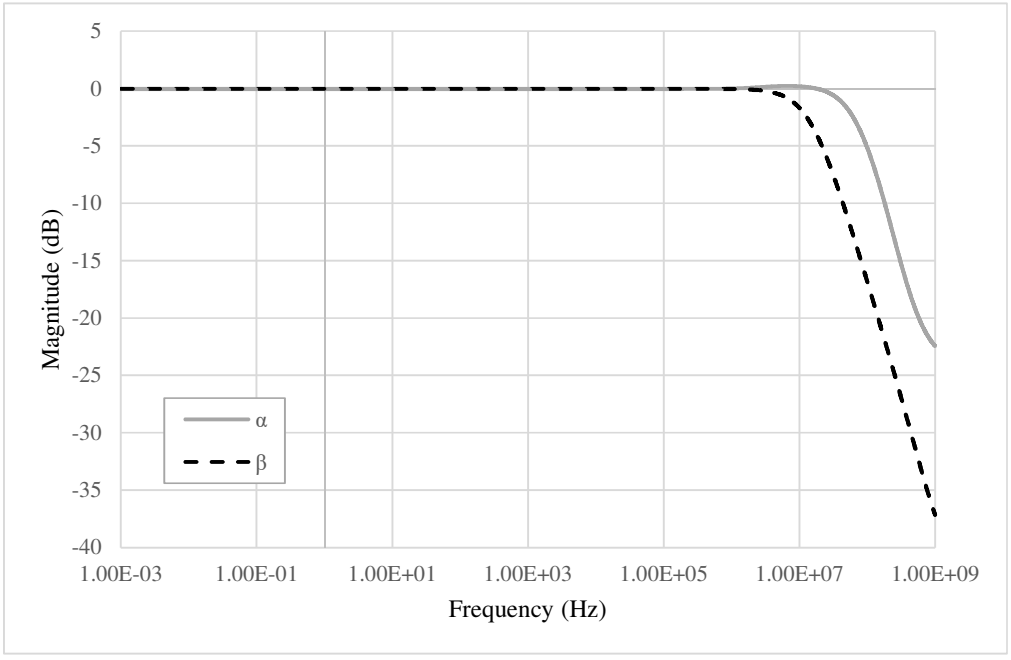
The proposed read-out circuit of Fig. 5.1 has been simulated using Spice in 0.35μm CMOS technology and a supply voltage of ±1.65 V. For the required VCIIs the circuit of [101] (Fig. 5.2a) has been used with the same aspect ratios and biasing. Current sources have been implemented by means of simple current mirrors. AC and DC performances of the VCII in terms of α and β are shown respectively in Fig. 5.2b and Fig. 5.2c. The low impedance current input (Y) is implemented by a regulated common gate (M_1-M_5), while the current transferring action is performed by the current mirror M_6, M_7. The flipped voltage follower M_9, M_{10} allow to obtain the voltage buffering between the X voltage input and the Z voltage output. The important parameters of the used VCIIs are summarized in Table XVIII.

The values of I_{ref}, R_g, R and C have been selected as 5 μA, 12 kΩ, 1 kΩ and 20 pF respectively. The frequency of I_{ref} has been chosen equal to 500 kHz to test the interface behavior close to its maximum operating condition. By setting the sensor baseline C_{bl} at 10 pF, and the parasitic capacitance C_p at 5 pF, the simulation results where the compensation loop has been first enabled and then disabled are shown in Fig. 5.3a and Fig. 5.3b respectively. For sake of clarity, the picture shows the output voltage only in the case of phase equal to zero. As visible, without the compensation, the amplitude of the output voltage reaches only 80% of full-scale. This behavior is better shown in Fig. 5.4 where the amplitude of each curve has been extracted and compared to ideal values. The full-scale error for each case has also been calculated and is shown in Fig. 5.5: with compensation, the error remains below 2.1% further proving the effectiveness of the proposed compensation technique. As it is seen, the compensation technique is very effective. It is also observed that thanks to the proposed method, the large parasitic capacitance of 5 pF has not any effect on the output voltage. In order to analyze both the effects of VCII non-idealities and the effects of mismatches on passive and active components, a mixed simulation was

carried out where a Monte Carlo analysis was performed on both PVT conditions for active devices and on tolerances for passive ones. In particular, temperature range was set from -10 °C to 80 °C, supply voltage variation from -5% to 5% of the nominal one, resistors tolerance was set to 5% while capacitor one to 10%. The overall maximum variation from the nominal reference value has been experienced at $x = 90\%$ with a deviation from the ideality of about 3 mV. These results are achieved while the circuit consumes 5.2 mW.



a)



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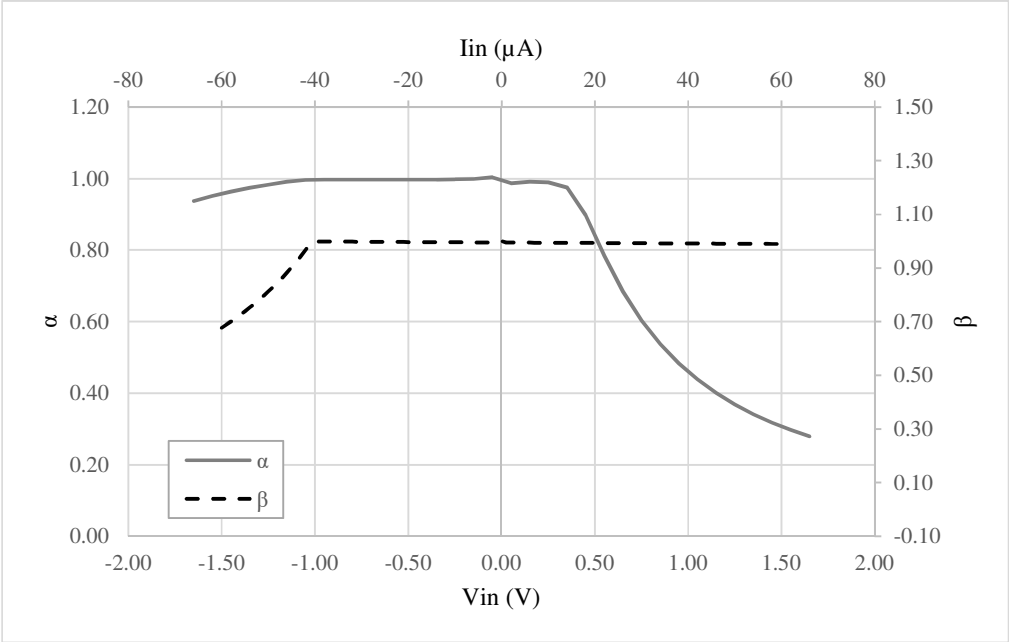
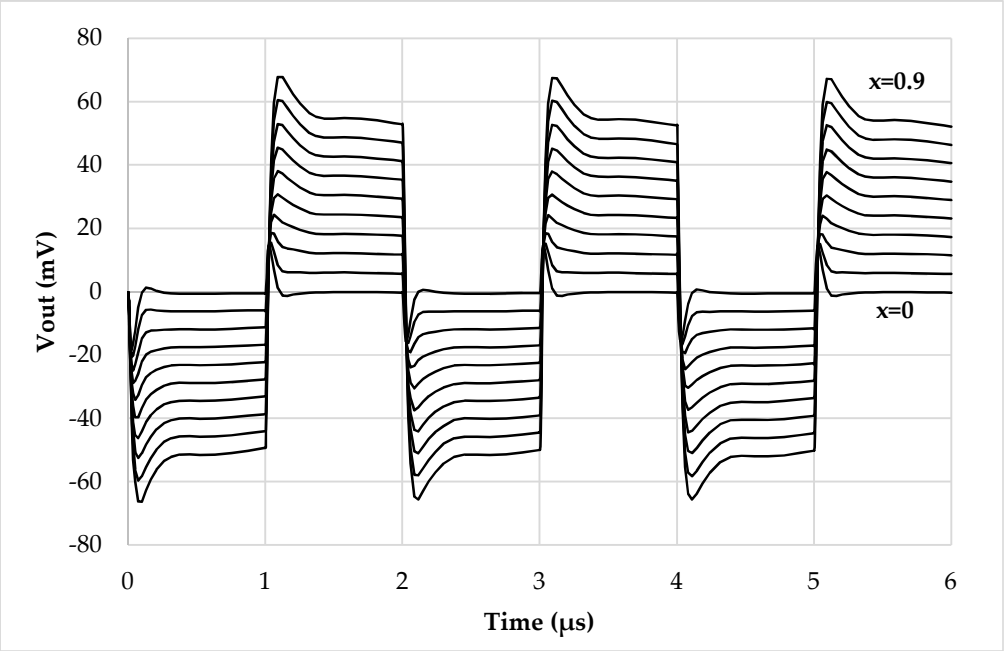


c)

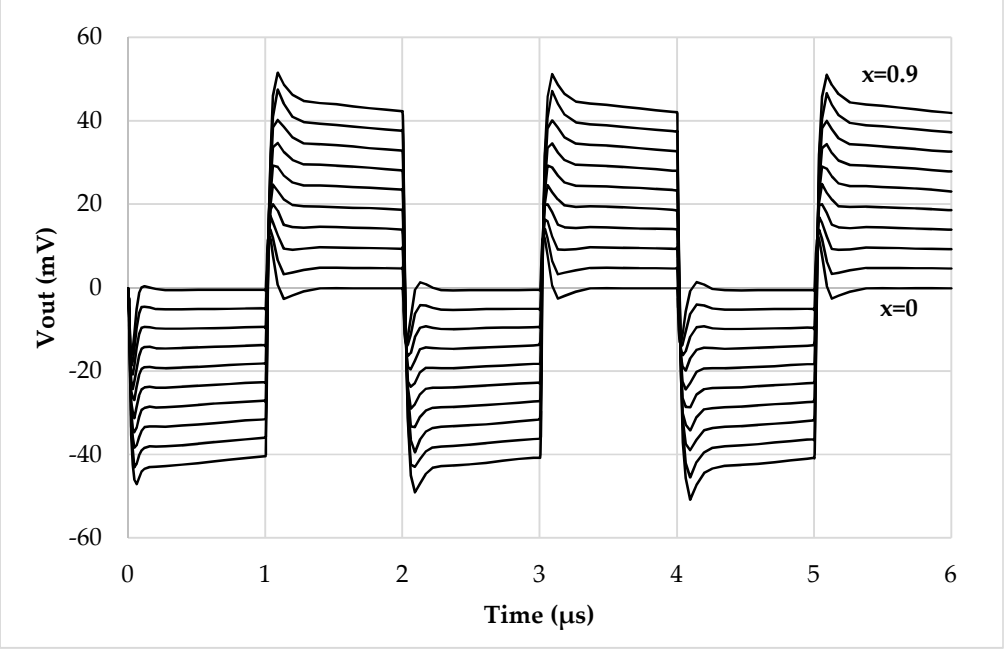
Figure 5.2 The VCII used in the simulations: a) topology (see [101]) b) AC performances (determined with a 3 pF load at X) c) DC performances (determined with a 1 kΩ load at Y for β simulations, and with a 100 kΩ load at Z for α simulations).

Table XVIII The used VCII parameters.

Parameter		*Value*
r_x		800kΩ
r_y		50Ω
r_z		80Ω
α		-43mdB
β		-45mdB
Voltage noise density at	x	342nV/√Hz
	y	420nV/√Hz
	z	118nV/√Hz
Power dissipation		0.7mW



a)



b)

Figure 5.3 Time domain output voltage with a) compensation enabled b) compensation disabled.

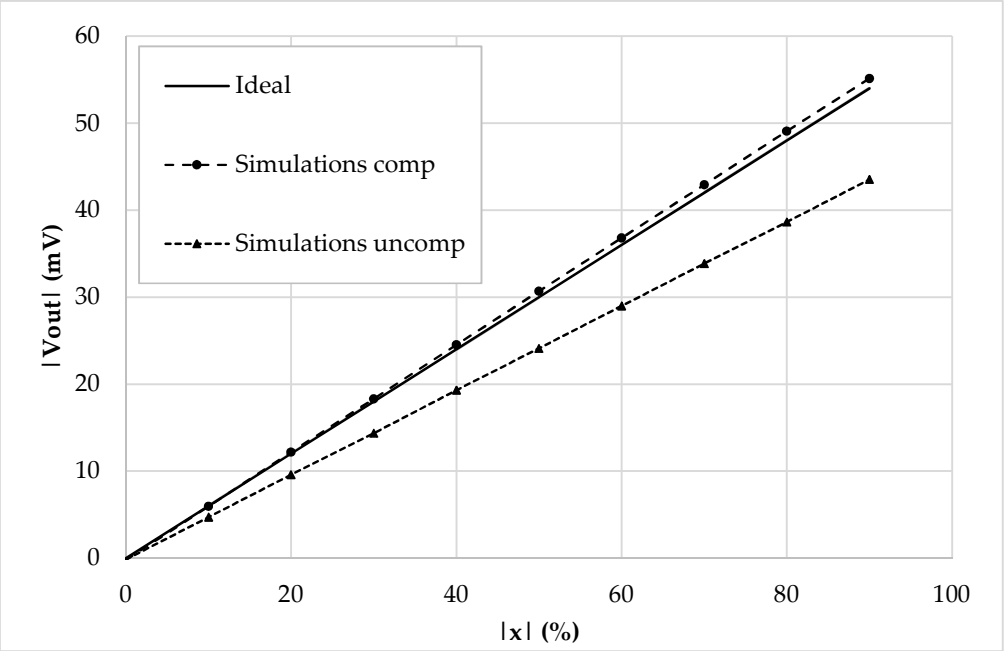


Figure 5.4 DC characteristic (|Vout| vs |x|) of the integrated interface.

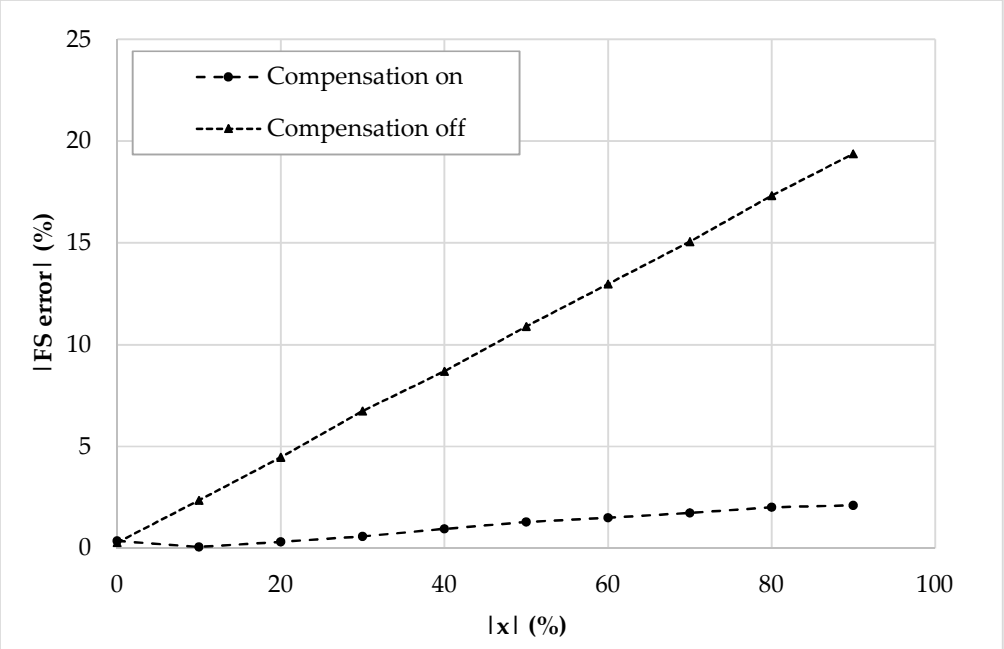


Figure 5.5 Full-scale error (%) of the compensated and uncompensated integrated interface.

To demonstrate the validity of the proposed architecture before the chip fabrication, and to obtain tangible results, a discrete version of the interface has been simulated and fabricated. The discrete VCII has been implemented as shown in Fig. 5.6 where

the current I/O of the AD844 has been used to implement a current buffer, and a simple LF411 has been suitably added to perform a voltage buffering action. Although directly available from the AD844, an external voltage buffer has been adopted in order to gain the possibility of setting an α value greater than unity. For the simulations, taking Fig. 5.1 as reference, R and C have been again set to 1 kΩ and 20 pF respectively, while R_g has been set to 33 kΩ.

Sensor baseline C_{bl} and parasitic capacitance C_p have been set to 200 pF and 120 pF respectively. The reference current I_{ref} has been set to 250 μA peak amplitude and 100 kHz frequency. Fig. 5.7 acknowledges the functionality of the discrete interface and of the compensation mechanism, showing the time domain behavior (Fig. 5.7a), the DC characteristic (Fig. 5.7b) and the full-scale error (Fig. 5.7c).

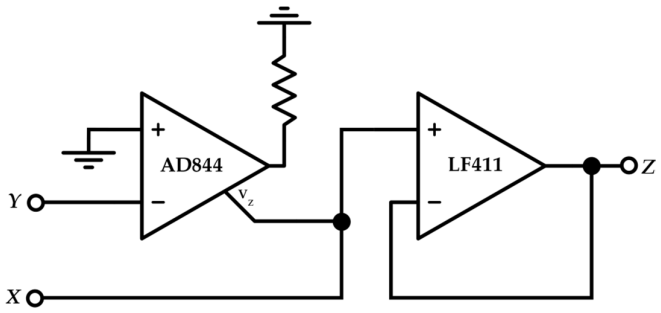
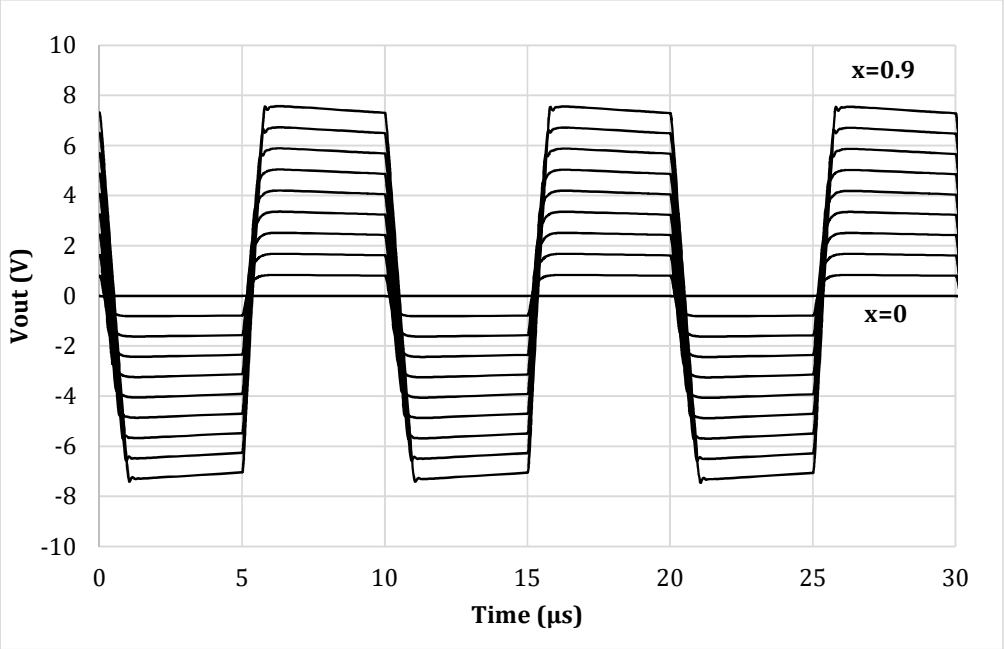
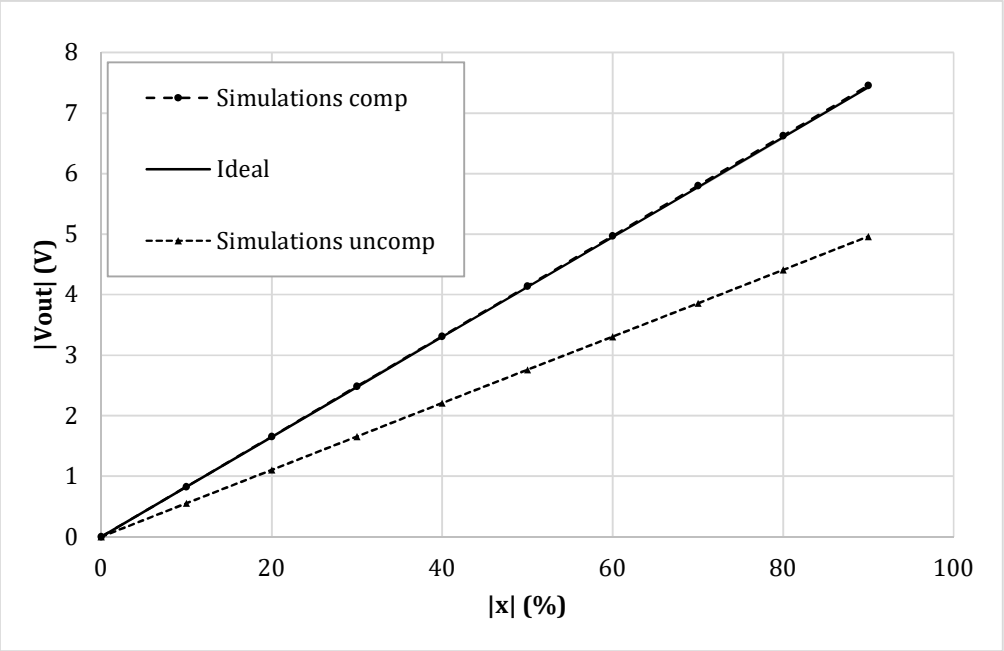


Figure 5.6 Discrete VCII implementation.



a)



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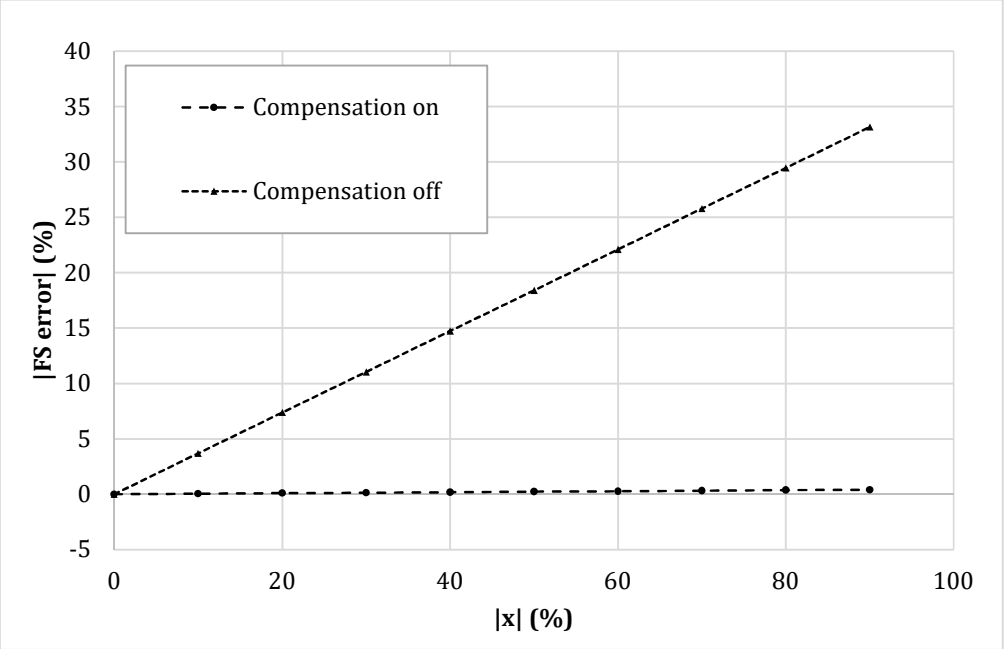


c)

Figure 5.7 Discrete interface simulations: a) time domain output voltage, b) extracted DC characteristic, c) full-scale error (%).

In Fig. 5.8 the prototyped board is shown. All the parameters have been set to match the ones used in the simulation environment. The reference current has been generated through a Keysight 33600A signal generator which, together with two resistors and two current buffers, has been able to output accurate values of 250 µA and 500 µA for I_{ref} and $2I_{ref}$. The output voltage has been measured through a Keysight MSOX3054T oscilloscope and a Keysight N2843A probe. To emulate the behavior of a 200 pF baseline linear differential capacitive sensor (Fig. 1.11a), a set of reference capacitors has been used. The test bench allows to freely add parasitic capacitances so to mimic even harsh conditions when stray capacitances are comparable to the baseline of the sensor. The time domain measurements are reported in Fig. 5.9, while Fig. 5.10 shows the DC characteristic of the prototype board. As visible, the behavior of the interface is very close to the simulations and the full-scale error (Fig. 5.11) remains always below the 2.5%. The maximum linearity error is equal to 0.9%FS. The presented setup allows to obtain a sensitivity of 21 mV/pF.

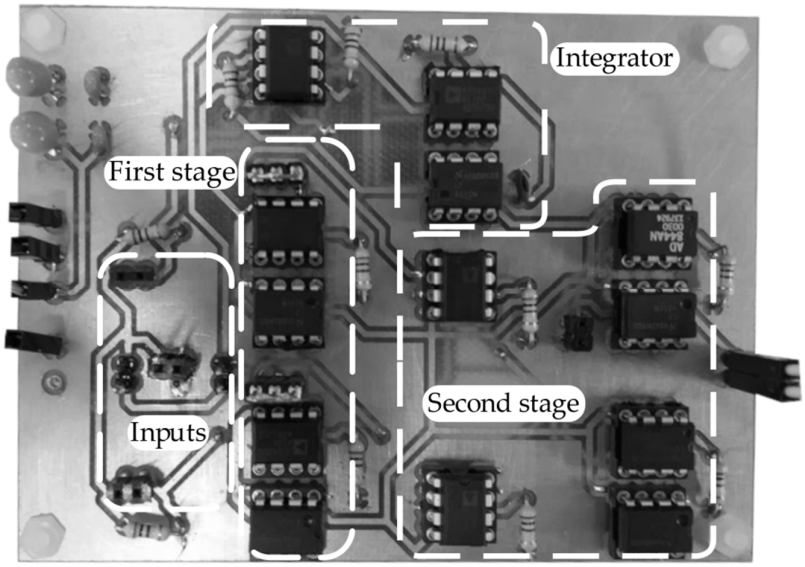


Figure 5.8 The prototyped interface.

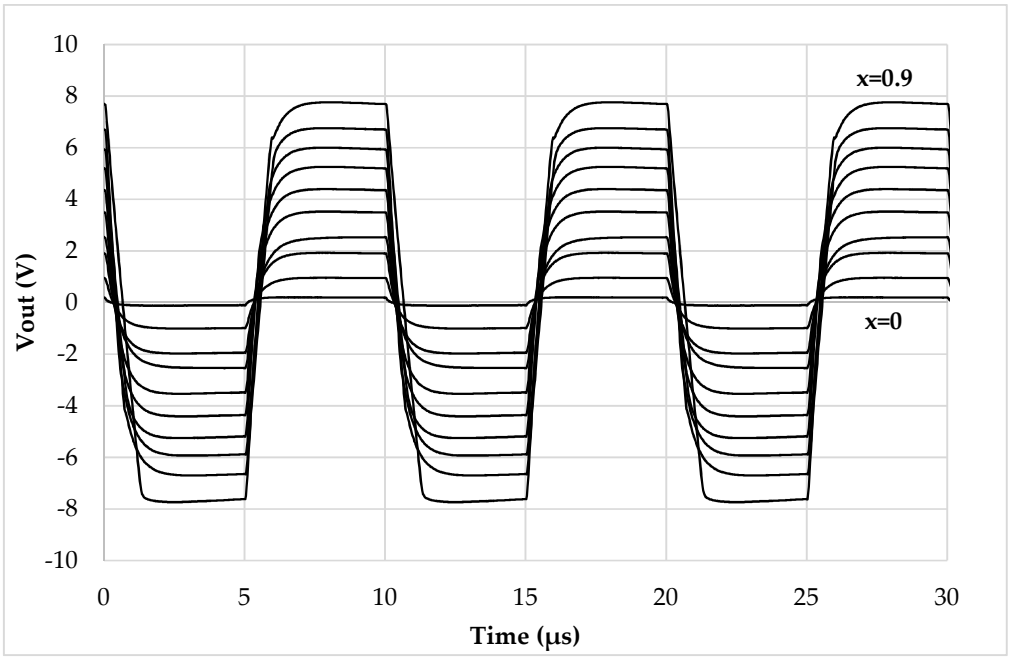


Figure 5.9 Time domain output voltage of the prototyped interface.

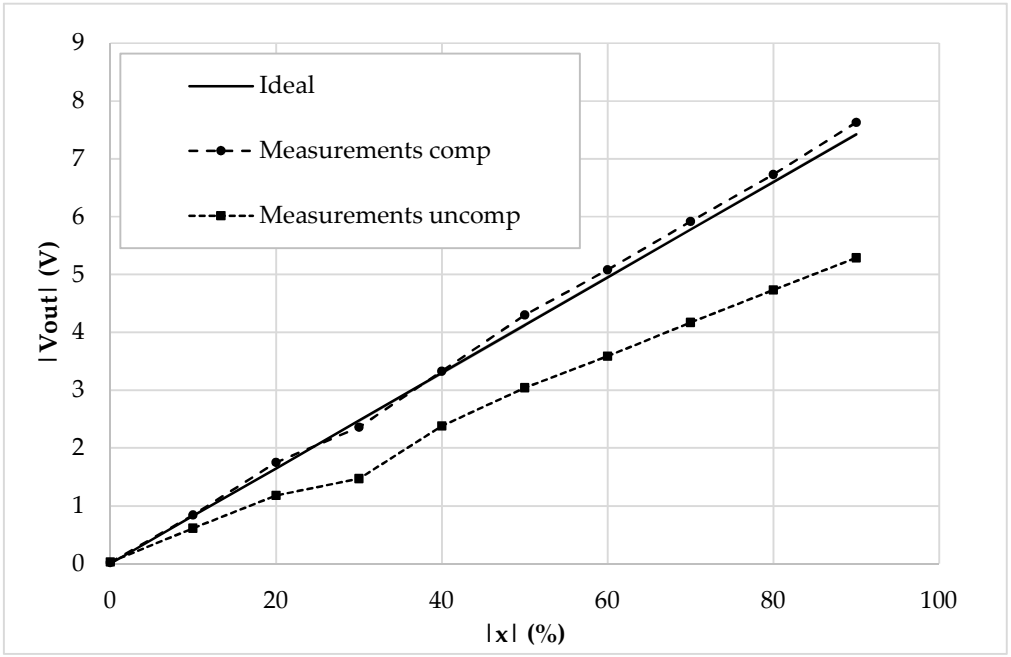


Figure 5.10 DC characteristic (|Vout| vs |x|) of the prototyped interface.

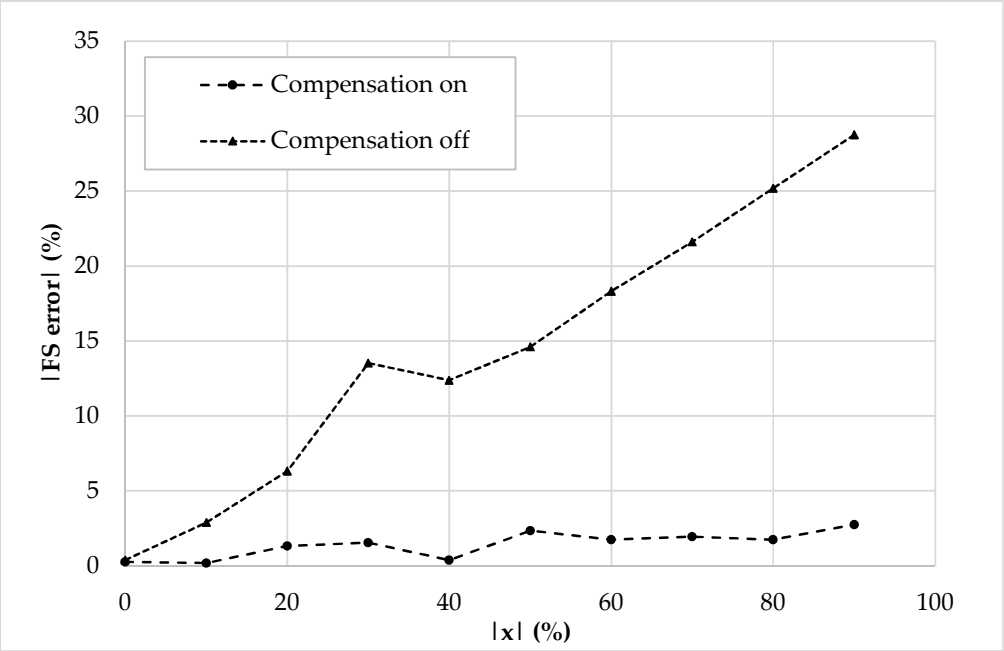


Figure 5.11 Full-scale error (%) of the compensated and uncompensated prototyped interface.

The interface capability of reading very low baseline values has been investigated as well. A set of 1% tolerance capacitors was adopted to mimic a 10 pF baseline sensor. The DC characteristic is shown in Fig. 5.12: as expected, the error increases up to the 3.3% however the interface still shows a good behavior being the maximum linearity error equal to 1.9%FS. The resulted sensitivity is equal to 412 mV/pF. The maximum value of C_0 i.e. C_{0max} is 200 pF and its minimum value C_{0min} is 10 pF. Therefore, the dynamic range is $C_{0max} - C_{0min} = 200\ \text{pF} - 10\ \text{pF} = 190\ \text{pF}$.

Table XIX compares the presented readout technique with data available from the literature: as visible the advantages coming from a mixed current-voltage approach together with the consequent ease in alleviating the effects of parasitic capacitances, allow to maintain a full range readout capability if compared to traditional voltage mode circuits while sensibly reducing the allowable sensors baseline. The sensitivity parameter reported in the table is calculated from the output voltage relationships of the referenced works and referred to the minimum baseline allowed by the interface. Since the circuit in Section 3.2.1 has a non-linear input output relationship the sensitivity cannot be uniquely determined.

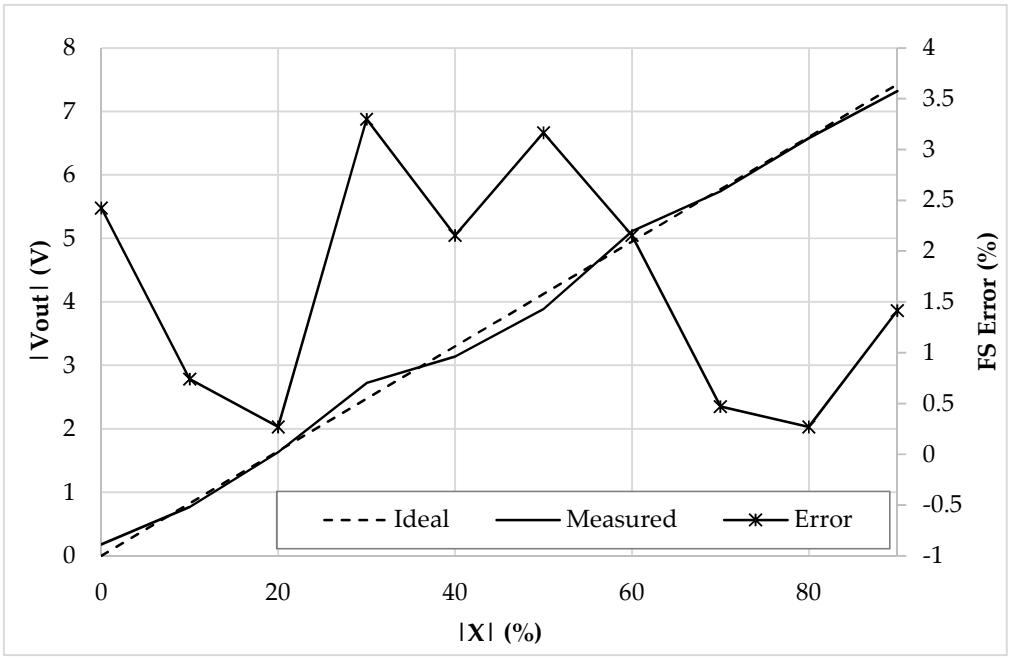


Figure 5.12 DC characteristic (|Vout| vs |x|) and full-scale error (%) of the prototyped interface with a 10 pF sensor baseline.

Table XIX Comparison table.

Ref.	This work	Section 3.3.1	Section 3.2.1	[64]	[56]	[23]	[16]
Approach	Mixed	C to V	C to V	C to Digital	C to I	C to V	C to V
Variation range	±100%	±100%	-30%; +100%	±50%	±100%	±60%	±50%
C_{bl}	10 pF / 200 pF	140pF÷14 nF	400 pF	400 pF	1 pF	20 pF	500 pF
Linearity error FS	<1.9% / <0.9%	0.5÷0.8%	<0.45%	<0.2%	±1.5%	<0.1%	<0.03%
Sensitivity	412 mV/pF / 21 mV/pF	71 mV/pF	Non-linear	4 counts/pF	50 nA/fF	833mV/pf	5mV/pF
Typology	Discrete	Discrete	Discrete	Discrete	Integrated	Discrete	Discrete

5.4 Discussion

A parasitic insensitive read-out circuit for differential-capacitive sensors has been presented in this chapter. The proposed circuit utilizes VCII and produces an output voltage proportional to the sensor variation. The working principle is based on current summing and subtracting technique resulting in a very simple yet effective implementation. To reduce the errors to the minimum value, no switches are employed. The effect of parasitic capacitances is cancelled using a very simple compensation circuit. The proposed method has been theoretically analysed and simulated. The simulation results have shown a negligible full-scale error even for parasitic capacitances comparable to the baseline value. The notable advantage of the proposed circuit is that the sensitivity can be simply adjusted by a resistor. Measurement collected from a discrete prototype have been given, proving a good agreement with theory and simulation results and the capability of the circuit to host low baseline sensors. Several degrees of freedom are also available for the designer to better optimize the performances according to necessity. A comparison with the available literature has been also proposed highlighting the effectiveness of the presented idea and the good potential of the integrated version.

6 SECOND GENERATION CURRENT AND VOLTAGE CONVEYORS

The last chapter of this Ph.D. thesis aims to give to the reader an insight about the contributions that have been proposed about the design of second generation current conveyor (CCII) and second generation voltage conveyor (VCII) architectures.

After a high-level analysis, evidencing the non-idealities of these devices, with respect to their ideal use cases, a number of transistor-level architectures will be shown, featuring their properties and their working principles. Both state of the art and novel proposals will be analysed.

6.1 Second generation current conveyors

6.1.1 Introduction

As the name suggests, the CCII was conceived in 1970 as the successor of the previously proposed first generation current conveyor (CCI) [65] with the aim of improving its flexibility by adding a voltage input terminal [58-59, 66-70]. Indeed, a CCII (Fig. 6.1) can be considered as a three terminals active device having a high-impedance voltage input, Y terminal, a low-impedance current input, X terminal, and

a high impedance current output, Z terminal. Ideally, the relationships that link each terminal can be expressed by the following matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{6.1}$$

From Eq. 6.1 it comes out that a voltage that is applied to the Y terminal is ideally buffered to the X terminal, whereas a current that is generated at the X terminal is 'conveyed' to the output Z port. The direction of the current vector is determined by the CCII itself. As visible from Fig. 6.1a, in a positive current conveyor (CCII+), currents at X and Z share the same direction with respect to the device terminals. On the other hand, as shown in from Fig. 6.1b, in a negative current conveyor (CCII-), the same currents have opposite directions. Moreover, being Y a high (ideally infinite) impedance node, no current flows in it whenever a voltage is applied.

From the matrix reported in Eq. 6.1, it is remarkable the analogy between a CCII and a MOSFET. Indeed, as shown in Fig. 6.2, the buffering action between the Y and X terminal resembles the behaviour of the gate-source voltage, being the gate a high impedance input, and the source a low impedance voltage output (given by the inverse of the transistor transconductance *1/gm*). Similarly, the drain current matches the source current, mimicking the conveying action between the low impedance current input X (the source of the MOSFET) and the high impedance current output Z (the drain of the MOSFET, being equal to the drain-source resistance R_{ds}).

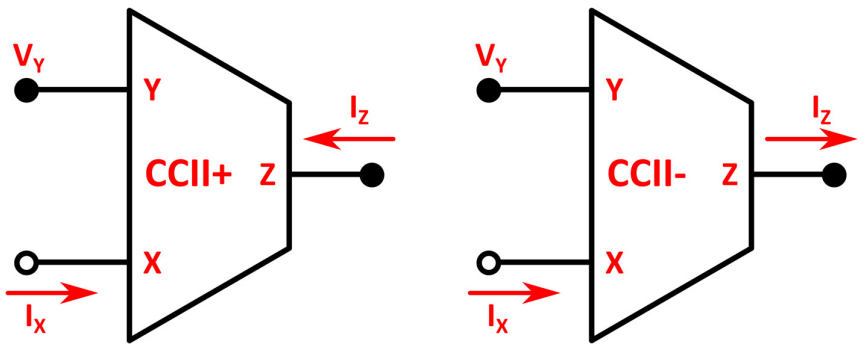


Figure 6.1 High level representation of a a) CCII+; b) CCII-.

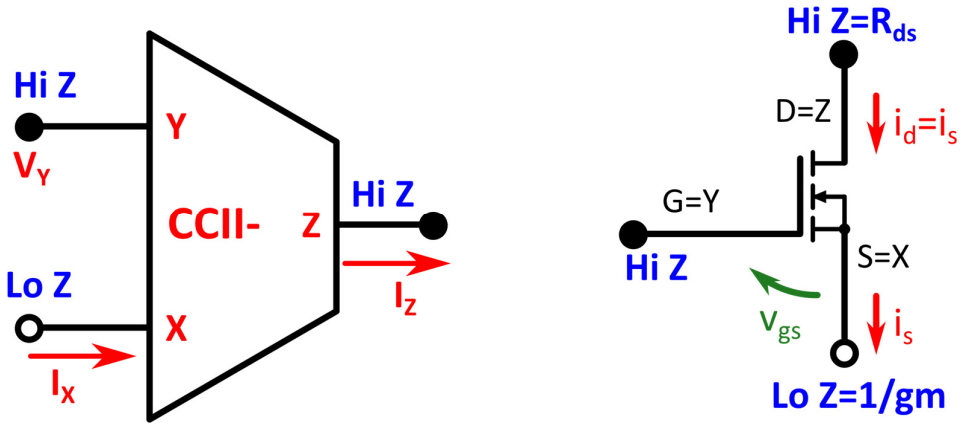


Figure 6.2 Analogy between a CCII and a MOSFET.

Compared to the widespread Op-Amp, a CCII, thanks to its native current and voltage processing capability, allows to achieve a wider bandwidth given a fixed gain level, and allows to reach better common mode rejection ratios in many applications like instrumentation amplifiers [71-74].

6.1.2 CCII non-idealities

The non-idealities of a CCII reside in three main aspects: the non-unitary voltage and current buffering between the terminals, their constant voltage or current offsets and, most importantly, the impedance levels at the same X, Y and Z terminals. Indeed, a more realistic version of Eq. 6.1 is given in Eq. 6.2.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} sC_Y & 0 & 0 \\ \alpha & (R_X + sL_X)//\dfrac{1}{sC_X} & 0 \\ 0 & \pm\beta & \dfrac{1}{R_Z//\dfrac{1}{sC_Z}} \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{6.2}$$

The elements on the main diagonal represent the actual impedance (or admittance) at each port (see Fig. 6.3). As visible, at the Y terminal the impedance is purely capacitive: this is a typical feature of CCII designed using CMOS differential pair inputs. A resistive component may be present in the case of BJT input stage implementations, or even in the case of CMOS stages where the input is different from a gate terminal.

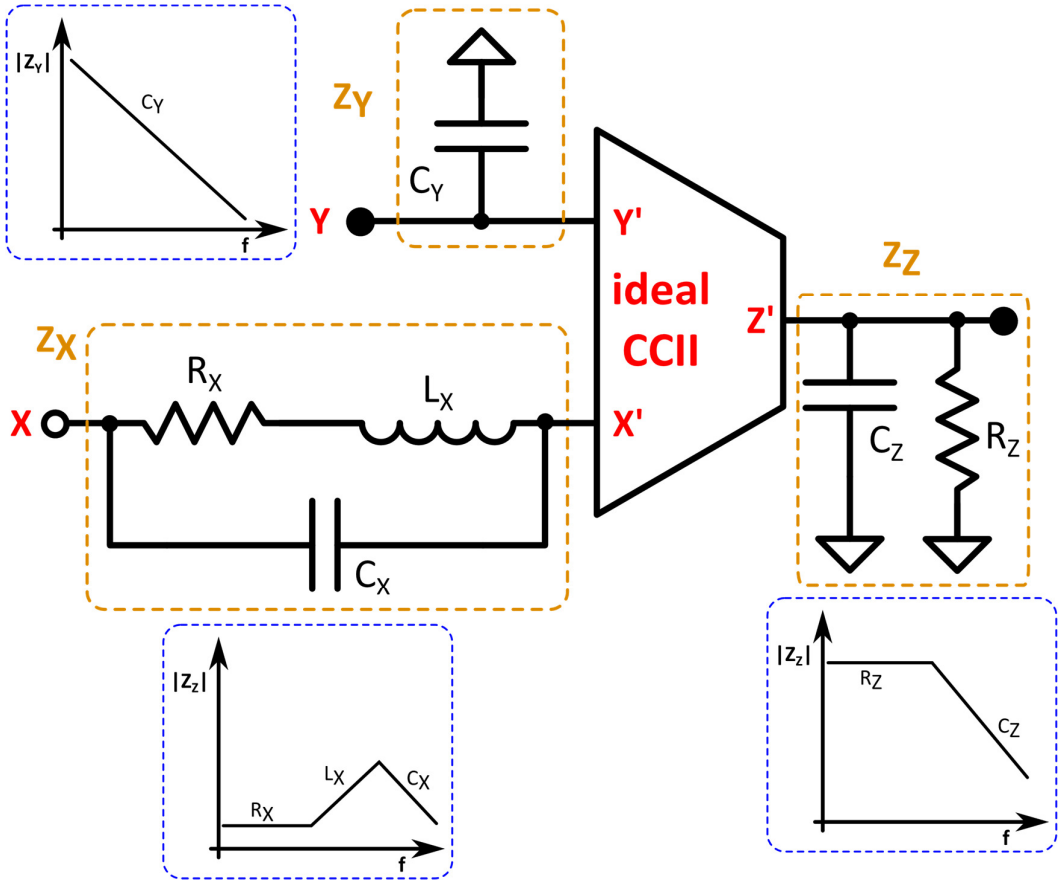


Figure 6.3 CCII impedances at each terminal.

Since ideally the impedance level at Y is infinite, as the operating frequency increases, the CCII loses ideality. At X terminal, the main low-frequency contribution is typically resistive and very low in magnitude. As the frequency increases, the inductive contribution becomes predominant increasing the overall impedance at this terminal. Similarly, at Z output terminal, the low-frequency impedance is purely resistive with a large magnitude. At high frequency however, the capacitive contribution lowers it. The bandwidth of the impedance (identified as the frequency interval where the value of the impedance remains acceptable for a specific application) is an important metric to evaluate the ideality of a CCII.

The α and β parameters represent the voltage and current buffering coefficients, respectively. Their magnitude is ideally equal to unity, although in some modified versions of the CCII [75-76] they are made greater than one for a specific purpose.

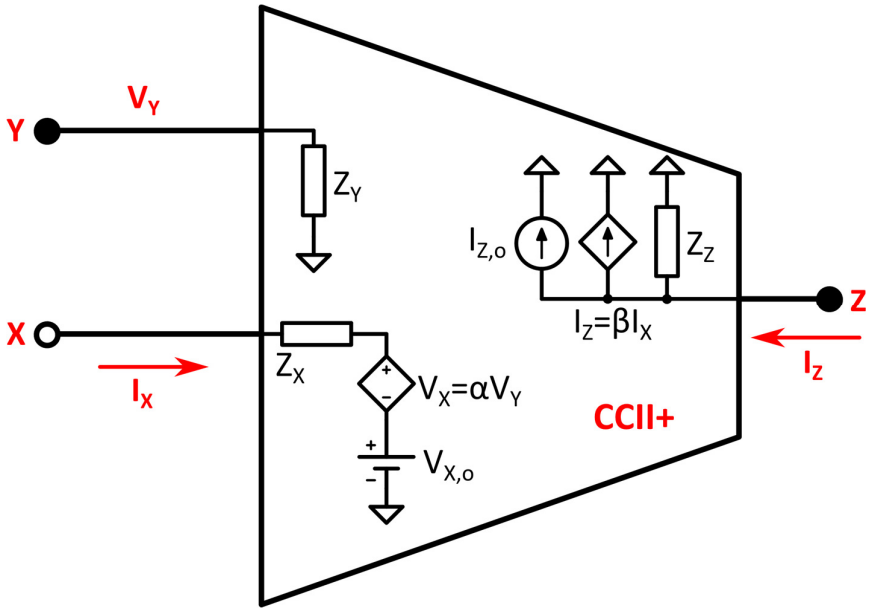


Figure 6.4 Real CCII equivalent circuit.

A real CCII can be represented as in Fig. 6.4. As visible, this model takes into account the impedances at each port, α and β parameters and also voltage and current offsets at X ($V_{X,o}$) and Z ($I_{Z,o}$) terminals.

6.1.3 Differential pair based CCIIs

There are many possibilities when it comes to design transistor level CCII topologies [77-80]. We will analyse solutions based on a classical differential pair because we want to show how, starting from very simple architectures proposed in the literature, we managed to improve them maintaining the same approach thus obtaining more performing and advanced solutions.

A basic topology that implements a current conveyor is shown in Fig. 6.5 (please consider the scheme as purely ideal, in particular concerning the current sources). Transistors M_1 and M_2 implement the differential pair. A simple unitary negative feedback at M_2 creates the low impedance current input X, whereas M_3 and M_4 make sure that the current that is forced into X is mirrored at the high impedance Z terminal.

A simple small signal analysis allows to evaluate both α and β parameters, and impedances. The former parameters can be evaluated as:

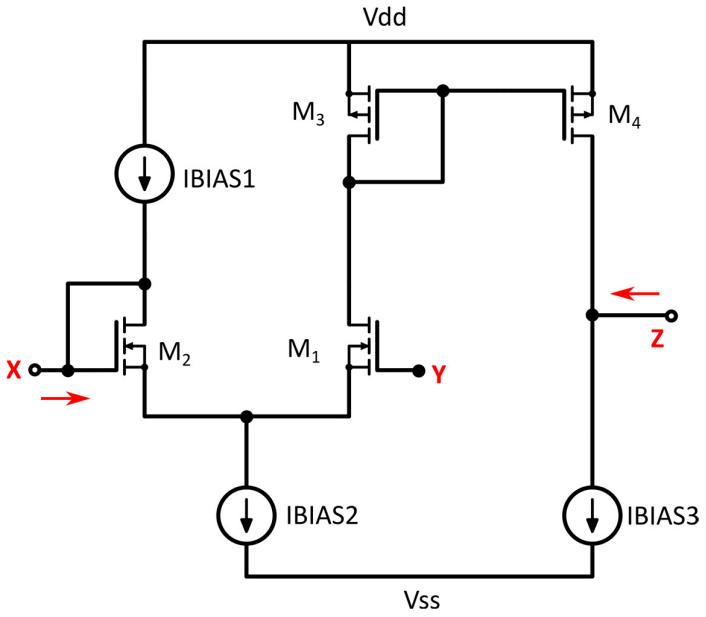


Figure 6.5 Class A CCII based on a differential pair.

$$\alpha = \frac{R_{ds1} gm_1}{1 + R_{ds2} gm_2} \cong \frac{gm_1}{gm_2} \tag{6.3}$$

$$\beta = \frac{R_{ds3} R_{ds4} gm_4}{(1 + R_{ds3} gm_3)(R_{ds4} + R_{LOAD})} \cong \frac{gm_4}{gm_3} \tag{6.4}$$

As visible α depends on the ratio of gm_1 and gm_2. As long as M_1 and M_2 have the same dimensions it results close to unity. Unlike this, β depends on the load impedance, therefore the approximation of Eq. 6.4 stands only if it is negligible compared to R_{ds4}.

Terminal impedances can be evaluated as:

$$Z_X \cong \frac{1}{gm_2} \tag{6.5}$$

$$Z_Y = \frac{1}{(WL)_{M1} C_{ox}} \tag{6.6}$$

$$Z_Z = \frac{R_{ds4} R_{bias3}}{R_{ds4} + R_{bias3}} \tag{6.7}$$

The high input impedance at the Y terminal depends only on the geometry of M_1 (and on the technology used), whereas the low impedance at the X port is given by the inverse of the transconductance of M_2 transistor, being it diode-connected.

An upgraded class AB CCII, based on a differential input pair, is shown in Fig 6.6. As visible, the CCII is composed by three stages, a simple operational transconductance amplifier (OTA) as input stage (M_1-M_4), and two CMOS inverters working in parallel.

M_5 and M_6 provide the necessary phase shift that performs the negative feedback generating the low impedance X terminal, M_7 and M_8, if made equal to M_5 and M_6 respectively, make sure that the current flowing through the X terminal is suitably conveyed to the Z terminal.

Since transistors M_1-M_6 form a dual stage Miller OTA, stability has to be studied in order to safely close the loop. The open loop gain of the Miller OTA can be calculated as:

$$\boldsymbol{A_V = gm_1(R_{ds1}//R_{ds3})(gm_6 + gm_5)(R_{ds6}//R_{ds5})} \qquad \textbf{(6.8)}$$

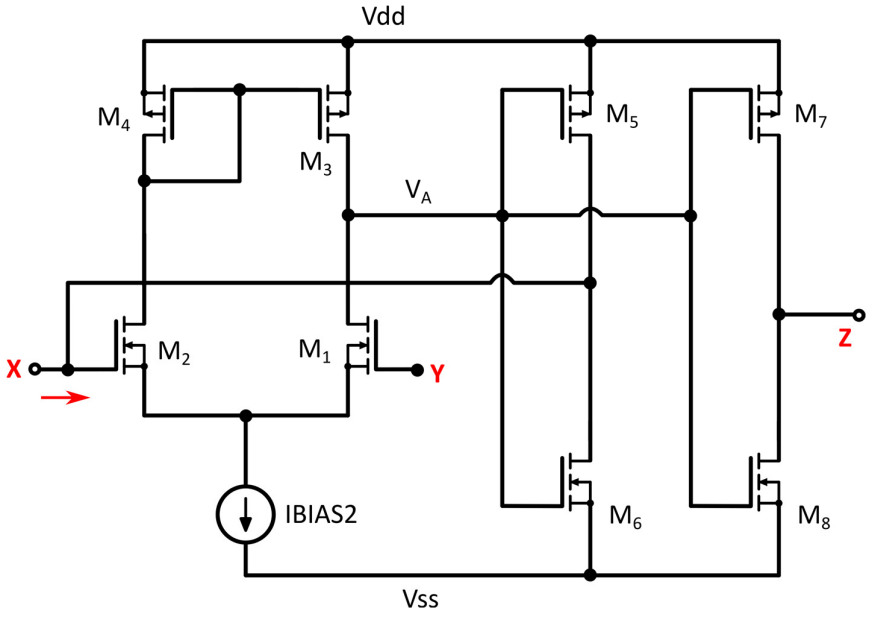


Figure 6.6 Class AB CCII based on a differential pair.

It is very important since the higher it is, the lower is the input impedance at the X terminal:

$$\boldsymbol{R_X = \frac{R_{ds6}//R_{ds5}}{1+A} = \frac{R_{ds7}//R_{ds8}}{1+A} = \frac{R_Z}{1+A}} \qquad (6.9)$$

having designed $M_5 = M_7$ and $M_6 = M_8$. The Y terminal impedance is the same as Eq. 6.6.

6.1.4 Rail to Rail Differential Pair based CCII

6.1.4.1 Design

Based on the same differential pair concept, Fig. 6.7 shows how we designed a rail-to-rail CCII topology.

In order to achieve the full swing at the input, n-MOS (M_1, M_2) and p-MOS (M_3, M_4) differential pairs are placed in parallel, so to proportionally activate one or the other, according to the input amplitude and common mode.

To make sure that the CCII performs equally regardless of the previously mentioned parameters, the circuit is also capable of maintaining a constant total gain gm_T. To do that, input transistors can be biased in weak inversion region, so that the total transconductance results proportional to the current:

$$\boldsymbol{gm_T = \frac{I_P}{2n_p V_T} + \frac{I_N}{2n_n V_T}} \qquad (6.10)$$

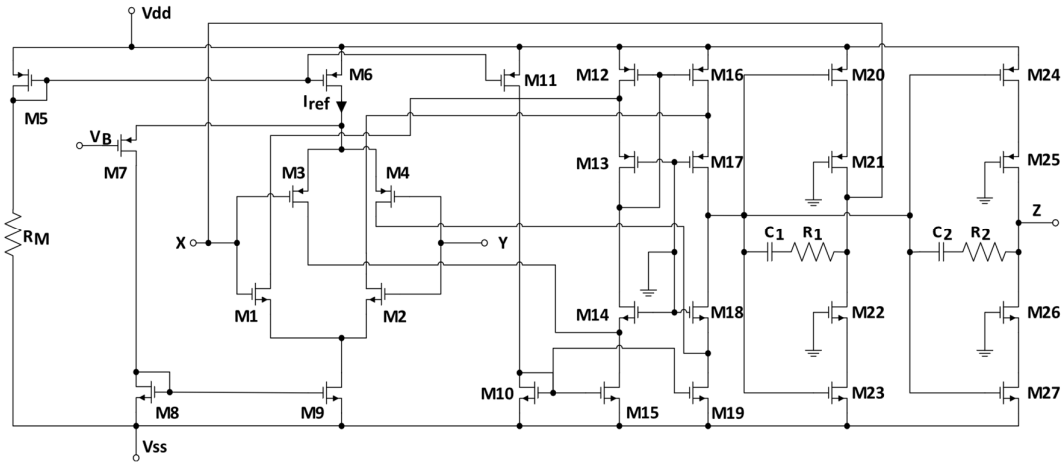


Figure 6.7 RtR constant gm CCII based on a differential pair [81].

*The work presented in this section was published by the authors in [81].

where I_P is the biasing current flowing in the input p-channel pair and I_N the same for the input n-channel pair and n an index ranging from 1 to 2.

The constant-gm condition is established through the switch M_7 and the current mirror M_8, M_9. When a low common mode input is applied, the reference current (I_{ref}), set through R_M, M_5, M_6, flows only into the input p-type differential pair, being M_7 off. If, on the other hand, the common mode voltage increases to a value of about V_B (see Fig. 6.7), the current switch M_7 allows I_{ref} to flow through M_8 and M_9 transistors and into the n-type input differential pair. The sum of currents flowing in both complementary pairs is always kept equal to I_{ref}, so it remains the same at any common mode level. The value of V_B is crucial to set the range when one differential pair is on and the other is off.

In this topology it is also shown how it is possible to use a different OTA topology (folded cascode) than a Miller one.

The second stage (M_{20}-M_{23}) and the matched third stage (M_{24}-M_{27}) are developed as cascoded class-AB inverters to increase Z impedance. The impedance at the Y port results as:

$$\boldsymbol{Z_Y = Z_{M2} // Z_{M4}} \tag{6.11}$$

where Z_{M2} and Z_{M4} can be calculated as in Eq. 6.6. By choosing a cascoded inverter as second stage, allows to further reduce the impedance at X, since the gain of the open loop equivalent OTA composed by the folded cascode M_1-M_{19} and the cascoded inverter M_{20}-M_{23} is increased and equal to:

$$\boldsymbol{A_V = A_I A_{II}} \tag{6.12}$$

where A_I corresponds to the folded cascode input stage gain and can be evaluated as:

$$\boldsymbol{A_I = G_{MI}\{[g_{m18} r_{ds18}(r_{ds19} /\!/ r_{ds4})] /\!/ [g_{m17} r_{ds17}(r_{ds16} /\!/ r_{ds2})]\}} \tag{6.13}$$

A_{II} is the gain of the cascode inverter second stage and can be calculated as:

$$A_{II} = G_{MII}[(g_{m21}r_{ds20}r_{ds21}) /\!/ (g_{m22}r_{ds23}r_{ds22})] \quad (6.14)$$

In Eq. 6.13 and Eq. 6.14 the terms G_{MI} and G_{M2} can be evaluated as:

$$G_{MI} = g_{mT} = g_{mP} + g_{mN}; G_{MII} = g_{m20} + g_{m23} \quad (6.15)$$

The output impedance at the Z node corresponds to the impedance of a folded cascode and can be evaluated as:

$$A_{II} = (g_{m25}r_{ds24}r_{ds25}) /\!/ (g_{m26}r_{ds27}r_{ds26}) \quad (6.16)$$

6.1.4.2 Application

The basic block shown in the previous subsection, has been employed in the implementation of a current mode instrumentation amplifier (IA). The block scheme of such a device is shown in Fig. 6.8 [82-88]. It is based on two CCIIs as active building blocks which transfer Y terminal voltage to X one and converts it to a current using a resistor. The current produced at X terminal is copied to output (Z terminal). The ideal input-output relationship is given in Eq. 6.17.

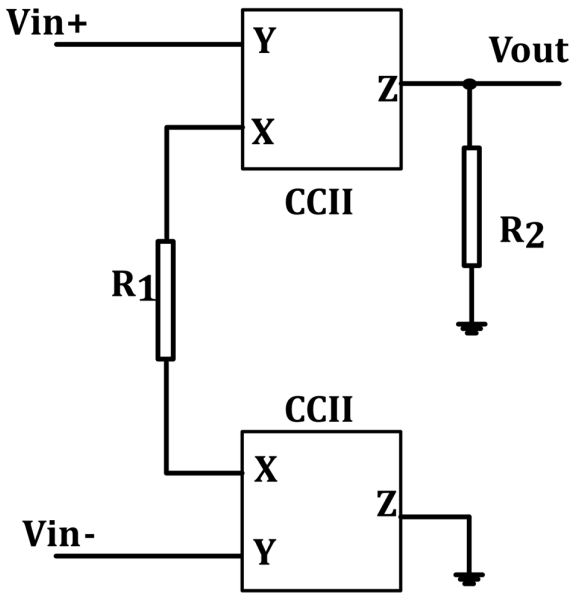


Figure 6.8 Block scheme of the utilized CCII based IA.

$$\mathbf{V_{out}} = (\boldsymbol{V_{in+}} - \boldsymbol{V_{in-}}) * \frac{\boldsymbol{R_2}}{\boldsymbol{R_1}} \qquad \textbf{(6.17)}$$

The complete circuit was designed in a standard CMOS technology (0.35 µm by AMS) designing two identical CCII. Transistor dimensions of the single CCII are shown in Table XX. For the single CCII, at a 1.5V supply voltage, DC power dissipation is 88.5 µW. Always concerning the standalone CCII, Fig. 6.9 shows the transconductance of both the n- and p-channel CCII differential pairs, as well as the total transconductance g_{mT}, given by the sum of the two g_m's, that can be considered constant with the common-mode input voltage. Finally, the standalone CCII open loop gain and phase response are depicted in Fig. 6.10. In agreement with the theoretical calculations, a 115dB DC gain and a 10 MHz GBW are obtained. The rail-to-rail voltage swing at terminal X (versus Y) of the single CCII is illustrated in Fig. 6.11 while Figs. 6.12 and 6.13 depict CCII parameters α and β vs. frequency. Bandwidth is about 10MHz in both the cases.

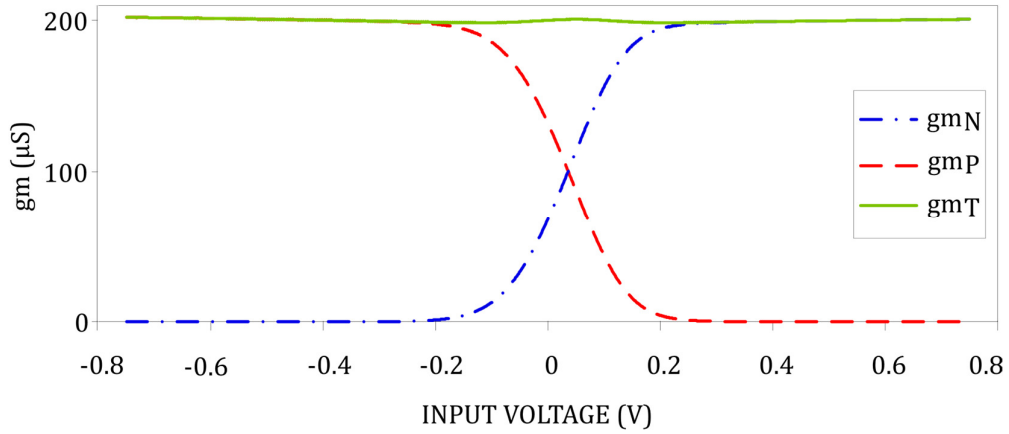


Figure 6.9 CCII open loop gm behavior vs. input common mode voltage.

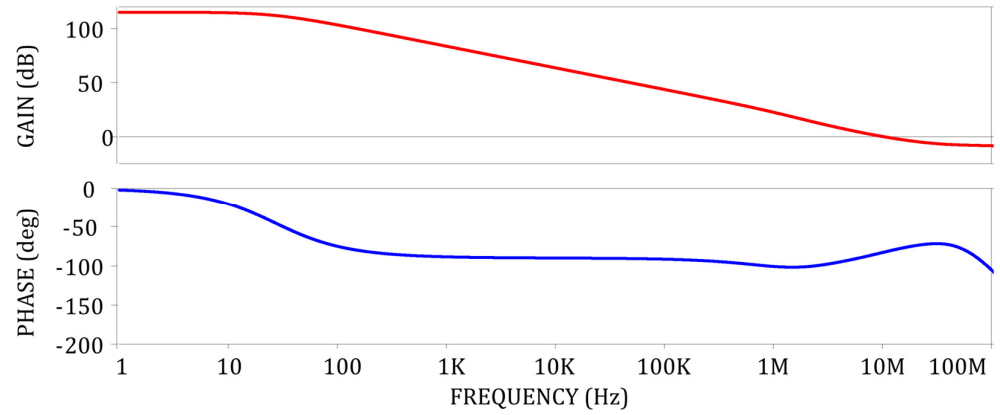


Figure 6.10 CCII open loop gain and phase response.

Taking into account the IA block scheme of Fig. 6.8, simulation results have shown a rail-to-rail characteristic (see Fig. 6.14) with an IA low-frequency CMRR of about 105dB (see Fig. 6.15). As it can be noticed from Fig. 6.16, the AC performances of the instrumentation amplifier for three different gain levels (1,5,10) well match the theoretical behaviour described by Eq. 6.17. Figs. 6.18 and 6.19 show the behaviour of the CMRR with respect to PVT variations and transistor mismatches respectively. As visible, it varies from 94dB to 115dB across all the PVT combinations, while remains almost constant for a ±5% input transistor mismatch. Table XXI summarizes the main features of the proposed IA compared with those of other recent solutions taken from the literature. It is seen that the proposed circuit provides very good performances.

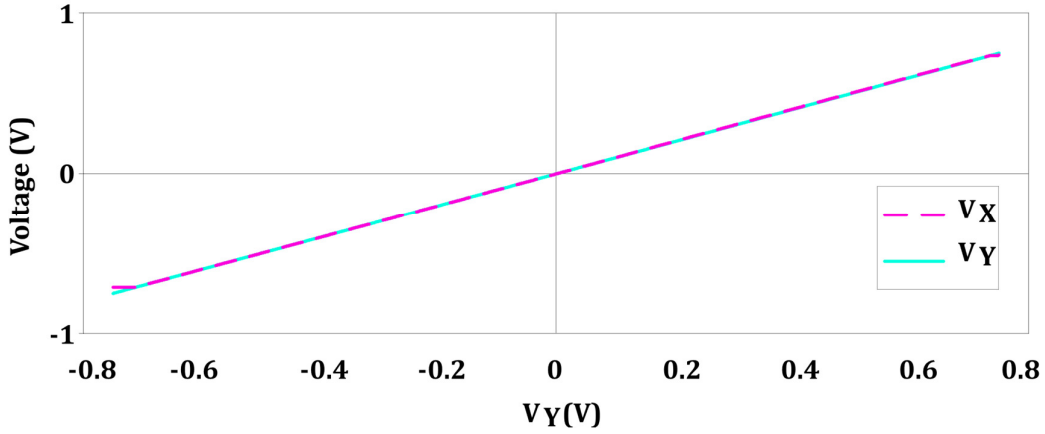


Figure 6.11 CCII DC input voltage characteristics.

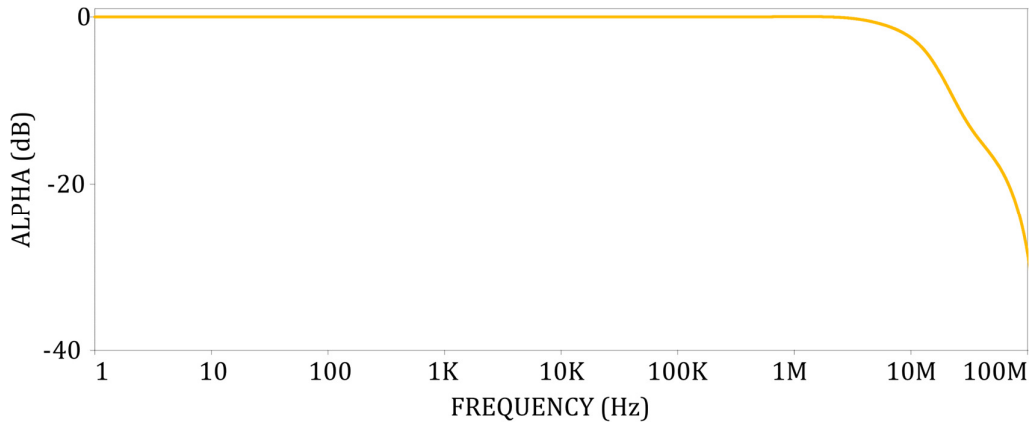


Figure 6.12 Parameter α vs. frequency.

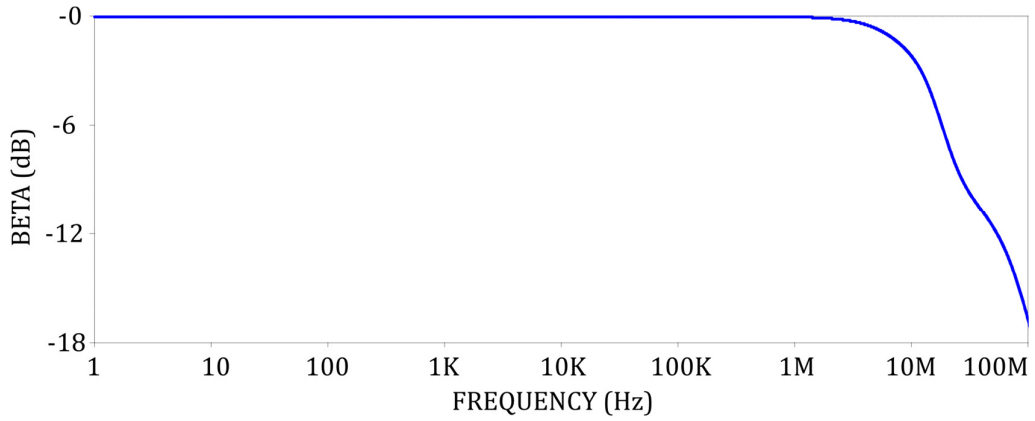


Figure 6.13 Parameter β vs. frequency.

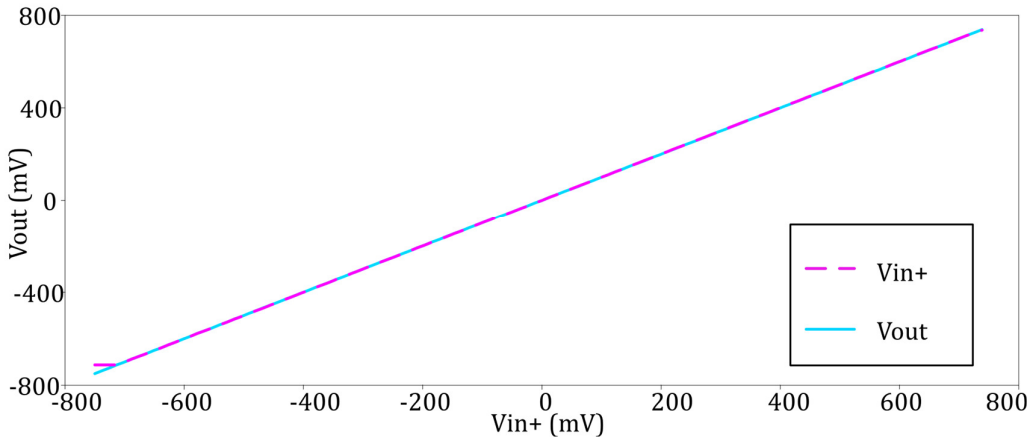


Figure 6.14 IA DC input voltage characteristics.

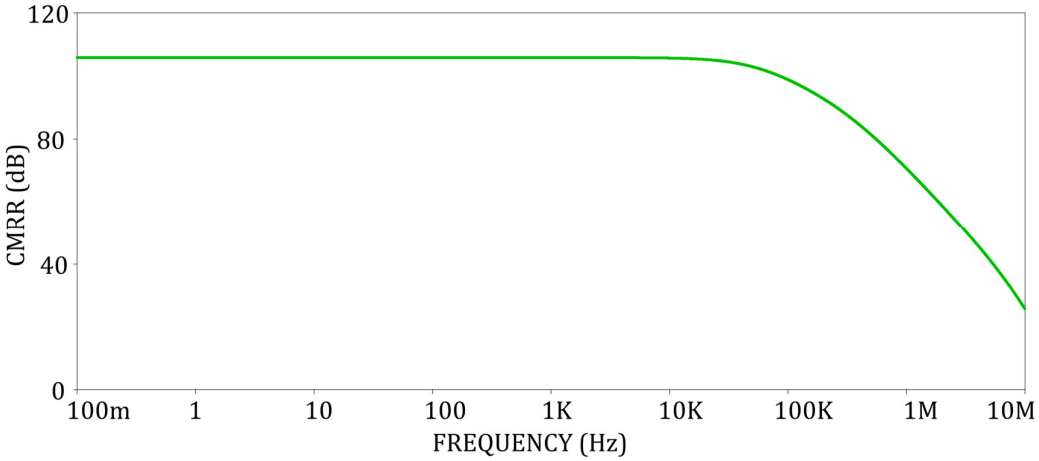


Figure 6.15 IA Common Mode Rejection Ratio.

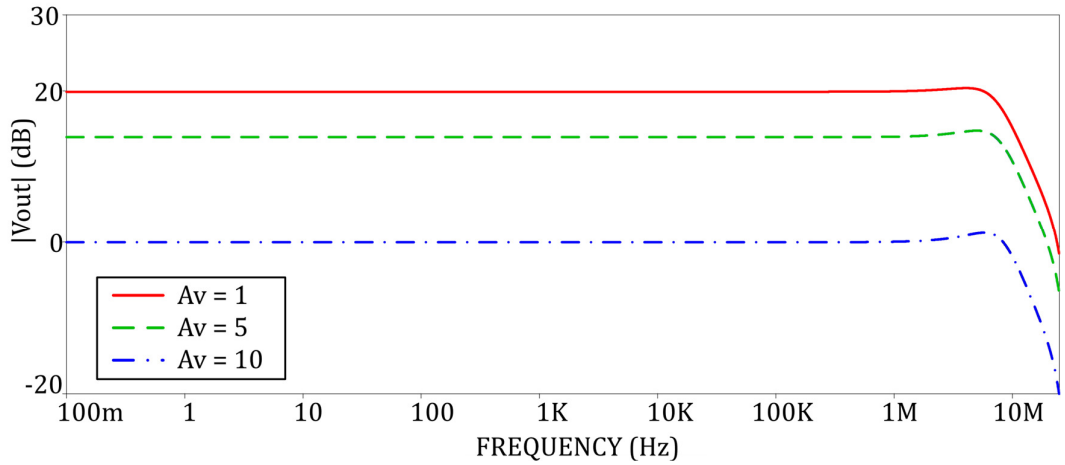


Figure 6.16 IA AC performances at different gain levels.

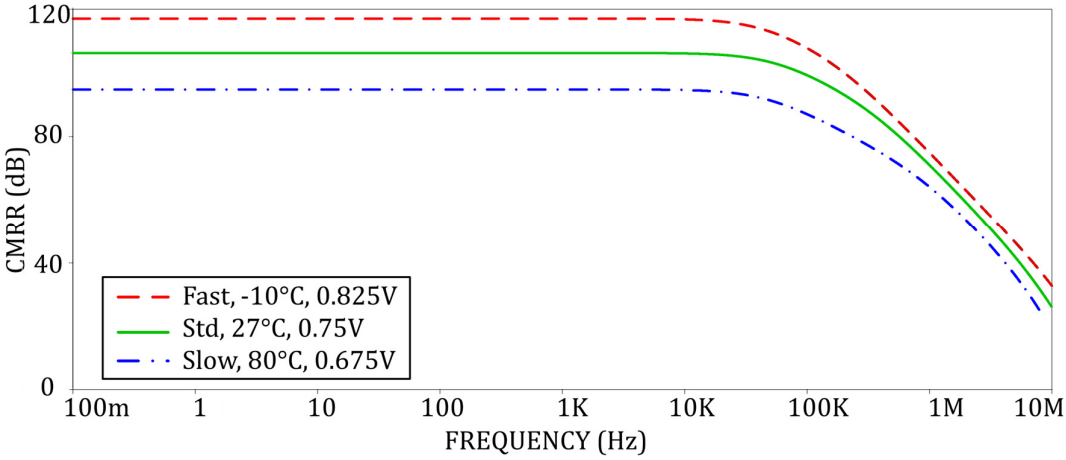


Figure 6.17 CMRR corner analysis.

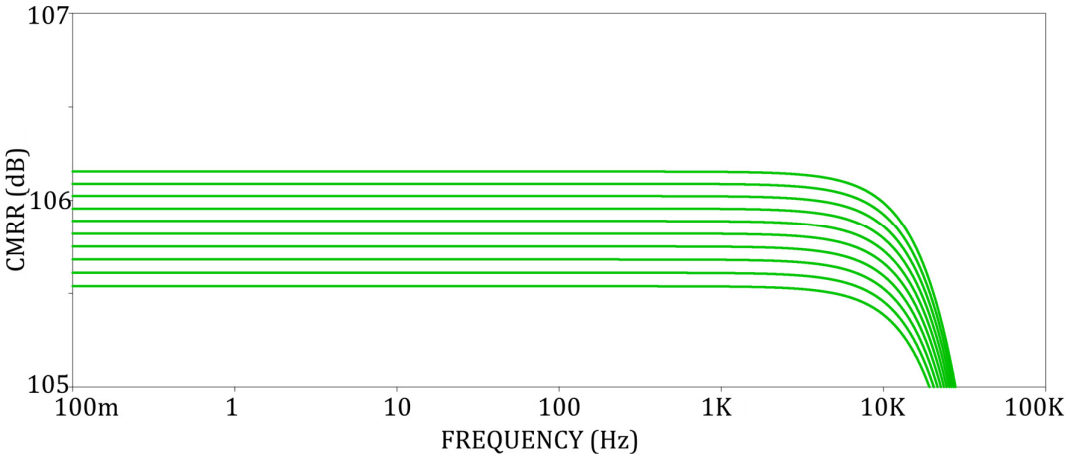


Figure 6.18 CMRR variations for a ±10% input transistors mismatch.

Table XX Transistor values of the implemented IA (both CCIIs are equal).

Transistor	W (µm)	L (µm)	Transistor	W (µm)	L (µm)
M1-M4	200	0.35	M12, M16	19	1.3
M5	5	1	M13, M17	25.2	2.1
M6	38	2	M14, M18	2	2
M7	25	2	M15, M19	17.9	1
M8	30	2	M20, M24	23.1	0.35
M9	33	2	M21, M25	13.3	0.35
M10	40	1	M22, M26	2	1
M11	30	1	M23, M27	5	1

Table XXI IA main performance and comparison.

Parameters	This	[82]	[83]	[85]	[87]	[89]	[90]
V_{DD}-V_{SS}(V)	1.5	1.8	2.2	3	NA	NA	NA
Power (µW)	177	NA	166	110	NA	NA	NA
CMRR (dB)	105	143	120	140	70	100	80
Max gain (dB)	44	40	41	66	NA	40	30
BW (MHz)	8	2	NA	0.2	NA	2	4
Output swing	Rail-to-rail	Non RtR	Non RtR	Rail-to-rail	Non RtR	Non RtR	Non RtR
Active/passive blocks	2+2	4+2	4+2	3+3	3+2	2+3	3+2
Approach	CCII	OP-Amp	Op-Amp	Op-Amp	Op-Amp	CCII	Op-Amp
Technology	0.35µm	0.18µm	0.35µm	0.5 µm	NA	NA	NA

6.1.4.3 Discussion

In this paragraph we have proposed an enhanced RtR constant gm CCII based on a differential pair input stage and used it to implement a current mode Instrumentation Amplifier (IA). Simulation results have shown the validity of the proposed architecture for integrated circuits for low-voltage portable applications.

6.1.5 Adaptively-biased differential pair based CCII

In this section, we will show how we have applied the adaptive biasing feature [92-95], for the first time, to a differential pair-based CCII allowing to decrease its steady state power consumption, minimally affecting its performance. The dynamic biasing (DB) solution here conceived is able to sense the input signal providing an extra current to the CCII only when an input voltage variation occurs.

6.1.5.1 Design

The proposed DB circuitry is reported in Fig. 6.19. It is formed by a *Dummy* circuit (replica of the CCII input stage) and a more specific DB section that we will call *ADABIA*. The *Dummy* is a differential amplifier (*Q1-Q10*) based on a pMOS differential pair (*Q1-Q2*) in a symmetrical OTA and a mirroring stage (*Q11-Q14),* the reference current given by *R1*=100kΩ, which drives the *ADABIA* circuit regulating the output current as a function of the differential voltage applied to its input terminals. It controls the current flowing in the *ADABIA* (*Q15-Q24*) architecture providing the extra current (*Ibias*) and the biasing voltage (*Vbias*) to the main CCII block by a simple current mirror (*Q23-Q24)*. The DB circuit has been suitably dimensioned to furnish a biasing extra current of 5 μA when a differential input voltage is applied. Moreover the provided biasing voltage allows the shutting down of the CCII feedback and output stages. In Fig. 6.20 the typical characteristics of the output current and voltage of the DB architecture as a function of the input differential voltage are reported. The circuit is supplied with ±0.75 V and is conceived to provide a current of 5 μA when a differential voltage greater of 0.2 V is applied even if for negative input differential voltages the current *Ibias* has a small variation (100 nA) that does not affect the operation of the circuit. From simulation results, it comes that voltage *Vbias* has two possible values in the DB operation: 0.4 V and 0 V. In particular, when the voltage is equal to 0.4 V, CCII transistors M9 and M13 are switched off whilst when the voltage is 0 V, they are on.

*The work presented in this section was published by the authors in [91].

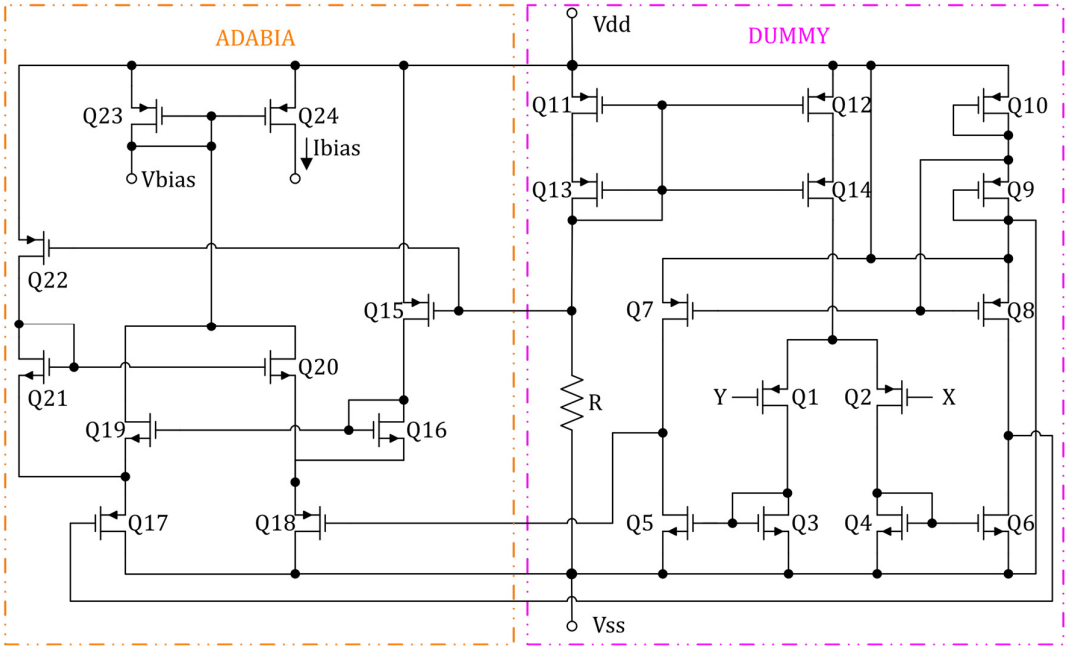


Figure 6.19 The proposed dynamic biasing topology [91].

In Table XXII the sizes of the transistors used in the design of the DB scheme are also reported. The current *Ibias* reaches the maximum value (5 μA) when a different voltage (greater than ±100 mV) is applied on the gate of transistor *Q1* and *Q2*. The voltage slope in transition region depends on *W/L* ratio of transistor *Q1* and *Q2*. In particular, we have chosen high values for the transistor widths. The difference between static and dynamic current depends on *Q17* and *Q18 W/L* ratios. The higher these values are, the higher the difference between static and dynamic current is.

The actual CCII (shown in Fig. 6.21) has been designed by using a symmetrical p-type OTA topology (*M1-M8*) in the input stage, dynamically biased by *Ibias*, a cascode inverter for the X feedback signal *(M9-M12)* and another cascode inverter for the Z node (*M13-M16*). As X node and Z node are equal, *Ix* and *Iz* currents are equal. As shown in Fig. 6.21, these last two stages are biased through *Vbias* voltage, provided by DB circuit, as previously described. This technique allows to completely shut down biasing and output stages so decreasing the average power consumption. Capacitors *C1* and *C2* (4 pF) have been used in the output section to ensure stability. The CCII supply voltage is set again to ±0.75 V in order to use a single reference voltage level. In Table XXIII the sizing for each transistor in CCII main stage is

reported. The W/L choice for transistor M5 and M6 allows to give a high $B = \frac{W_5/L_5}{W_3/L_3} = \frac{W_6/L_6}{W_4/L_4}$ that ensures a higher slew-rate.

Table XXII Transistors sizes of the dynamic biased circuit

Section	NAME (Type)	W (µm)	L (µm)
DUMMY	Q1 (pMOS)	500	0.35
	Q2 (pMOS)	500	0.35
	Q3 (nMOS)	50	0.35
	Q4 (nMOS)	50	0.35
	Q5 (nMOS)	250	0.35
	Q6 (nMOS)	250	0.35
	Q7 (pMOS)	15	0.35
	Q8 (pMOS)	14.4	0.35
	Q9 (pMOS)	1	0.35
	Q10 (pMOS)	14.5	0.35
	Q11 (pMOS)	5	0.35
	Q12 (pMOS)	5	0.35
	Q13 (pMOS)	5	0.35
	Q14 (pMOS)	4.5	0.35
ADABIA	Q15 (pMOS)	0.35	0.35
	Q16 (nMOS)	5	0.35
	Q17 (pMOS)	500	0.35
	Q18 (pMOS)	500	0.35
	Q19 (nMOS)	14	0.35
	Q20 (nMOS)	14	0.35
	Q21 (nMOS)	5	0.35
	Q22 (pMOS)	0.35	0.35
	Q23 (pMOS)	5	0.35
	Q24 (pMOS)	5.9	0.35

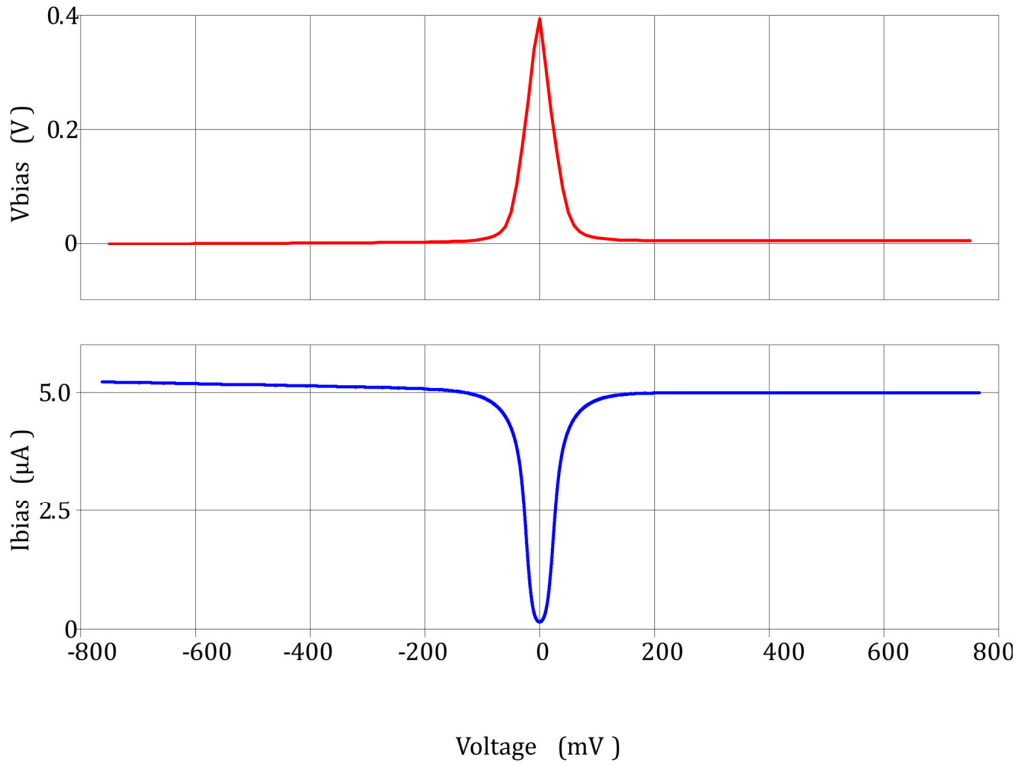


Figure 6.20 Output voltage (above) and output current (below) of the dynamic biased circuit as a function of the input differential voltage [91].

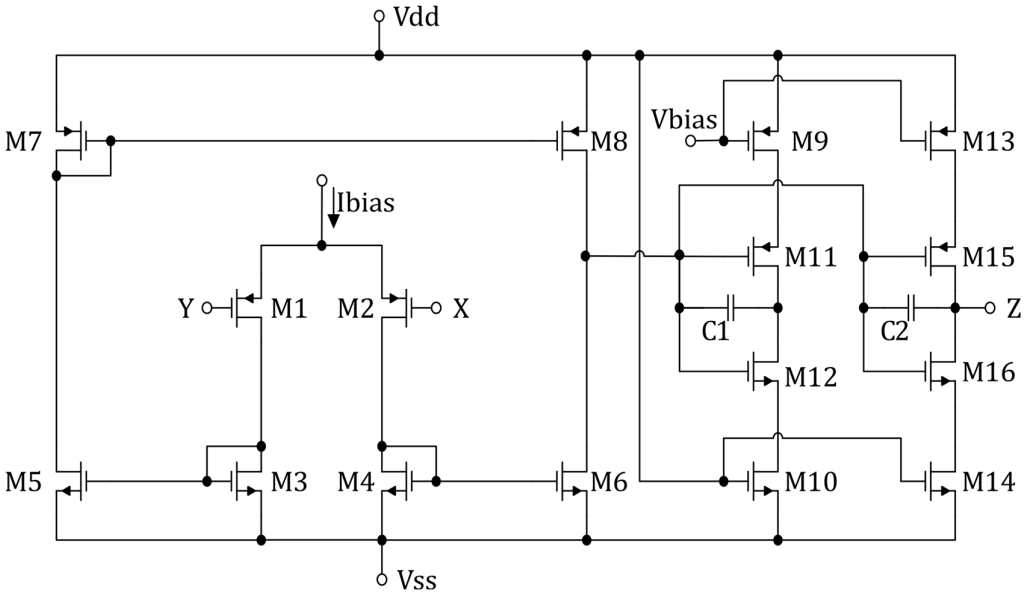


Figure 6.21 The proposed CCII topology [91].

Table XXIII Transistors Sizes of the CCII main circuit

NAME (Type)	W (μm)	L (μm)
M1 (pMOS)	500	0.35
M2 (pMOS)	500	0.35
M3 (nMOS)	50	0.35
M4 (nMOS)	50	0.35
M5 (nMOS)	250	0.35
M6 (nMOS)	250	0.35
M7 (pMOS)	15	0.35
M8 (pMOS)	14.4	0.35
M9 (pMOS)	40	0.35
M10 (nMOS)	40	0.35
M11 (pMOS)	90	0.35
M12 (nMOS)	90	0.35
M13 (pMOS)	40	0.35
M14 (nMOS)	40	0.35
M15 (pMOS)	90	0.35
M16 (nMOS)	90	0.35

6.1.5.2 Application

The above-described circuits (DB and CCII) have been connected as in Fig. 6.22. The purpose is to drive the CCII bias current and voltage as a function of the input signal. The CCII has a static, quiescent bias current of 100 nA that grows up to 5 μA when an input signal variation happens. The complete system has been simulated and tested to evaluate the advantages of the DB architecture applied to a CCII. The simulation setup is defined considering a real resistive/capacitive load of 10 KΩ and

5 pF (named *Zload* in Fig. 6.22) and a square wave input signal having an amplitude of 0.5 V, a period of 20 µs and a settling time of 5 ns.

Furthermore, the characteristics of the proposed DB-CCII are compared with those obtained with a classical CCII design, biased with a constant current of 5 µA, in terms of power consumption, step response and node impedances. In Fig. 6.23 (bottom) a first comparison is shown, evaluating the input signal together with the buffer output voltages provided by the DB-CCII solution and the CCII without the DB circuitry. The results show that the proposed solution has a rise time that is comparable with that provided by the CCII with a static bias current of 5 µA and both of them are able to follow the variation of the input signal with good accuracy. Fig. 6.23 (top) illustrates also the extra-biasing current flowing into the CCII when the same square wave input signal is applied to the Y node of the DB-CCII. This analysis clearly shows the power saving that characterizes the proposed solution. The DB current grows up to 5 µA following the input voltage step and then goes back rapidly to the quiescent value, so minimizing the average power consumption. From a joint evaluation of the characteristics shown in Fig. 6.23, it is evident that the DB-CCII solution is able to provide significant improvements in terms of biasing requirements, moving the classical CCII towards a low-voltage low-power oriented design and without affecting its dynamic performance.

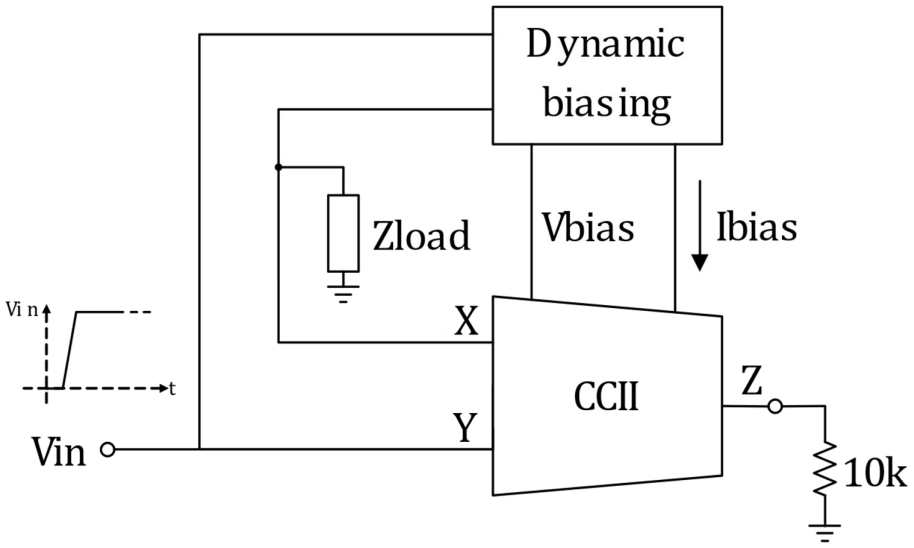


Figure 6.22 The DB-CCII architecture [91].

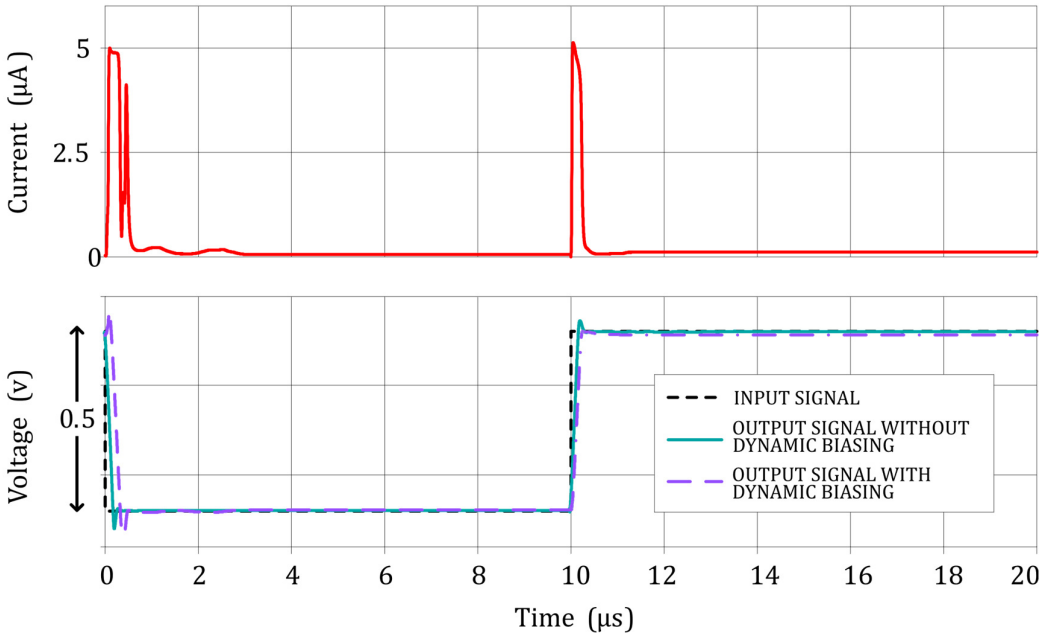


Figure 6.23 Extra-current behavior (top) and comparison (bottom) on the step response between the DB-CCII solution and a classical CCII circuit with a static bias current equal to the maximum value of the extra current managed by the adaptive solution. Input signal has been also depicted [91].

Finally, the node impedances of the DB-CCII solution have been evaluated. It is important to remark that, at this stage, we have not paid particular attention to the impedance absolute values that clearly depend on the CCII design choices, but only on the influence of the DB circuit on the CCII characteristics. In Fig. 6.24 the impedances seen at X, Y and Z nodes are shown when DB circuit is in active mode hence having a maximum bias current. In this scenario, the Y node shows impedances that are fully comparable with typical CCII. The Z node impedance changes from a resistive to an inductive behaviour, as expected, with a high resistance value and a low capacitive value at higher frequencies. Same considerations can be made for the X node where the impedance shows a series resistance and inductance with a parallel capacitance. Clearly, if the DB bias current is turned off, all the impedances have a possible different behavior, especially at X node. However, analyzing impedances in the static condition is meaningless since in this status, the CCII in the DB-CCII architecture is not properly working, so the obtained behavior does not represent the real impedance level seen by the incoming signal when a stimulus is applied. In dynamic conditions, all the impedances of the

DB-CCII tends to converge to those of the classic CCII biased with a constant current of 5 µA. Table XXIV shows the values of the parasitic impedances whilst synthesis of the enhancements obtained with the proposed solution with DB, with respect to that without DB, is summarized in Table XXV, confirming this assumption.

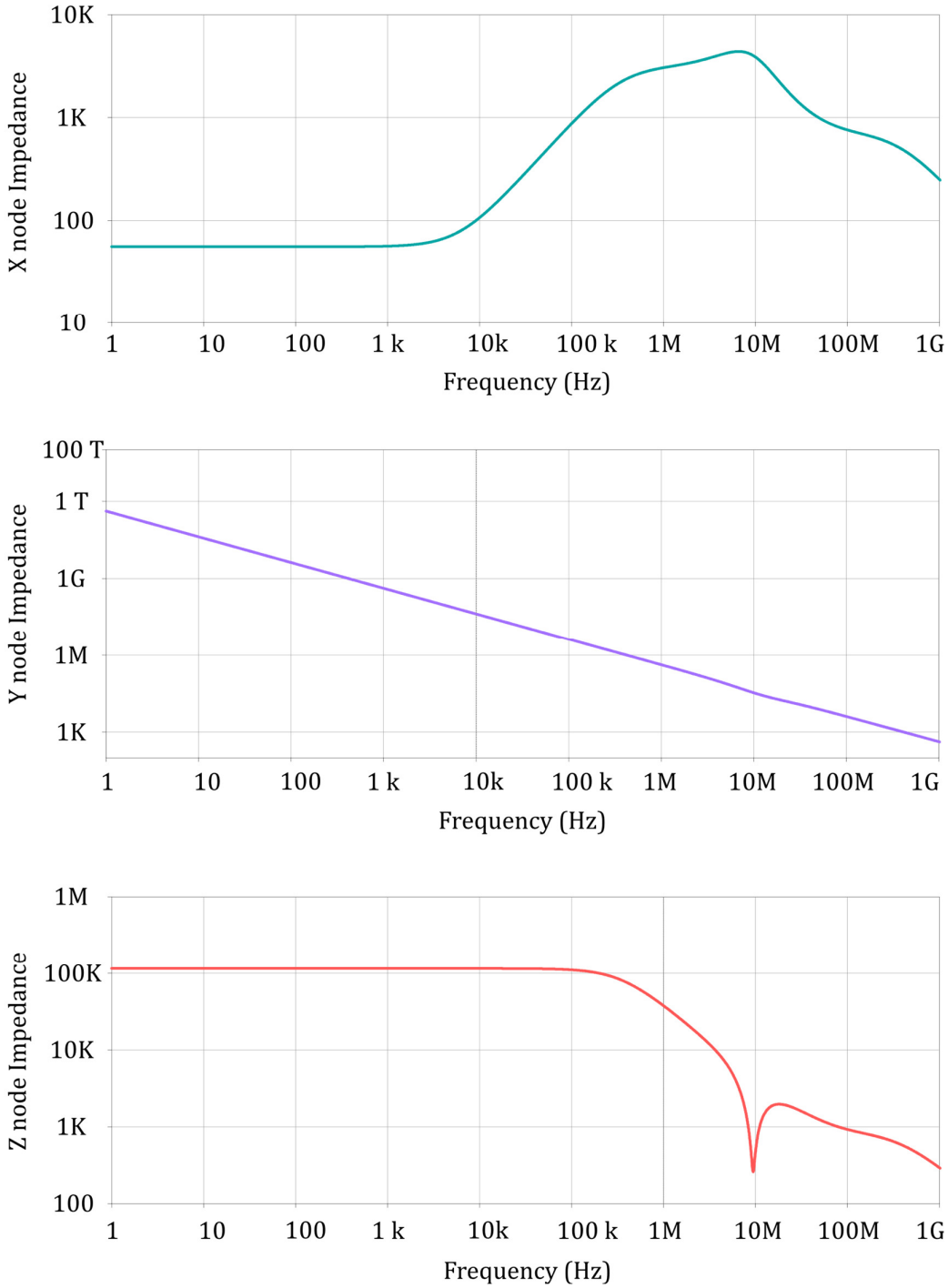


Figure 6.24 Node impedances determined for a 5 µA bias current [91].

Table XXIV Node impedance parasitic values

Resistance at X-node (Rx)	55 Ω
Inductance at X-node (Lx)	0.6 mH
Capacitance at X-node (Cx)	6 pF
Capacitance at Y-node (Cy)	0.4 pF
Resistance at Z-node (Rz)	115 kΩ
Capacitance at Z-node (Cz)	4.3 pF

Table XXV Comparison between the DB-CCII characteristics and those of a CCII without dynamic biasing

Parameters	*CCII*	*DB-CCII*
Power Supply	±0.75 V	±0.75 V
Static bias current	5 µA	100 nA
Dynamic bias current	-	5.1 µA
Static Power Consumption	310 µW	62.3 µW
Dynamic Power Consumption	310 µW	330 µW
Negative slew rate (SR-)	2.89 V/µs	2.58 V/µs
Positive slew rate (SR+)	2.93 V/µs	2.50 V/µs

6.1.5.3 Discussion

We have here presented an innovative dynamic biasing circuit for current conveyor applications. The promising novel architecture allows to implement many low-

voltage low-power applications with a compact and versatile new current mode block that can be designed in a standard CMOS technology. This type of DB-CCII occupies a larger area than the conventional CCII with static biased current but has the advantage of a lower average power dissipation. In fact, when the DB-CCII is not operating, the power dissipation is 5 times lower than that of the traditional current conveyor without the dynamic biased but the performances of the circuit in terms of SR are similar. For this reason, the proposed circuit can be useful in many low-power applications.

6.2 Second generation Voltage conveyor

6.2.1 Introduction

The second generation voltage conveyor (VCII) is born as the dual block of the CCII, from which inherits the "second generation" appellation, even though a first generation voltage conveyor does not really exist. The idea of theorizing such an active device, dates back to two decades ago [60-61], however, only recently, its capabilities are gaining scientific attention and transistor level synthesis are proposed [96-98].

As shown in Fig. 6.25, where a generic voltage conveyor symbol is reported, it is still a three-port block, where terminals are denoted, again, by X, Y, and Z. Unlike CCII, however, Y and Z terminals show a low impedance (ideally zero), being a current input and a voltage output terminal respectively, while X terminal presents a high impedance (ideally infinite) being a voltage input terminal. The ideal outputs of its three ports in terms of their corresponding inputs are shown in the matrix of Eq. 6.18.

$$\begin{bmatrix} \boldsymbol{i_x} \\ \boldsymbol{v_y} \\ \boldsymbol{v_z} \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{\pm 1} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{1} & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{v_x} \\ \boldsymbol{i_y} \\ \boldsymbol{i_z} \end{bmatrix} \tag{6.18}$$

It is seen that a VCII consists of a current buffer between Y and X terminals and a voltage buffer between X and Z ones. By therefore forcing a current to flow into the Y node, it is mirrored to the X node, whereas, by setting a voltage at the X port, it is buffered to the Z port. Ideally, Y terminal can be considered at virtual ground.

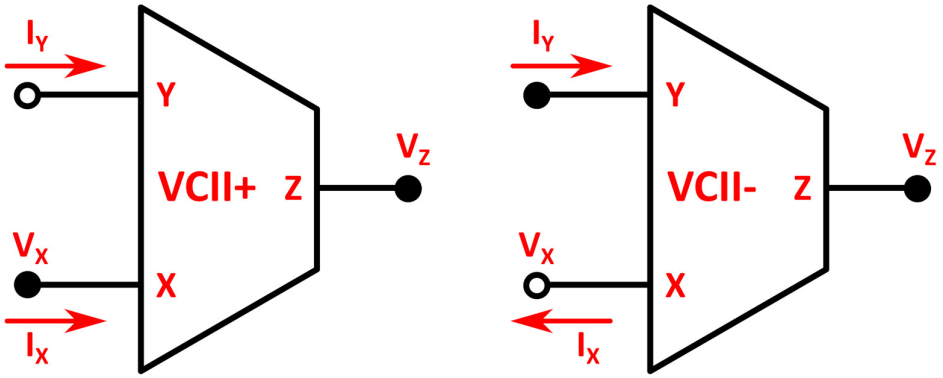


Figure 6.25 High level representation of a a) VCII+; b) VCII-.

Although very simple, VCII has a great potential, since joins both the benefits of Op-Amps and of CCIIs. In fact, it is able to work both in a voltage mode and in a current mode environment, as well as to create a linking point between them.

Op-Amp based circuits are typically limited to produce inverting type outputs. On the contrary, by replacing Op-Amps with VCIIs in these applications, both inverting and non-inverting outputs can be easily produced without modifying the circuital configuration. Also, VCIIs are able to overcome problems such as current crosstalk in non-inverting voltage summing amplifiers which, for an Op-Amp, cannot be avoided given that only high impedance inputs are available. Another crucial feature of the VCII is the wide and gain-independent bandwidth, whereas, for Op-Amp based counterparts, bandwidth reduces proportionally by increasing gain [97].

Since the emergence of current-mode signal processing, where it is possible to achieve fast and reliable signal processing with a very low voltage level (condition that perfectly suits for the new scaled technologies), CCIIs have replaced Op-Amp in many applications. Indeed, as shown in the previous paragraph, they have a very simple internal topology, and operate in open loop conditions. These things make the CCII easier to utilize and able to reach wider bandwidths. In spite of these advantages, the lack of a low impedance voltage output port forces designers to add extra voltage buffers in applications requiring a voltage output. VCIIs deal with this limitation offering a low impedance voltage output.

6.2.2 VCII non-idealities

Eq. 6.19 shows a real-world input-output relationship matrix for a VCII.

$$\begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} = \begin{bmatrix} \frac{1}{r_x} + sCx & \pm\beta & 0 \\ 0 & r_y + sL_y & 0 \\ \alpha & 0 & r_z + sL_z \end{bmatrix} \begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} \tag{6.19}$$

The elements on the main diagonal represent the equivalent impedance or admittance at each terminal (see Fig. 6.26). Indeed, r_y, L_y, r_x, C_x, r_z and L_z are the parasitic resistances associated to Y terminal (ideally = 0), the parasitic inductance at Y terminal (ideally = 0), the parasitic resistance at X terminal (ideally = ∞), the parasitic capacitance at X terminal (ideally = 0), the parasitic resistance at Z terminal (ideally = 0) and the parasitic inductance at Z terminal (ideally = 0), respectively. Coefficients α and β have the same meaning as for a CCII, with the former the ratio between voltages at Z and X, whereas the latter referencing to the ratio between currents at X and Y (sign denotes whether currents are share the same or opposite direction).

Fig. 6.27 depicts a real world equivalent model for a VCII. Similarly to the CCII, other than the effects of impedances and mirroring coefficients, offset voltages and currents have been represented as well.

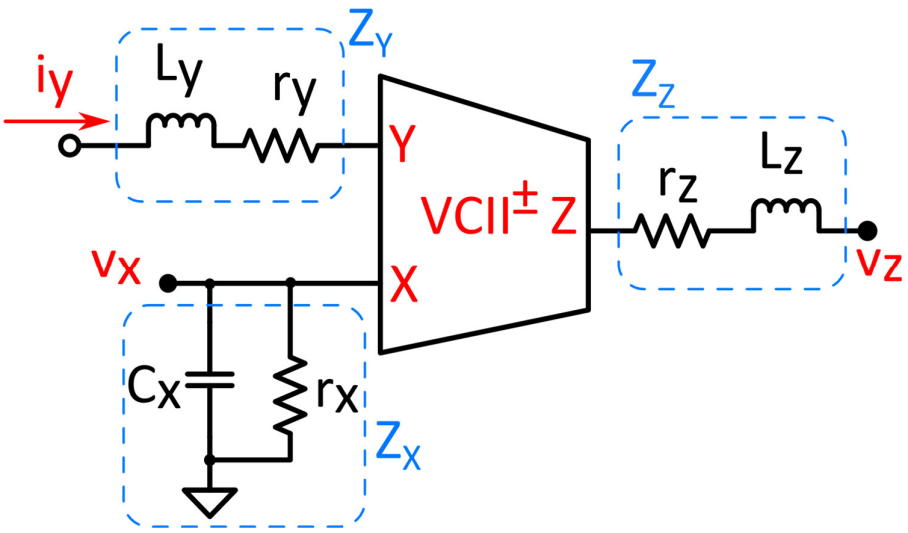


Figure 6.26 VCII impedances at each terminal.

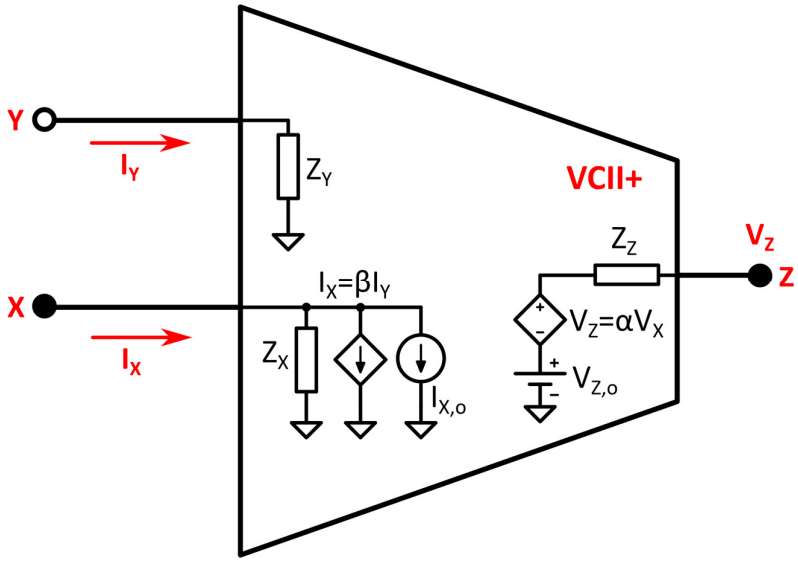


Figure 6.27 Real VCII equivalent circuit.

As previously introduced, since the second generation voltage conveyor has been only recently rediscovered, there is no actual circuital synthesis available in the literature to report here. For this reason, we will show, in the following, our approaches in designing architectures that actually implement such a device.

6.2.3 Super transistor based VCII

6.2.3.1 Design

Like it is underlined in the previous sections, a VCII is made of a current buffer between Y and X terminals and a voltage buffer between X and Z terminals.

Referring to Fig. 6.28, the former is made of transistors M_1-M_7 and the current sources I_{B1}-I_{B4}, whereas the latter is implemented by M_8, M_{A1}-M_{A3} and I_{B5}-I_{B7} current sources. A first negative feedback loop, established by M_1-M_3, forces the offset voltage at Y terminal to be equal to ground, lowering its impedance. The second negative feedback loop, formed by M_4-M_7 transistors, has the dual task to further reduce the impedance at Y terminal while mirroring the input current to the X terminal.

Based on the small signal equivalent circuit (see Fig. 6.29), the impedance at Y and X terminals can be calculated as:

*The work presented in this section was published by the authors in [99].

$$r_Y = \frac{1}{gm_3 gm_1 (ro_1 \| ro_{I_{B1}})\, gm'_4 (ro_{IB_3} \| ro_3)} \tag{6.20}$$

$$r_X = \frac{(ro_7 + ro_6 + gm_6 ro_6 ro_7)(ro_{IB4} + 1/gm_8)}{(ro_7 + ro_6 + gm_6 ro_6 ro_7 + ro_{IB4} + 1/gm_8)} \tag{6.21}$$

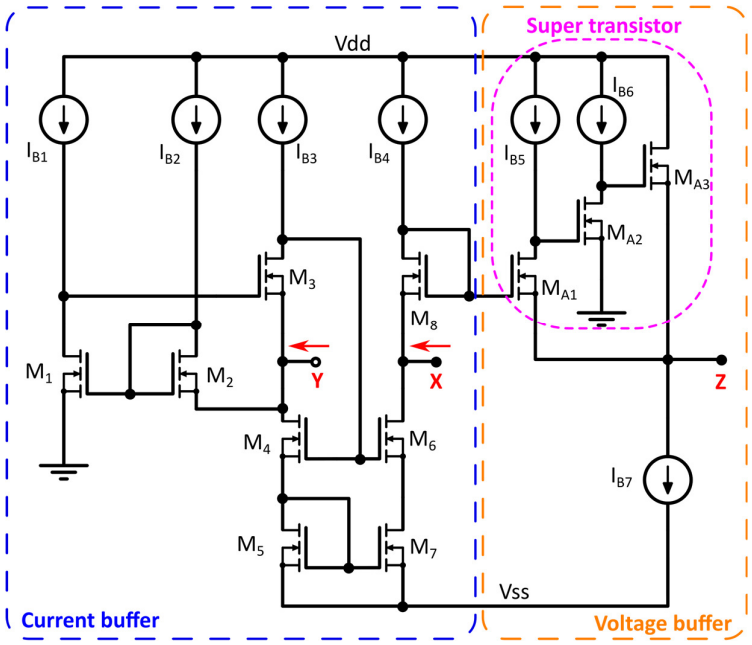


Figure 6.28 Super transistor-based VCII architecture [99].

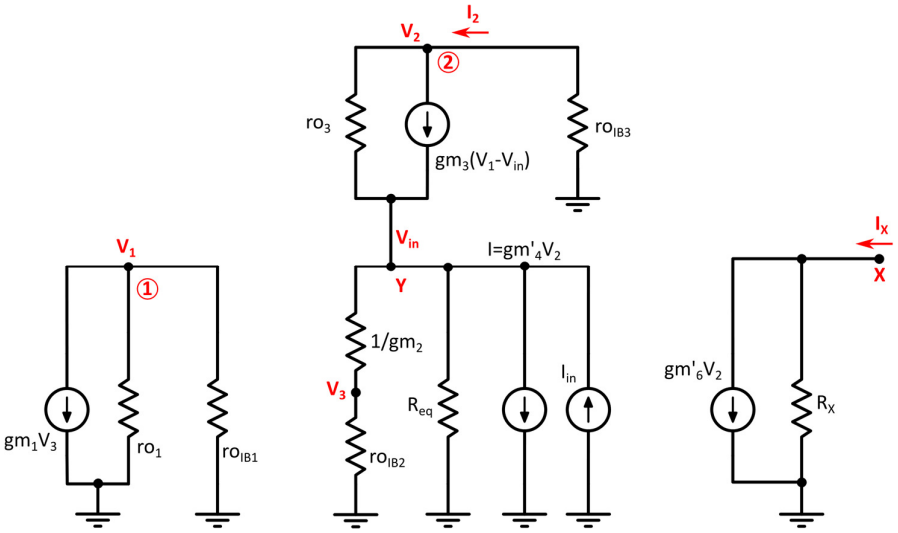


Figure 6.29 Small signal equivalent circuit for X and Y terminals of the proposed VCII [99].

Based on the same model, it is possible to extract the β equation:

$$\boldsymbol{\beta = \frac{i_x}{i_y} = \frac{gm'_6 ro_{IB_3}(R_{eq} \| ro_{IB_2})}{1 + gm'_4 ro_{IB_3}(R_{eq} \| ro_{IB_2})} \approx \frac{gm'_6}{gm'_4} = \frac{gm_7}{gm_5}} \quad (6.22)$$

where:

$$\boldsymbol{gm'_4 = \frac{gm_4 gm_5}{gm_5 + gm_4} \quad , \quad gm'_6 = \frac{gm_4 gm_7}{gm_5 + gm_4}} \quad (6.23)$$

Parameters gm_i, ro_i represent the transconductance and the output impedance of the related transistor respectively and ro_{IBi} is the output impedance of related current source. R_{eq} is the equivalent resistance seen from drain of M_4.

To implement the Z stage of the VCII, the presented topology uses a super transistor (M_{A1}-M_{A3}) [100] which, thanks to its negative feedback, provides a very low impedance at Z terminal also improving the buffering between X and Z terminals. A small signal analysis of this structure [100] allows to derive the voltage transfer between X and Z terminals and the Z terminal impedance, respectively:

$$\boldsymbol{\alpha = \frac{v_z}{v_x} = \frac{ro_{IB4}}{ro_{IB4} + gm_8^{-1}} \frac{1}{1 + [gm_{A1} gm_{A2}(ro_{A1} \| ro_{IB5})(ro_{A2} \| ro_{IB6})]^{-1}}} \quad (6.24)$$

$$\boldsymbol{r_Z = \frac{1}{gm_{A1} gm_{A2} gm_{A3}(ro_{A1} \| ro_{IB5})(ro_{A2} \| ro_{IB6})}} \quad (6.25)$$

6.2.3.2 Simulation results

The VCII of Fig. 6.28 is designed using 0.35μm CMOS technology parameters and supply voltage of ±1.65V. The transistors aspect ratios chosen for simulations are given in Table XXVI. All the current sources are implemented by means of simple current mirrors whose dimensions have been chosen in order to provide the biasing currents shown in Table XXVII. Table XXVIII summarizes the main characteristics of the proposed VCII. As it is seen, it exhibits very low input impedances at Y and Z terminals and high impedance at X terminal. The current and voltage transfer gains are very close to unity (with a load impedance of 1pF//1kΩ). The frequency performance is high while power consumption is only 330μW with a very low nodes voltage offset.

Table XXVI Transistors aspect ratios.

Transistor	*W (μm)*	*L (μm)*	*Type*
$M_{1,2,3}$	35	0.35	nMOS
$M_{4,6}$	2.1	2.1	nMOS
$M_{5,7}$	1.4	1.4	nMOS
$M_{8,A1}$	57.05	1.05	nMOS
M_{A2}	3.5	0.35	nMOS
M_{A3}	16.1	0.35	nMOS

Table XXVII The value of current sources.

Current source	Value (μA)
$I_{B1,B2}$	9.2
I_{B3}	8.5
$I_{B4,5}$	17.7
I_{B6}	8.2
I_{B7}	30

As case study we have utilized the proposed VCII in the applications where VCII is the best candidate, i.e. I to V converter, V to I converter, voltage amplifier, voltage differentiator and voltage integrator. The equivalent circuital implementation of these functions is shown in Fig. 6.30a-e respectively. Fig. 6.31 shows the frequency performance and step response of the VCII-based I-to-V converter which results to be excellent for different values of gain.

Table XXVIII The proposed VCII performance parameters.

Parameter	Value
rx, Cx	1.2MΩ, ~30fF
ry, Ly	6.7Ω, ~1.5μH
rz, Lz	0.7Ω, ~9μH
Offset Voltage	V_{oX}=33 μV, V_{oY}=27μV, V_{oZ}=370μV
α (DC value, -3dB BW)	(0.997, 217MHz)
β (DC value, -3dB BW)	(0.988, 200MHz)
THD Vz (input Vx = 1 V_{p-p} @1MHz, 10 harm)	0.068% (-63dB)
THD Ix (input Iy = 20 μA_{p-p} @1MHz, 10 harm)	0.1% (-59dB)
Static Power Consumption	330μW (101μA)

The VCII-based I-to-V converter also takes advantage of the very low input and output impedances (6.7Ω and 0.7Ω respectively) as shown in Table XXVIII. The Simulations of the VCII as V to I converter in frequency domain and time domain to a step response of 10 mV are shown in Fig. 6.32. This circuit enjoys a high output impedance of 1.2MΩ and very high frequency performance.

Frequency and time domain performances of the VCII based voltage amplifier are shown in Fig. 6.33. In this case, the output impedance is only 0.7Ω and the circuit exhibits approximately constant bandwidth independent of gain. Finally, the simulations of VCII as voltage differentiator and integrator in time domain are shown in Fig. 6.34 and Fig. 6.35 respectively. Both of these circuits exhibit very low output impedance of 0.7Ω.

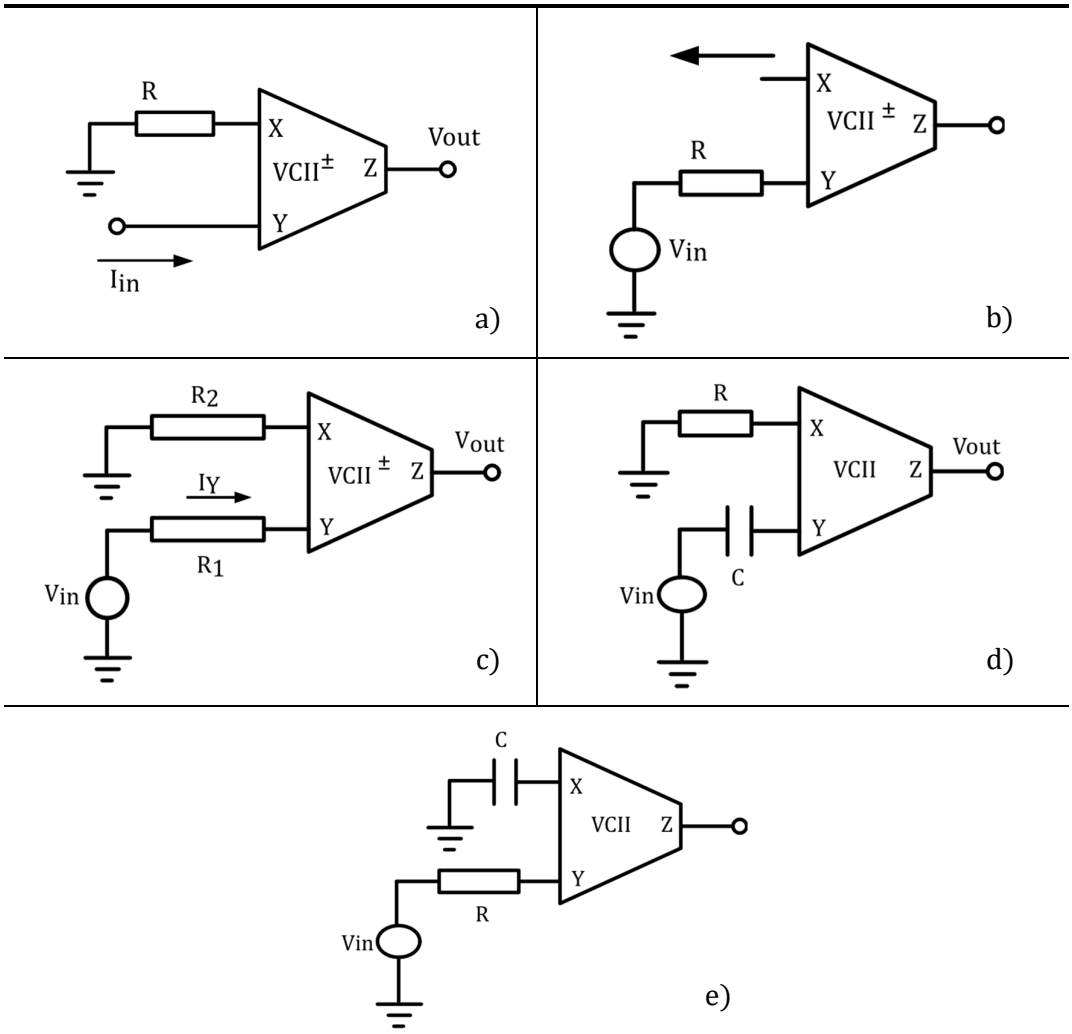
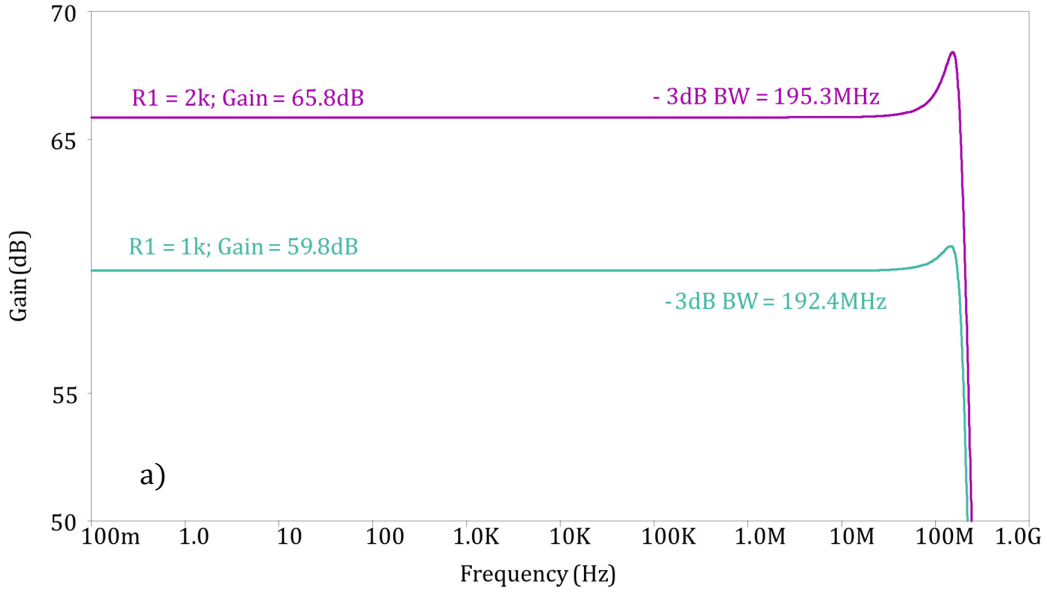


Figure 6.30 VCII based configurations: a) I to V converter, b) V to I converter, c) voltage amplifier, d) voltage differentiator, e) voltage integrator.



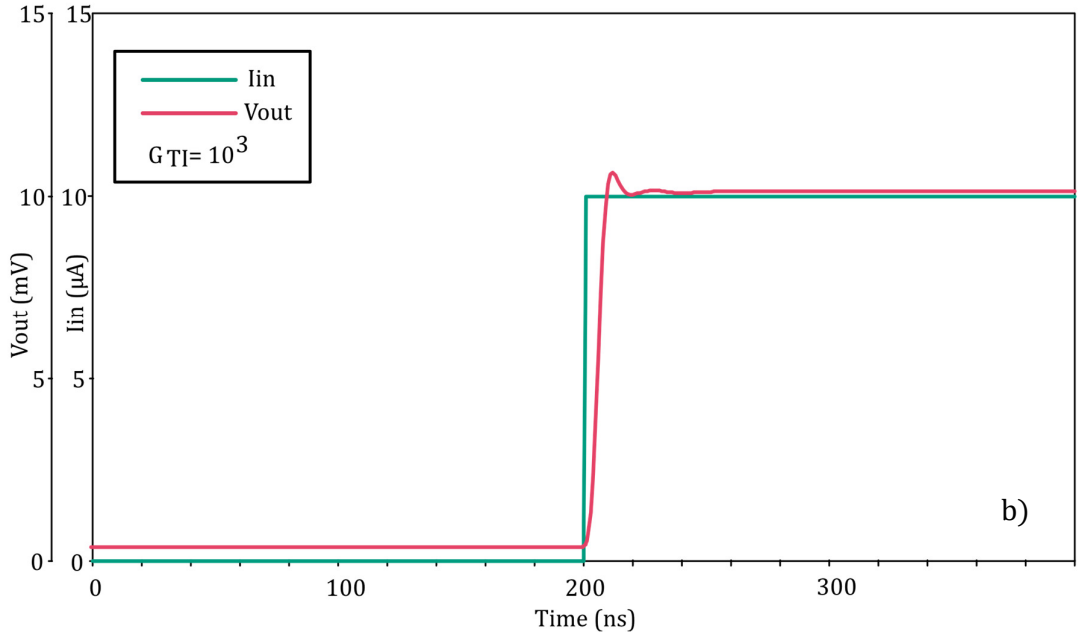
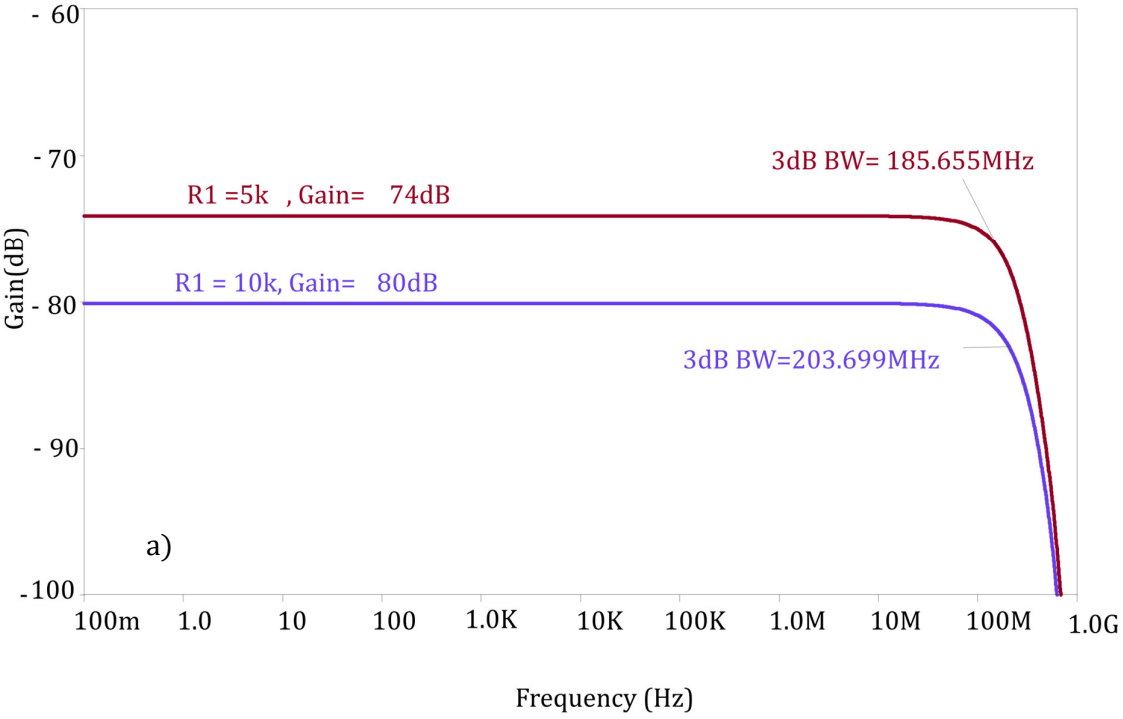


Figure 6.31 VCII based I-to-V converter a) Frequency response and b) step response to a current input with amplitude of 10µA.



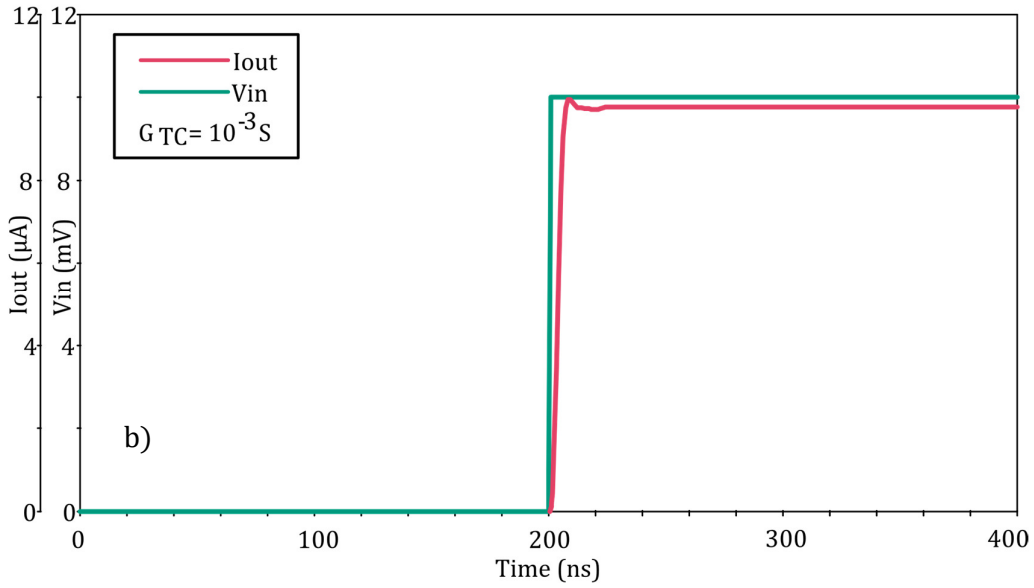
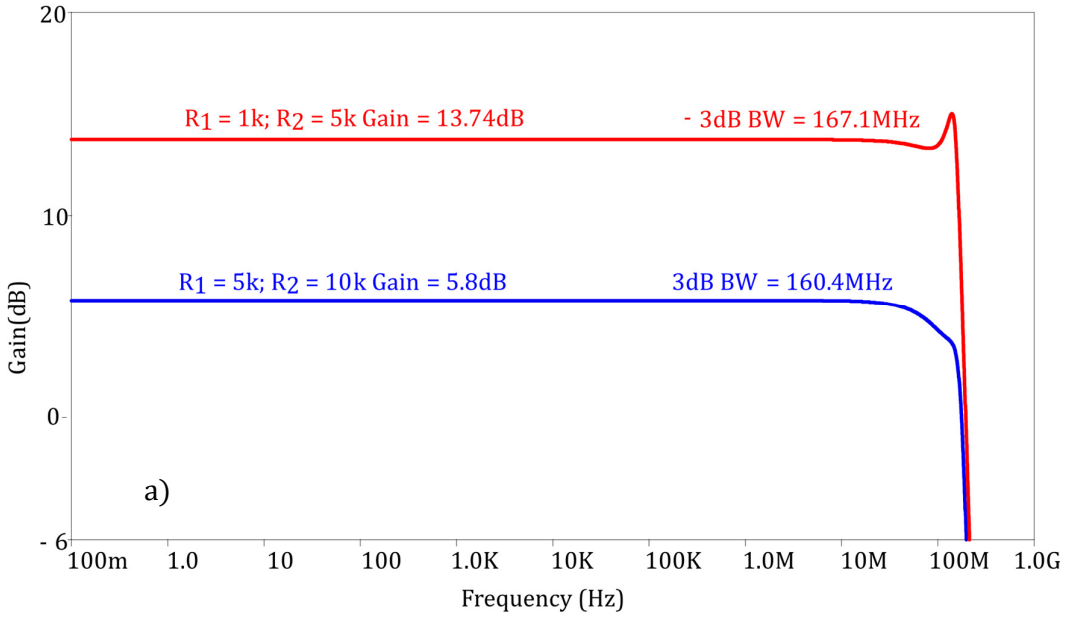


Figure 6.32 VCII based V-to-I converter a) frequency performance and b) step response to a voltage step input with amplitude of 10mV.



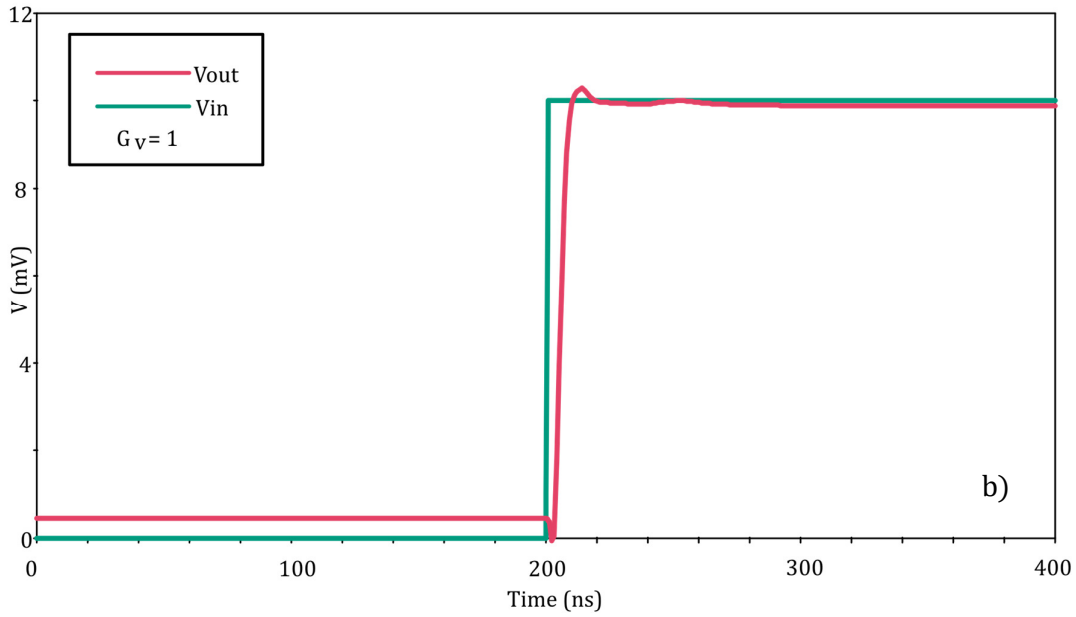


Figure 6.33 VCII based voltage amplifier a) frequency performance and b) step response to a voltage step input of 10mV.

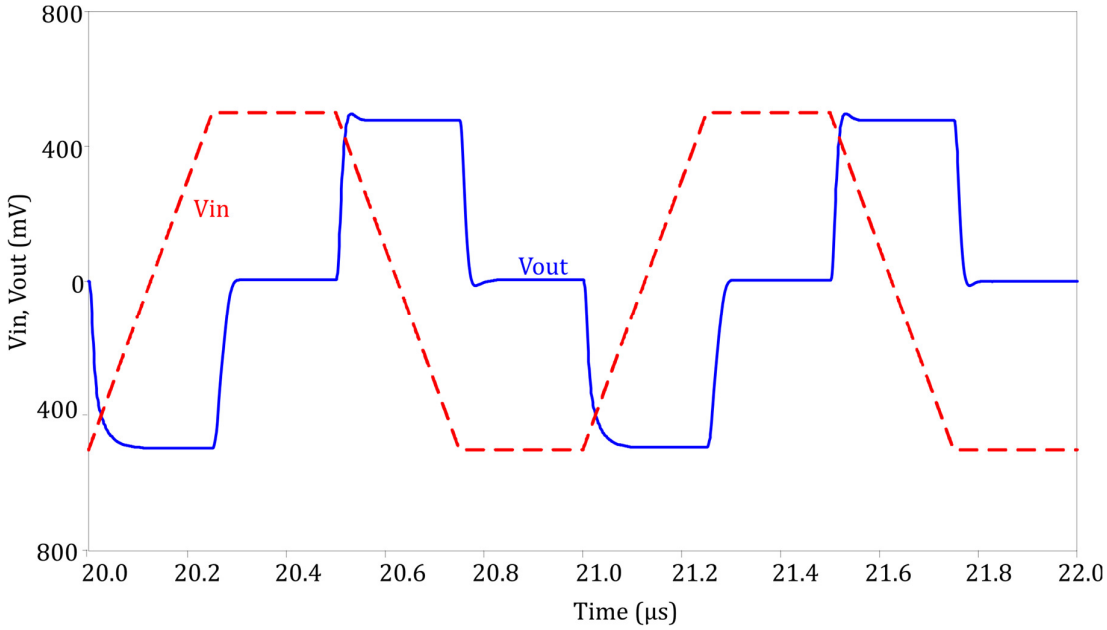


Figure 6.34 Time Domain Response of VCII based voltage differentiator.

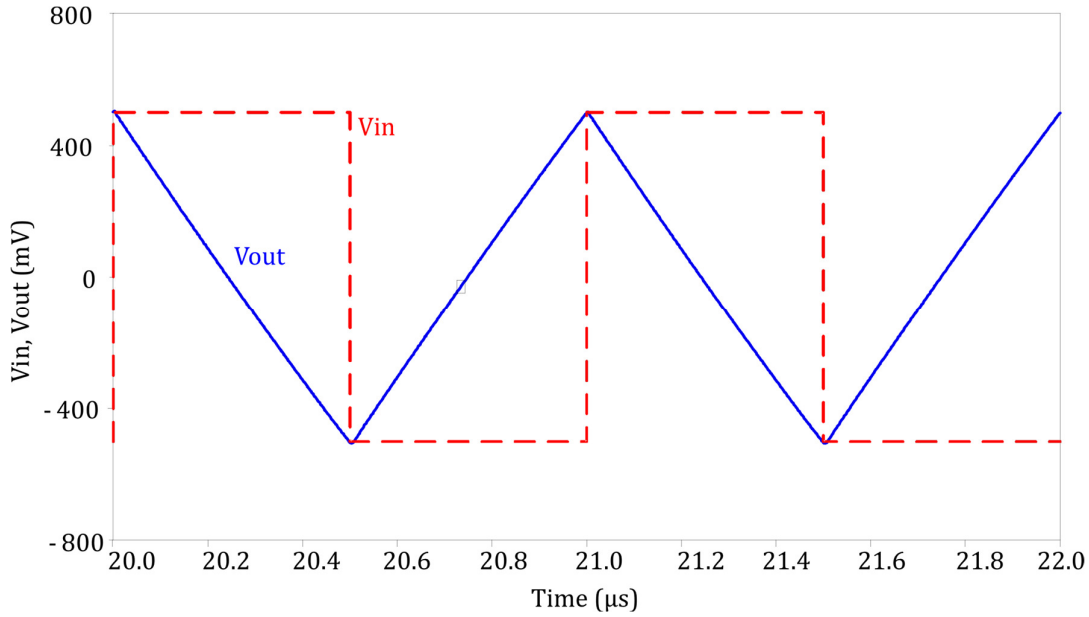


Figure 6.35 Time Domain Response of VCII based voltage integrator.

6.2.4 Flipped Voltage Follower based VCII

6.2.4.1 Design

Fig. 6.36 shows how we have implemented a flipped voltage follower [102-103] based VCII. The Y branch of the VCII is implemented by means of an AB-class super common-gate cell formed by M_1-M_6 together with current sources I_{B1} and I_{B2}. The local negative feedback performed by the differential pair M_1, M_2 and by M_5, fixes to ground the voltage at Y helping to lower the impedance at the same node. Transistors M_6 and M_7 implement a simple current mirror to make sure that the current forced into the Y terminal is suitably mirrored to the X terminal.

The low input impedance at the Y port can be therefore approximatively evaluated as:

$$r_Y \cong \frac{1}{gm_5 gm_2 (R_{ds2} // R_{ds4})} \qquad (6.26)$$

The high impedance at the X node is ensured by the presence of the drain of M_7 together with the current source I_{B3} (which can be implemented with a simple current mirror).

*The work presented in this section was published by the authors in [101].

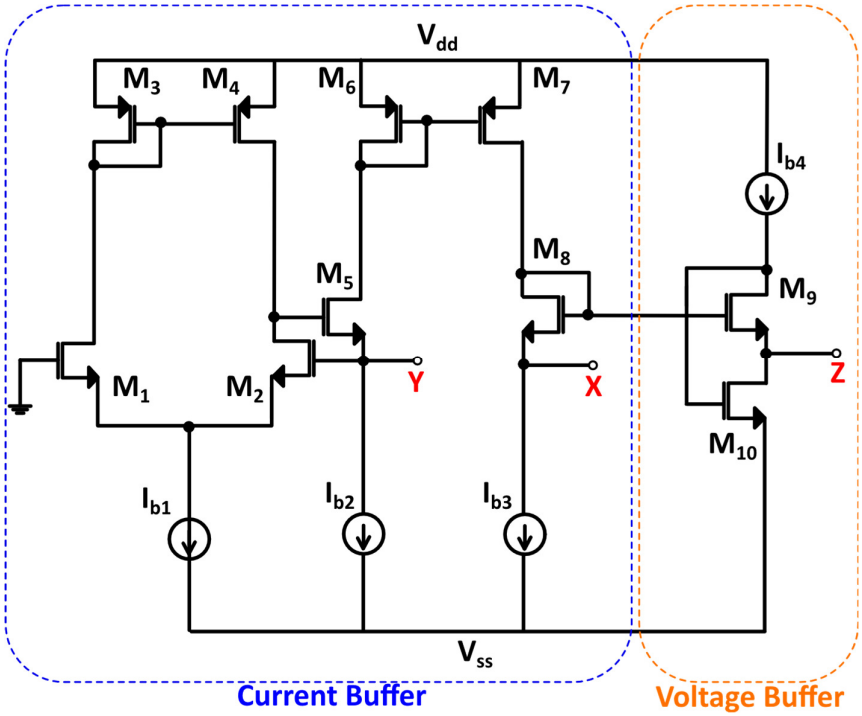


Figure 6.36 Flipped voltage follower based VCII architecture [101].

Indeed, it can be calculated as:

$$r_X = \frac{R_{ds7} + R_{ds8} + gm_8 R_{ds8} R_{ds7}}{1 + gm_8 R_{ds8}} // R_{OIb3} \cong R_{ds7} // Ro_{Ib3} \qquad (6.27)$$

M8 acts as a level shifter to properly adjust the DC value at the input of the FVF voltage buffer. Since it constitutes the Z output node, the impedance at this terminal can be easily evaluated as:

$$r_Z \cong \frac{1}{gm_9 gm_{10} R_{ds9}} \qquad (6.28)$$

6.2.4.2 Simulation results and application

The VCII circuit is simulated using 0.35μm CMOS parameters and supply voltage of ±1.65V. The used transistors aspect ratios are reported in Table XXIX. The important parameters of the VCII are also summarized in Table XXX. As it is seen, the circuit provides voltage and current gains very close to unity, low input impedances at Y and Z terminals and a high impedance at X terminal.

Table XXIX Transistors aspect ratios

Transistor	Width	Length
$M_{1/2}$	21μm	0.35μm
$M_{3/4}$	4.2μm	0.35μm
M_5	7μm	0.35μm
$M_{6/7}$	72.8μm	4.6μm
$M_{8/9}$	28.7μm	1.4μm
M_{10}	14μm	52μm
Bias Current	**Value**	
I_{B1}	30μA	
$I_{B2/B3/B4}$	40μA	

Table XXX VCII performance parameters

Parameter	Value
Impedance at X node	802 kΩ
Impedance at Y node	49 Ω
Impedance at Z node	79 Ω
α (DC value, BW)	0.995, 340 MHz
β (DC value, BW)	0.996, 14.6 MHz
Static Power Consumption	700 μW

To prove the effectiveness of the proposed VCII, we have utilized it in a current mode Wheatstone bridge configuration (CMWB). Such a structure [104-106] (Fig. 6.37) is typically used to read the variations of a resistive sensor and is made of only two resistors (one fixed and one variable or both variable) excited by a current source (unlike its voltage mode counterpart, where four resistors and a voltage source are needed).

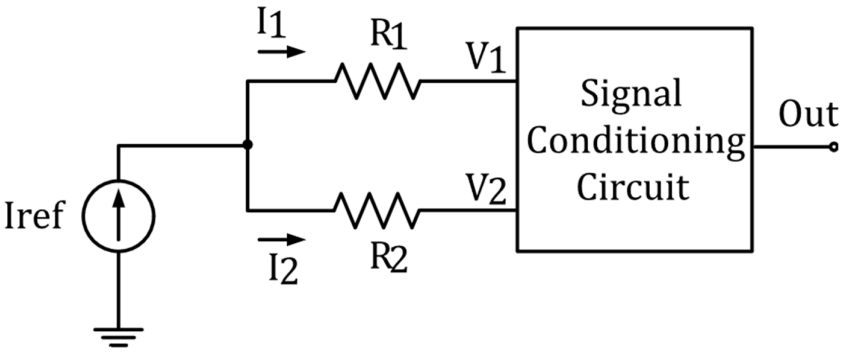


Figure 6.37 Current Mode Wheatstone bridge

CMWBs are generally used because they offer the typical advantages of current mode signal processing such as higher bandwidth, larger dynamic range, simpler circuitry etc. [105]. In a CMWB, referring to Fig. 6.37, the resistors are connected at one end and are forced to have equal and constant voltage (V_c) at the other end. Therefore, the signal conditioning circuit has to be designed so to fulfill the following conditions:

$$\boldsymbol{V_1 = V_2 = V_c} \tag{6.29}$$

$$\boldsymbol{I_{ref} = I_1 + I_2} \tag{6.30}$$

Since the resistors behave like parallel resistors, in the CMWB of Fig. 6.37, I_1 and I_2 can be expressed as:

$$\boldsymbol{I_1 = \frac{R_2}{R_1 + R_2} I_{ref};\ I_2 = \frac{R_1}{R_1 + R_2} I_{ref}} \tag{6.31}$$

By assuming $R_1=R_0\pm\Delta R$ and $R_2=R_0\mp\Delta R$, the signal conditioning circuit is used to produce an output signal proportional to the difference between I_1 and I_2:

$$\boldsymbol{I_1 - I_2 = \Delta I = \pm \frac{\Delta R}{R_0} I_{ref}} \tag{6.32}$$

Therefore, any variation in the value of resistors can be measured. However, in case of one sensor applications where $R_1=R_0\pm\Delta R$ and $R_2=R_0$, Eq. 6.32 will be a nonlinear function of ΔR. This limitation can be solved with the adoption of a VCII network as signal conditioning circuit. We propose two solutions, one for a two variable resistors configuration (Fig. 6.38a) and the other for a linear readout of a single resistor configuration (Fig. 6.38b). In both cases, the gain resistor is implemented by means of a voltage controlled element shown in Fig. 6.38c [107].

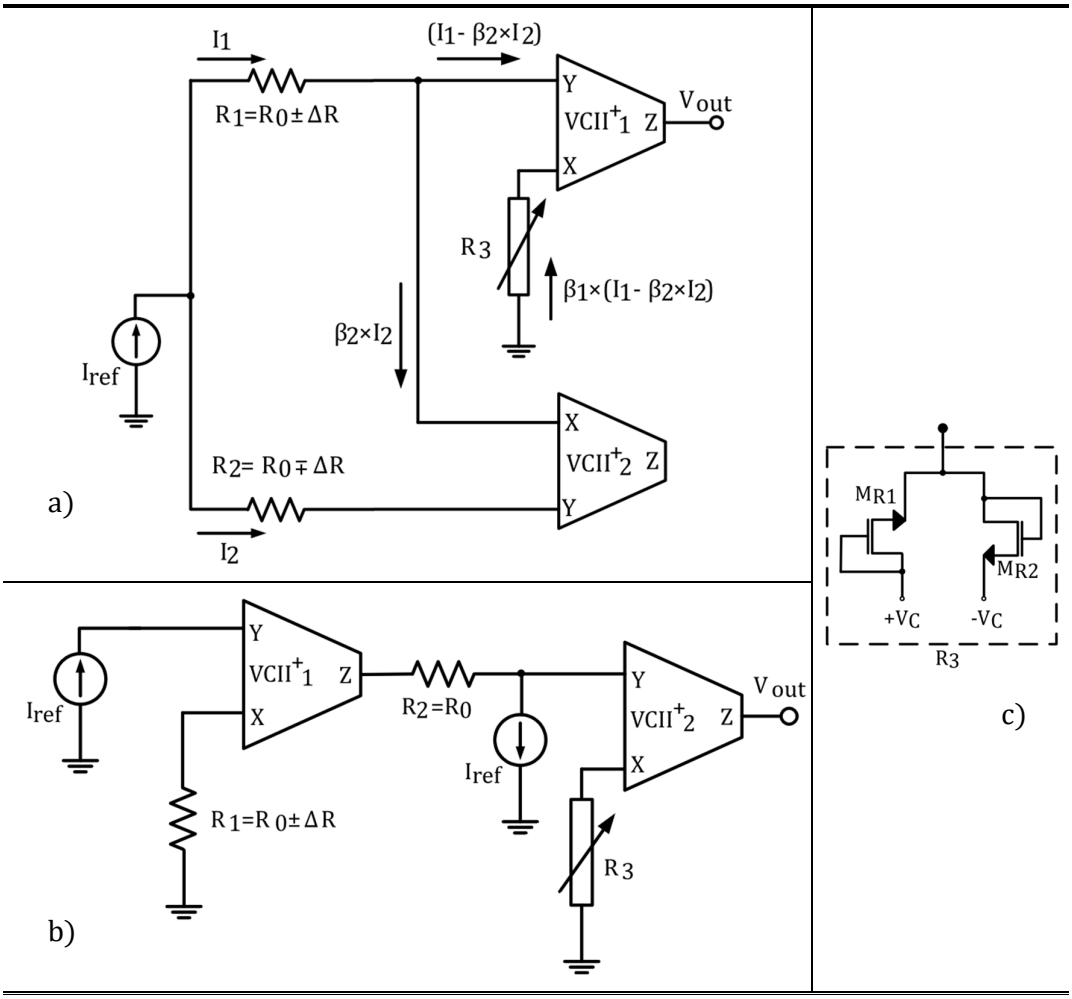


Figure 6.38 Proposed VCII based CMWB configuration for a) two sensors applications and b) single sensor applications; c) implementation of variable resistor R_3 [107].

The first proposed CMWB, designed for two sensor applications (Fig. 6.38a), consists of two VCIIs and one variable resistor. The X output of $VCII_2$ is directly connected to the Y input of $VCII_1$ to make a current subtraction node. Performing KCL analysis at Y input of $VCII_1$, it results:

$$\boldsymbol{I_{Y1} = I_1 - \beta_2 I_2} \qquad \textbf{(6.33)}$$

where I_{Y1} is the input current to Y port of $VCII_1$. As a result of the current following action between Y and X terminals of VCII, I_{Y1} is transferred to X port of $VCII_1$ and converted to a proportional voltage by R_3 expressed by:

$$\boldsymbol{V_{X1} = \beta_1 (I_1 - \beta_2 I_2) R_3} \qquad \textbf{(6.34)}$$

where β_1 is the current gain between Y and X terminals of $VCII_1$. The voltage following action between X and Z terminals of $VCII_1$ (with gain of α_1) results the output voltage as:

$$\boldsymbol{V_{out} = \beta_1(I_1 - \beta_2 I_2)\alpha_1 R_3} \quad \textbf{(6.35)}$$

In Eq. 6.35, β_1, β_2 and α_1 are defined as:

$$\boldsymbol{\beta_1 = 1 \pm \varepsilon_1;\ \beta_2 = 1 \pm \varepsilon_2;\ \alpha_1 = 1 \pm \varepsilon_3} \quad \textbf{(6.36)}$$

where ε_1, ε_2, $\varepsilon_3 << 1$ are error terms. For $R_1=R_2$, input currents are common mode currents $I_1=I_2=I_{ref}/2=I_{cm}$ and using Eq. 6.35 the (common mode) output voltage is:

$$\boldsymbol{V_{outc} \cong \varepsilon_2 \alpha_1 R_3 I_{cm}} \quad \textbf{(6.37)}$$

According to Eq. 6.37, in the case that there is no change in R_1 and R_2, due to low value of ε_2, a negligible output voltage is produced. The input currents for a change of $\pm\Delta R$ in R_1 and $\mp\Delta R$ in R_2 are:

$$\boldsymbol{I_1 = \frac{R_0 \mp \Delta R}{R_1 + R_2} I_{ref};\ I_2 = \frac{R_0 \pm \Delta R}{R_1 + R_2} I_{ref}} \quad \textbf{(6.38)}$$

Inserting Eq. 6.38 into Eq. 6.35 gives the output voltage as:

$$\boldsymbol{V_{outd} = \frac{\varepsilon_2 R_0 \pm 2\Delta R}{R_1 + R_2} \alpha_1 R_3 I_{ref} \cong \frac{\pm \Delta R}{R_0} \alpha_1 R_3 I_{ref}} \quad \textbf{(6.39)}$$

According to Eq. 6.39, if β_2 is made very close to unity, that is $\varepsilon_2<<1$, it is possible to obtain a linear relationship between ΔR and V_{out}. However, in case only one sensor is used i.e. $R_1= R_0\pm\Delta R$ and $R_2=R_0$, Eq. 6.35, like previously stated, is a nonlinear function of ΔR.

The second proposed circuit is suitable for one sensor applications and is shown in Fig. 6.38b. It exhibits a linear relationship between output voltage and ΔR. In this circuit R_1 is varying sensor, R_2 is constant with value equal to R_0 and R_3 is variable resistor. A simple analysis gives:

$$\boldsymbol{V_{out} = \left(\frac{\beta_1 \alpha_1 R_1}{R_2} - 1\right) I_{ref} \alpha_2 \beta_2 R_3} \quad \textbf{(6.40)}$$

By inserting $R_2=R_0$ and $R_1=R_0\pm\Delta R$ into Eq. 6.40, we have:

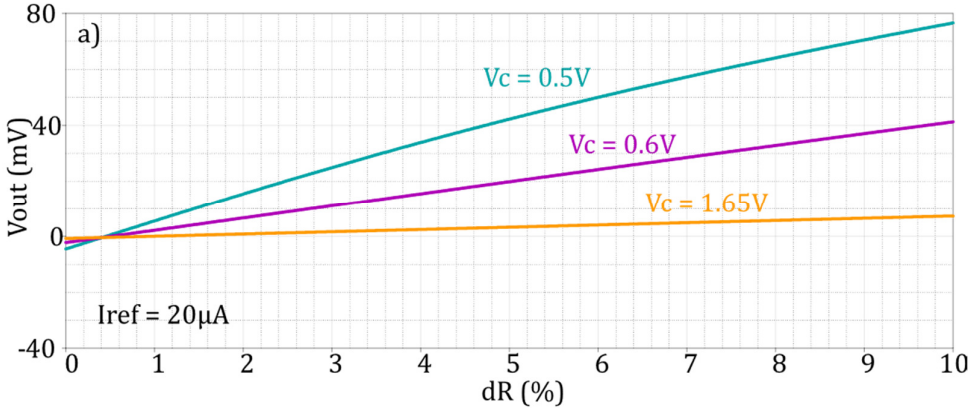
$$\boldsymbol{V_{out} = (\beta_1 \alpha_1 - 1)\alpha_2 \beta_2 R_3 I_{ref} + \frac{\pm \Delta R}{R_0} \alpha_2 \beta_2 R_3 I_{ref}} \quad \textbf{(6.41)}$$

The first term in Eq. 6.41 is an offset voltage which is negligible because the condition $\beta_1\alpha_1 = 1$ is always met. The second term is a linear function of ΔR controllable by R_3.

About the variable resistor shown in Fig. 6.38c, it is based on two nMOS. Its value can be changed by control voltages V_C and $-V_C$. The equivalent resistance is expressed as [107]:

$$\boldsymbol{R_3 = \frac{L}{2\mu C_{ox} W(V_C - V_{TH})}} \qquad \textbf{(6.42)}$$

Simulation results of the two interfaces are shown below. DC characteristics of the circuits of Fig. 6.38a-b are shown in Fig. 6.39a-b for three values of control voltage V_C=0.5V, 0.6V, 1.65V and setting R_1=10kΩ and different values of R_2. As it is seen, for R_1=R_2=10kΩ, the circuit shows negligible offset at output caused by VCII α parameter being slightly different from unity. Moreover, it shows a linear response. Fig. 6.40a-b shows differential mode performances of the proposed circuits where R_1=10kΩ and R=20kΩ and for different values of control voltages which shows variable gain with a -3dB bandwidth of 33MHz for the first topology and 6MHz for the second one. Circuits gain variation against different temperatures with R_1=10kΩ and R_2=20kΩ are shown in Fig. 6.41a-b. The result of Fig. 6.41a-b proves robust performance against temperature variation and suitability of the proposed circuits for temperature measurements applications. The output impedances of the proposed circuits are 79Ω. The power consumption of the circuits is 1.437mW and 1.436mW for V_C=0.5V and V_C=0.9V respectively, showing a negligible variation in power consumption for different values of gain.



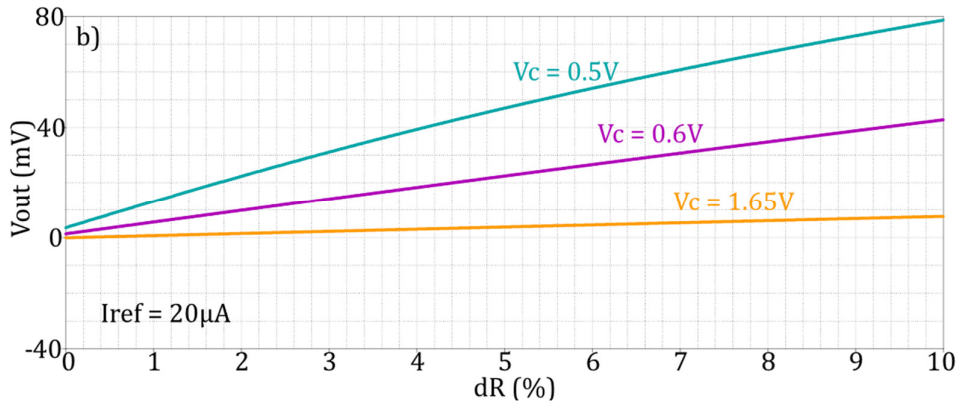


Figure 6.39 DC response of the proposed CMWB of a) Fig. 6.38a b) Fig. 6.38b.

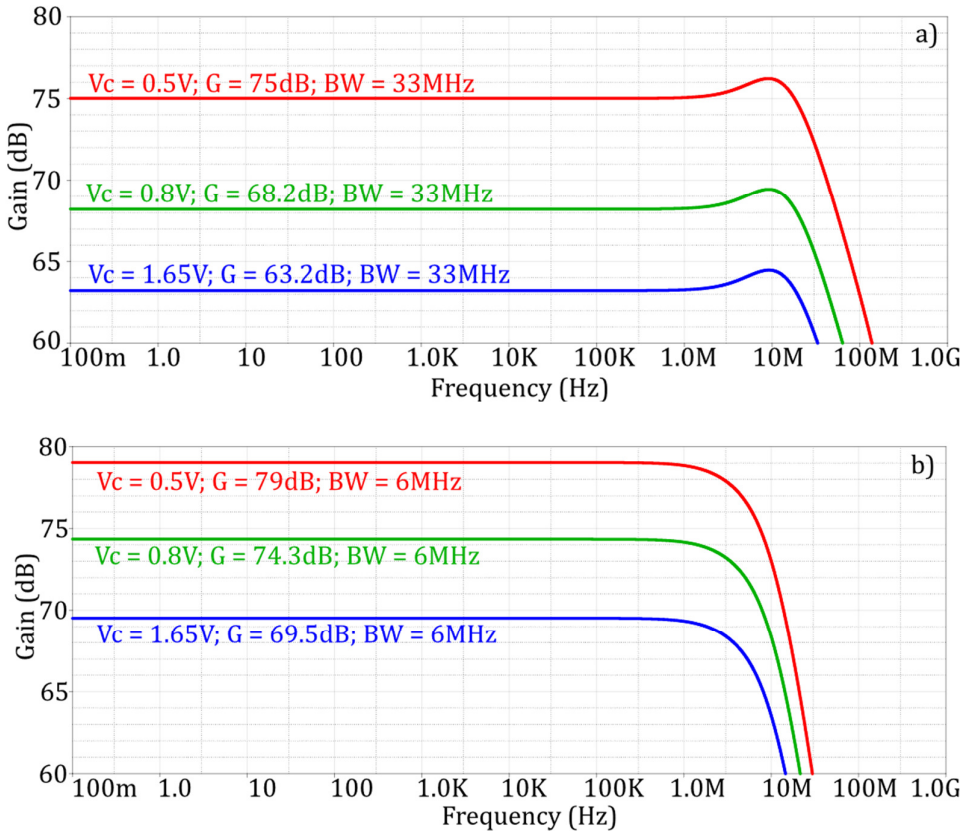


Figure 6.40 Differential mode frequency response of the proposed CMWB of a) Fig. 6.38a b) Fig. 6.38b.

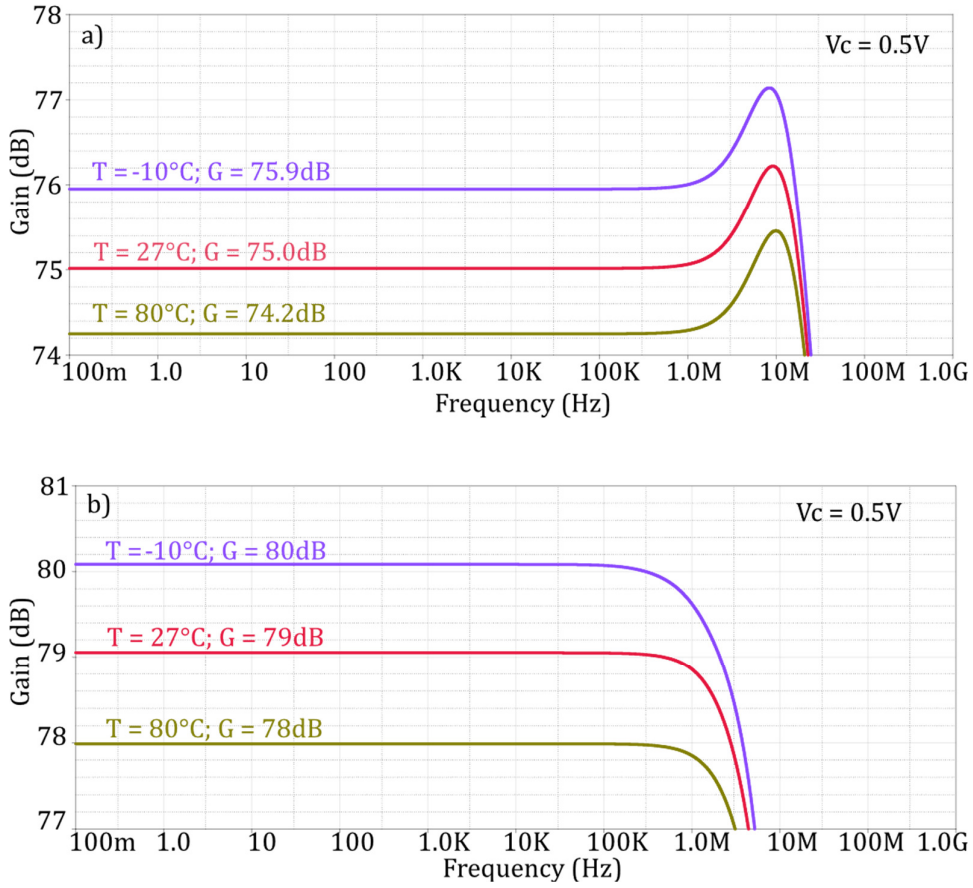


Figure 6.41 Differential mode response of the proposed CMWBs of a) Fig. 6.38a b) Fig. 6.38b with R1=10 kΩ and R2=20 kΩ at different temperatures.

6.2.4.3 Discussion

In this section, a novel architecture implementing a second generation voltage conveyor (VCII) has been proposed. Along with it, in order to test its capabilities and the benefits coming from such an active device, two new current mode Wheatstone bridge (CMWB) topologies based on VCII are presented as well. The proposed circuits employ two VCIIs as active elements and one active resistor made of two nMOS transistors. Simulation results acknowledge both the good behavior of the VCII itself, as well as the advantages coming from their employment as active devices of a CMWB: intrinsically linear input output relationship, resistor-free structure, electronically variable gain and suitability for practical applications due to very low output impedance.

6.2.5 Class AB high drive capable VCII

In this section, we will introduce the design of a class AB biased VCII based on a modified class AB flipped voltage follower (FVF). Due to its biasing conditions, the main feature of this device is to be able to drive large capacitive loads, being able to source and sink currents much greater than the biasing one.

6.2.5.1 Design

Fig. 6.42 shows the class AB biased VCII under analysis. It is based on a modified FVF structure and aims to achieve a high drive capability, meaning that is able to source and sink large amount of currents needed for instance during transient evolution of a large capacitive load.

The modified class AB FVF which constitutes the main structure of the VCII under analysis is shown in Fig. 6.43. Transistors *M5*-*M6*, together with *M1,* form a negative feedback loop. The combination of *M1*, *M5*-*M6* operate as a super transistor and with a proper design, frequency compensation is not required for the aforementioned local feedback loop. For low magnitude load currents, when, in other words, the FVF negative feedback loop formed by *M2* -*M4* is active, the output impedance is reduced by the cooperation of both *M1*, *M5* -*M6* transistors and *M2* -*M4* transistors loops. In this regard, it is possible to calculate the output impedance of such a structure, which corresponds also to the Y terminal input impedance of the VCII of Fig. 6.42:

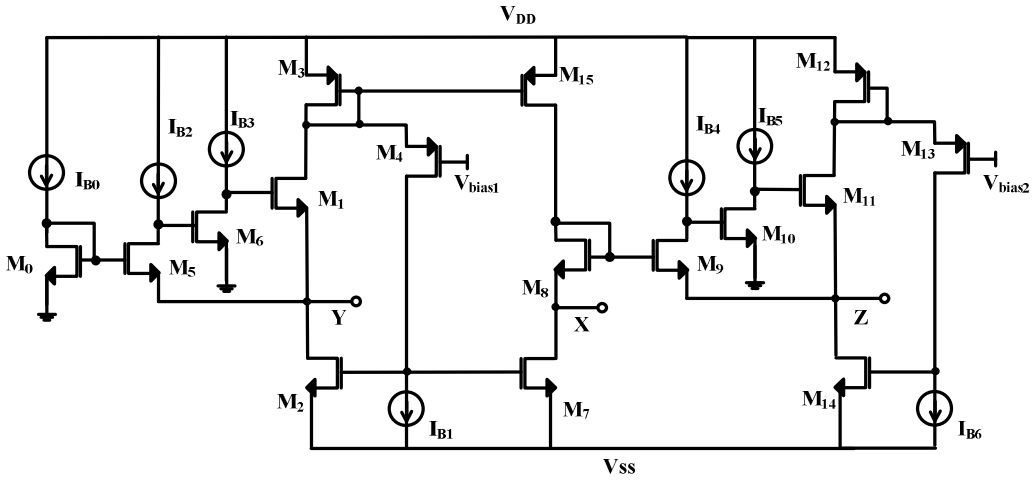


Figure 6.42 Class AB high drive VCII architecture [108].

*The work presented in this section was published by the authors in [108].

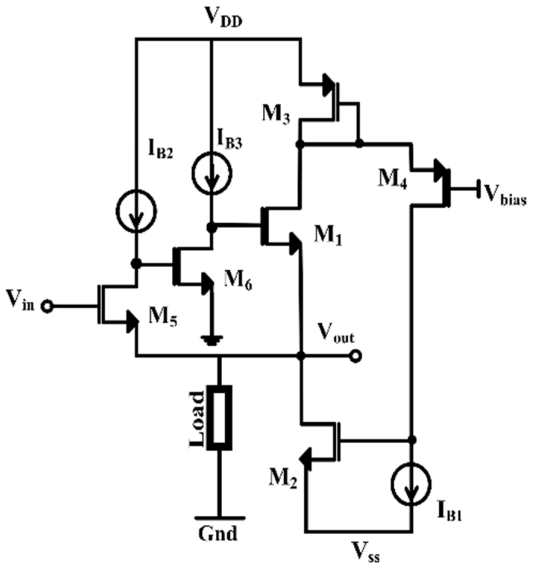


Figure 6.43 Modified class AB FVF cell [108].

$$r_{out} = r_{Y,low} \approx \frac{\left(1 + gm_3/gm_4\right)}{gm_1 gm_5 gm_6 gm_2 (ro_5 \| ro_{IB2})(ro_6 \| ro_{IB3}) R_{eq}} \tag{6.43}$$

where R_{eq} is the equivalent resistance seen at gate of M_2 expressed as:

$$R_{eq} = ro_{IB1} \| \left[ro_4 \left(1 + \frac{gm_4}{gm_3}\right)\right] \tag{6.44}$$

Parameters gm_i and ro_i denote, respectively the transconductance and output resistance of the corresponding transistor and ro_{IBi}, similarly, indicates the output resistance of the related current source. Even for large load currents, where M_2 is off and the FVF negative feedback loop does not operate, the added local negative feedback loop provides low output impedance. In this case, the output resistance still exhibits low value of:

$$r_{out} = r_{Y,high} \approx \frac{1}{gm_1 gm_5 gm_6 (ro_5 \| ro_{IB2})(ro_6 \| ro_{IB3})} \tag{6.45}$$

That is the reason why the VCII that operates with this basic modified class AB FVF, is able to ensure high current drive and low output impedance for both current source and sink phases.

The proposed VCII shown in Fig. 6.42 uses two class AB FVF circuits, one for the Y stage and another one for the Z stage. Transistors M_0-M_8 act as current buffer which

is obtained by connecting the input port of the relative FVF to ground. Transistor M_0 is added to adjust the DC offset voltage at Y terminal making sure that is equal to zero. Transistors M_9-M_{14} form the voltage buffer between X and Z terminals employing another class AB FVF circuit. The diode connected transistor M_8 operates as level shifter to compensate the effect of gate-source voltage of M_{12} at Z port. The resistance at X and Z terminals are expressed as:

$$r_X = \frac{ro_{15} + ro_8 + gm_8 ro_8 ro_{15}}{1 + gm_8 ro_8} \| ro_7 \approx ro_{15} \| ro_7 \tag{6.46}$$

$$r_Z \approx \frac{1 + \frac{gm_{12}}{gm_{13}}}{gm_9 gm_{10} gm_{11} gm_{14} (ro_9 \| ro_{IB4})(ro_{10} \| ro_{IB5}) R'_{eq}} \tag{6.47}$$

where:

$$R'_{eq} = ro_{IB6} || \left[ro_{13} \left(1 + \frac{gm_{13}}{gm_{12}} \right) \right] \tag{6.48}$$

And, again, gm_i and ro_i are the transconductance and output resistance of the related transistors, whereas ro_{IBi} represents the output resistance of the related current source. The bias voltages V_{bias1} and V_{bias2} can be set equal to V_{dd} -$2V_{sg}$.

6.2.5.2 Simulation results

The proposed class AB VCII circuit is simulated using PSpice and 0.35μm CMOS parameters and supply voltage of ±1.65V.

Transistor aspect ratios are reported in Table XXXI. Biasing currents are set as follows: $I_{B0}, I_{B1}, I_{B5} = 10\mu A$; $I_{B1}, I_{B2}, I_{B4}, I_{B6} = 5\mu A$; $I_{B3} = 17\mu A$. Biasing voltages $V_{bias1,2}$ are equal to 315mV.

To test the transient response of the proposed class AB VCII, a step input of ±2mA is applied to the Y terminal. The X terminal is connected to a load of 1Ω. The resulting current at X terminal is shown in Fig. 6.44. The positive and negative slew rates of the circuit are 510mA/μs and 860mA/μs respectively. From these results, the proposed circuit is able to source and sink a high current of 2mA to and from the load. Since the bias current of transistors M_7, M_8 is only 17μA, the current drive capability of the proposed FVF is at least 117.6 times larger than bias current.

Table XXXI Transistors aspect ratios

Transistor	*W(μm), L(μm)*	*Transistor*	*W(μm), L(μm)*
M_1, M_{11}	120.05, 0.35	M_5	3.15, 0.7
M_2, M_7, M_8	70, 0.7	M_6, M_{10}	20.3, 0.35
M_3, M_{12}, M_{15}	120.05, 0.7	M_9	31.5, 0.7
M_4, M_{13}	21, 0.35	M_0	21, 4.2

The circuit also enjoys low settling time of 200ns worse. To test the current transfer linearity between Y and X terminals, a sinusoidal input current with peak-to-peak value of 1mA is applied to the Y node. The resulted output at X node is shown in Fig. 6.45. The current signal at X node shows a low THD of 1.68% (-35.5dB) determined at 1MHz considering 10 harmonics. The simulation is repeated by connecting two different loads of 1KΩ and 0.5KΩ to the X terminal. Results are again showed in Fig. 6.45. In these cases, the maximum current drive capability is slightly reduced due to the limitation caused by the available supply voltages. The achieved THDs are 2.48% (-32.11dB) and 1.96% (-34.15dB) for 1KΩ and 0.5KΩ loads respectively. Then, to test the performance of the proposed VCII in transferring voltage signals between X and Z terminals, a step input of ±500mV is applied to X node. The Z node is connected to a load of 5nF. The resulted output at Z node is shown in Fig. 6.46. The positive and negative slew rates are 0.56V/μs and 1.8V/μs respectively. The settling time is also 540ns. Linearity of the voltage buffering is also investigated. A 1V peak-to-peak sinusoidal voltage is applied to the X terminal and the voltage at Z is measured. The analysis is performed connecting to the Z node 1MΩ, 10kΩ and 5kΩ resistor loads. Results, depicted in Fig. 6.47, show that there is a negligible difference between traces at different load levels. The voltage signals at Z terminal show a THD of 2.32% (-33dB), 2.95% (-30.6dB) and 3.36% (-29.47dB) for each of the aforementioned resistor value. The noise performance at X and Z nodes is shown in Fig. 6.48 which are achieved by terminating these nodes to 5KΩ load. The impedances at Y, X and Z terminals are estimated as 2mΩ, 370kΩ and 2mΩ respectively (at 1kHz reference frequency). The frequency performance of voltage transfer gain between X and Z terminals and current transfer gain between Y and X

terminals are shown in Fig. 6.49. For this simulation, the X and Z terminals are connected to a load of 5pF||1kΩ. For current transferring between Y and X terminals, the DC gain and -3dB bandwidth are -0.115dB and 22.4MHz, respectively. For voltage transferring between X and Z terminals, the DC gain and -3dB bandwidth are -0.068dB and 220MHz, respectively. Due to the presence of PMOS current mirror in the current buffer section, the current transfer bandwidth is smaller than the voltage transfer bandwidth. These two parameters were also analysed at different PVT conditions, showing an overall maximum variation in the magnitude and bandwidth of only 0.5dB and 20MHz respectively. The static power dissipation, including the biasing circuitry needed to generate $V_{bias1,2}$, is only 320µW. The estimated area of the chip is about 381.5µm*197µm.

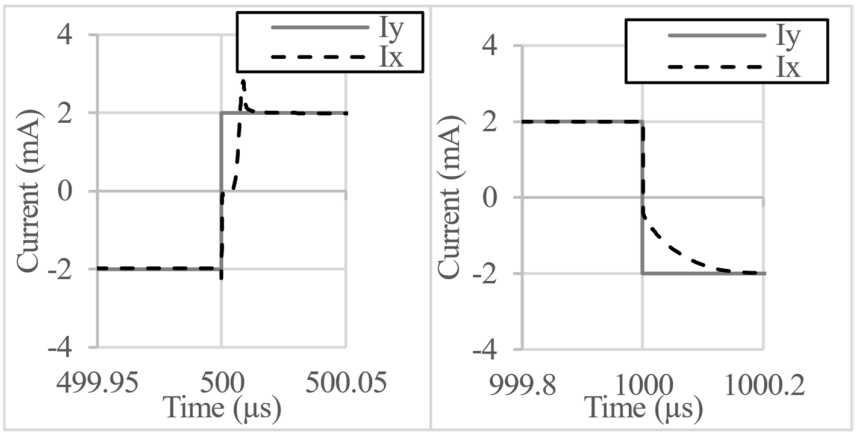


Figure 6.44 Y to X current transient response to a step input: focus on rising (left side) and falling (right side) edges.

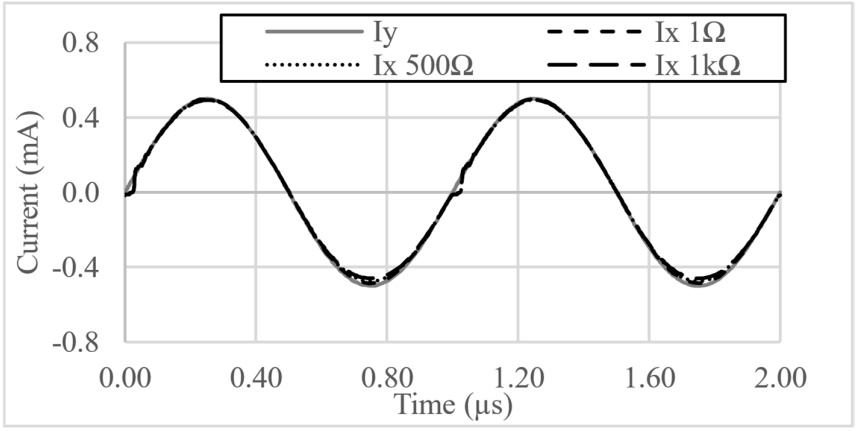


Figure 6.45 Y to X current transient response to a sinusoidal input.

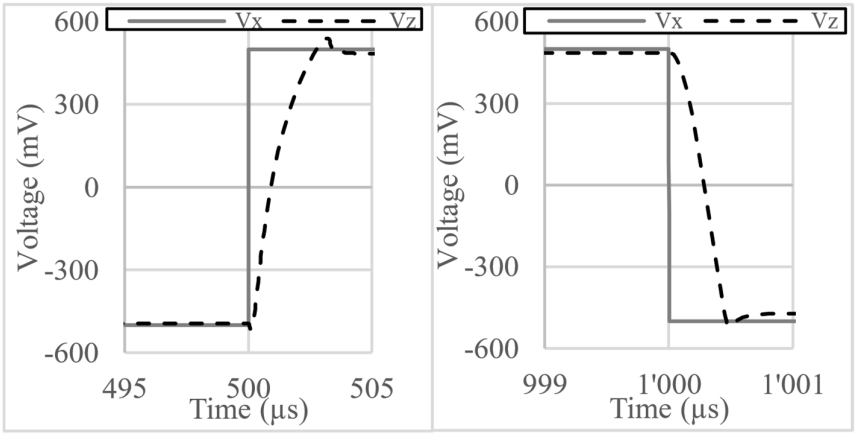


Figure 6.46 X to Z voltage transient response to a step input: focus on rising (left side) and falling (right side) edges.

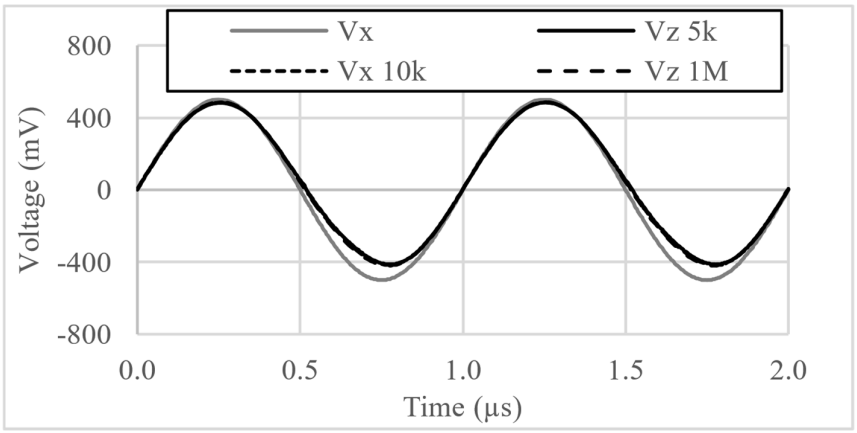


Figure 6.47 X to Z voltage transient response to a sinusoidal input.

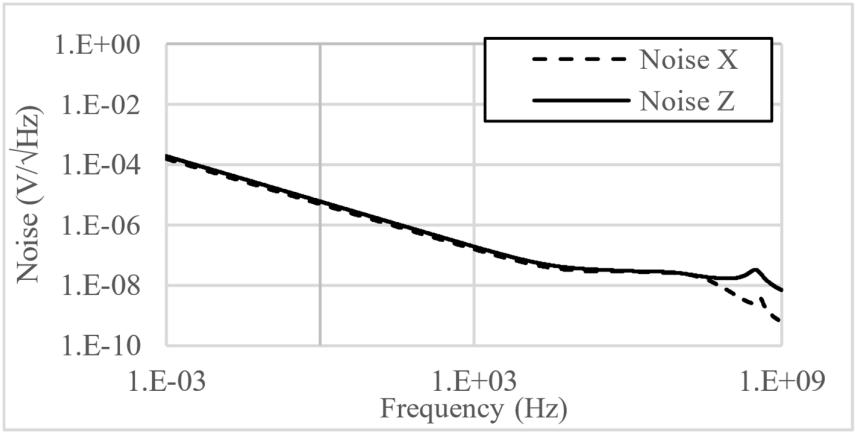


Figure 6.48 Noise performance of the proposed VCII at a) X b) Z.

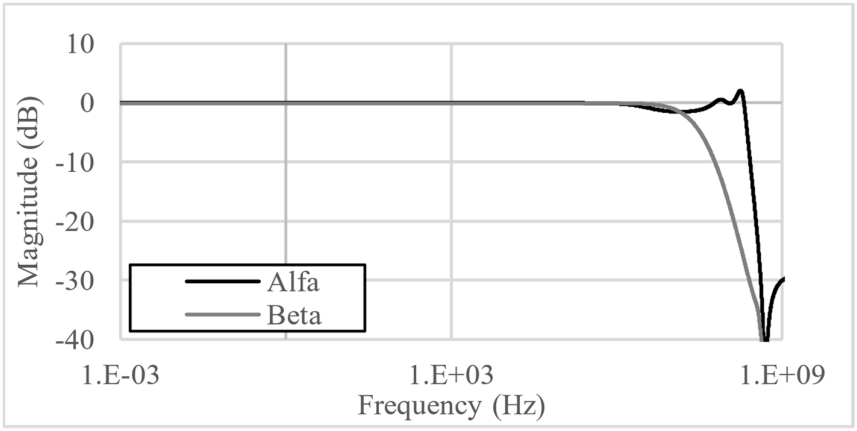


Figure 6.49 Frequency performance of the proposed VCII for β (current gain between Y and X) and α (voltage gain between X and Z).

6.2.5.3 Discussion

A new internal topology, at transistor level, has been here proposed. It takes the advantages of using flipped voltage followers to achieve good characteristics as accuracy, impedance level, current drive capability as acknowledged by the given simulation results.

6.2.6 Rail to rail VCII

In this final section, we are proposing yet another transistor level topology that enables the second generation voltage conveyor to achieve the full input and output voltage swings (at X and Z, in other words).

6.2.6.1 Design

The VCII topology is shown in Fig. 6.50. By using a rail to rail (RtR) voltage buffer, and a class AB biased input stage on the X terminal implements a fully RtR VCII device.

The current buffer that links the Y current input to the X current output is formed by transistors M_1–M_7 and the current sources I_{b1}–I_{b3}. Transistor M_3 in the common-gate configuration is biased by a voltage that is regulated by the negative feedback loop established by M_1–M_2, providing the virtual ground at the Y terminal also lowering its impedance.

*The work presented in this section was published by the authors in [109].

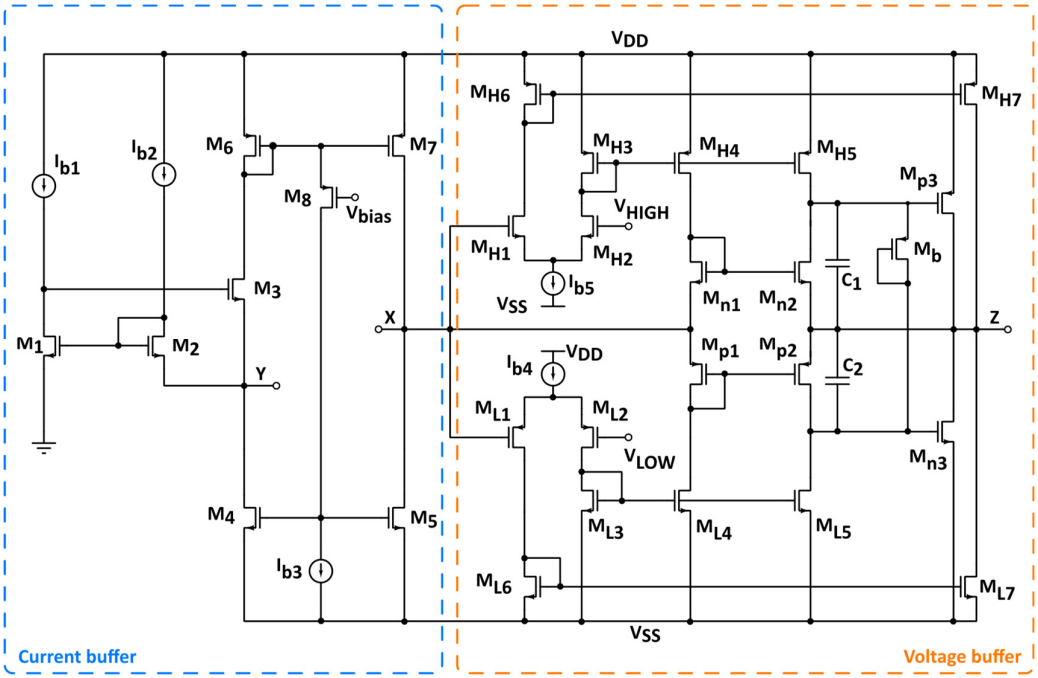


Figure 6.50 Rail to rail VCII architecture [109].

The voltage buffer implementation is based on a modified version of the standard class AB voltage follower [110]. PMOS M_{L1}–M_{L2} and NMOS M_{H1}–M_{H2} differential pairs drive a switching circuit that, based on the reference voltages V_{HIGH} and V_{LOW}, activate the correct portion of the buffer that is the standard voltage follower M_{n1}, M_{n2}, M_{p1}, M_{p2}, or the RtR pair M_{H7} and M_{L7}.

M_8 and I_{b3} fix the voltage at the drain of M_6. Then, it is possible to choose the gate voltage of M_8 (V_{bias}) to accurately tune the bias current of the Y and therefore the X terminals. Capacitors C_1 and C_2 are used to dampen the α parameter transfer function, ensuring the stability of the system. The impedances are derived using the small signal equivalent model depicted in Fig. 6.51. The impedance at the Y terminal is given by:

$$Z_Y \approx \frac{1}{gm_{M3}gm_{M1}(rds_{M1}//ro_{IB1})} \tag{6.49}$$

Transistors M_4–M_7 have the task of copying the input current (at Y) to the X terminal.

Since the current flowing at Y is mirrored on the class AB-biased branch formed M_5 and M_7, the voltage swing allowed at the X terminal is wide, even for high currents.

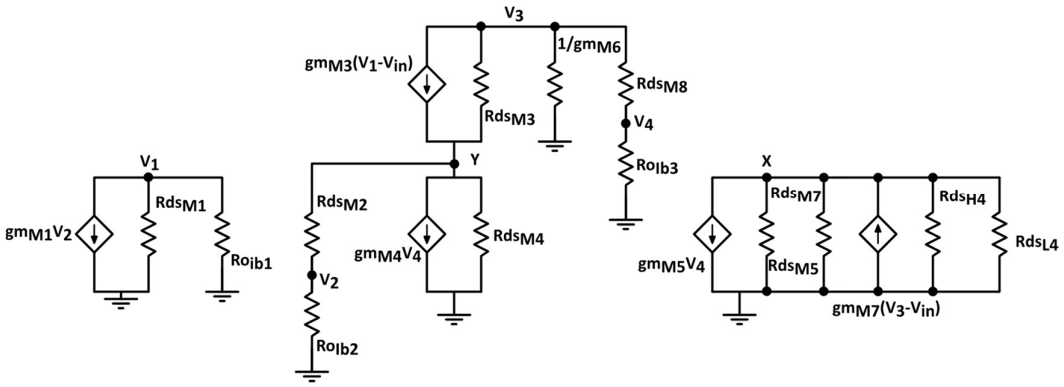


Figure 6.51 Small signal equivalent model of the RtR VCII architecture [109].

Precisely, it is given by:

$$\boldsymbol{Vss + Vds_{M5} \leq V_X \leq Vdd - Vsd_{M7}} \tag{6.50}$$

The total input impedance at the X terminal can be approximated as follows:

$$\boldsymbol{Z_X = Rds_{M5} // Rds_{M7}} \tag{6.51}$$

Concerning the voltage output Z terminal, the allowed voltage swing can be evaluated as:

$$\boldsymbol{Vss + Vds, sat_{ML7} \leq V_Z \leq Vdd - Vsd, sat_{MH7}} \tag{6.52}$$

Since the output stage changes shape according to the voltage level at the X port, the output impedance can be evaluated as [110]:

$$\boldsymbol{Z_Z \cong \begin{cases} \dfrac{Rds_{Mn3} Rds_{Mp3}}{Rds_{Mn3} + Rds_{Mp3} + (R_{k1} gm_{Mp3} Rds_{Mp3} + R_{k2} gm_{Mn3} Rds_{Mn3})} & if\ V_{LOW} < V_X < V_{HIGH} \\ \dfrac{1}{gm_{Mn3} gm_{mp2} Rds_{Mp2}} & if\ V_X > V_{HIGH} \\ \dfrac{1}{gm_{Mp3} gm_{mn2} Rds_{Mn2}} & if\ V_X < V_{LOW} \end{cases}} \tag{6.53}$$

where R_{k1} and R_{k2} are equal to ($gm_{Mn2} R_{dsMn2} R_{dsMp3} // R_{dsMH5}$) and ($gm_{Mp2} R_{dsMp2} R_{dsMn3} // R_{dsML5}$), respectively.

6.2.6.2 Simulation results

Simulations have been performed having employed a 0.15 μm CMOS technology from LFoundry through the Spice simulator. Current sources have been implemented by means of simple current mirrors designed to provide a current of

5 μA. Transistor dimensions are shown in Table XXXII. For the proposed VCII, the two input voltages V_{HIGH} and V_{LOW} at the differential amplifiers of the voltage buffer stage are set to +0.3 V and -0.35 V respectively, while supply voltages are ±0.9 V. The voltage V_{bias} has been set to -0.3 V in order to ensure a 10 μA bias current through Y and X branches.

Table XXXII Transistor dimensions and parameter values

Transistor	Dimensions (W, L)
M_1, M_2, M_8	1.8 μm, 0.3 μm
M_3	2.4 μm, 0.3 μm
M_4, M_5, M_{H7}	30 μm, 0.3 μm
M_6, M_7, M_{L7}	60 μm, 0.3 μm
M_{H1}, M_{H2}	7.2 μm, 0.3 μm
M_{H3}, M_{H4}, M_{H5}, M_{H6}	3.6 μm, 0.3 μm
M_{L1}, M_{L2}	14.4 μm, 0.3 μm
M_{L3}, M_{L4}, M_{L5}, M_{L6}	2.85 μm, 0.9 μm
M_{p1}, M_{p2}	8.75 μm, 0.75 μm
M_{n1}, M_{n2}	2.85 μm, 0.75 μm
M_{p3}	4.5 μm, 0.75 μm
M_{n3}	1.35 μm, 0.75 μm
M_b	0.3 μm, 0.6 μm
Parameter	**Value**
I_{b1}, I_{b2}, I_{b3}, I_{b4}, I_{b5}	5 μA
V_{HIGH}	300 mV
V_{LOW}	-350 mV
V_{bias}	-300 mV
C_1, C_2	250 fF

M_b dimensions have been regulated so to have 10 μA flowing through M_{p3} and M_{n3}. In order to guarantee a high driving capability for the X node, the W/L ratio of M_4-M_5 and M_6-M_7 has been set to 100 and 200, respectively.

The rail-to-rail capabilities of this circuit are shown in Fig. 6.52 and Fig. 6.53 where the DC performances of α and β are shown. To evaluate the former parameter, an input voltage at X terminal swinging from negative supply voltage to positive supply voltage has been applied, while the output voltage at Z port has been determined at different load levels (50 kΩ, 20 kΩ, 10 kΩ). As visible, α remains always greater than 0.95 for input voltages greater than ±0.8 V. Analogously, performances of the β parameter have been investigated applying a current at Y port and monitoring the current at X port for different load levels. Fig. 6.53 acknowledges both the good driving capability of currents of 0.5 mA (50 times greater than the X branch bias current) and the good voltage swing at X, which reaches ±0.72 V with a current of ±0.5 mA over a load of 2 kΩ.

Frequency performances of the voltage conveyor are presented in Fig. 6.54 and Fig. 6.55. The bandwidth for the α parameter, evaluated with a 1 pF load connected at the output Z node, is equal to 55 MHz (Fig. 6.54). The β transfer function is shown in Fig. 6.55. The bandwidth is equal to 165 MHz.

Terminal impedance values have been also evaluated. The resulting values (see Fig. 6.56) are 522 kΩ, 23 Ω and 160 Ω at X, Y and Z respectively. To investigate the time domain behaviour of the VCII, a 1 MHz sine wave with a 0.8 V peak amplitude has been applied to the X terminal. The total harmonic distortion (THD) at the output (Z terminal) with a 1 pF, 10 kΩ parallel load, considering 10 harmonics, is equal to 2.4% (-32.4 dB). The same analysis has been repeated applying a 1 MHz sine wave with a 0.5 mA peak amplitude at the Y port. The X terminal has been connected to a 100 Ω load. The THD is equal to 1.1% (-39 dB).

To show the benefit of a dual input-output rail-to-rail stages, the circuit was tested in a transimpedance amplifier configuration (refer to Fig. 6.30a). A sinusoidal current on the input terminal Y with an amplitude of 0.5 mV was imposed and the output voltage at the X node was determined. The output was connected to a 1 pF capacitor in parallel to a 10 kΩ resistor. The gain resistor was set equal to 500 Ω and 1.5 kΩ to take advantage of the full X branch dynamic. Results are shown in Fig. 6.57,

acknowledging the capability of the circuit to reach a dynamic of the 80% of the supply voltage without distortions.

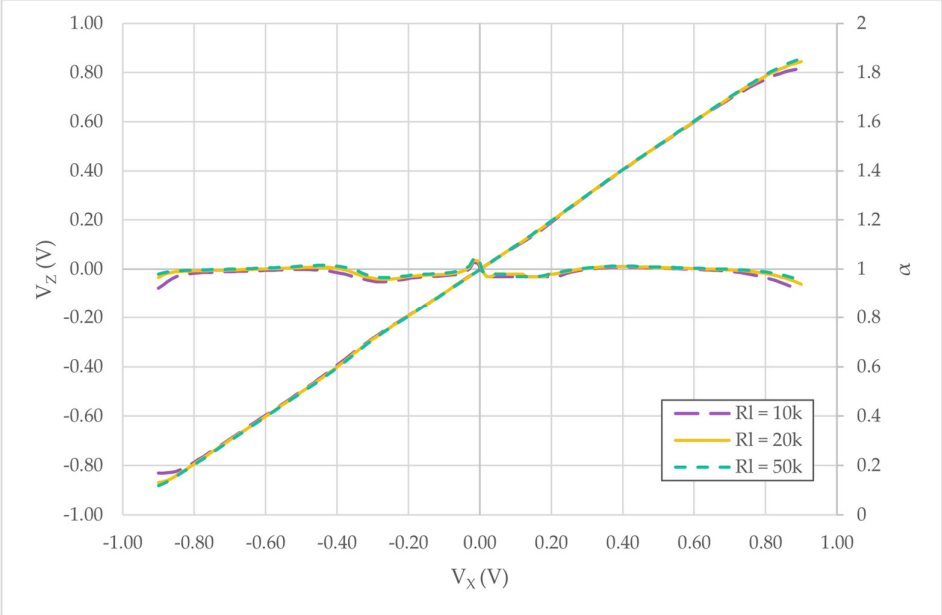


Figure 6.52 DC performances of the α parameter at different load levels connected to the Z node.

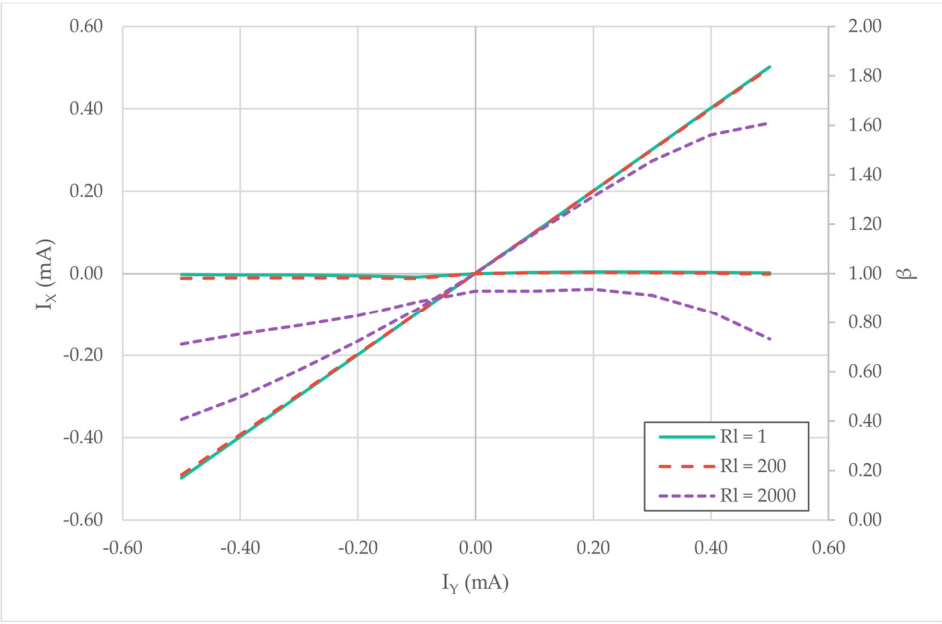


Figure 6.53 DC performances of the β parameter at different load levels connected to the X node.

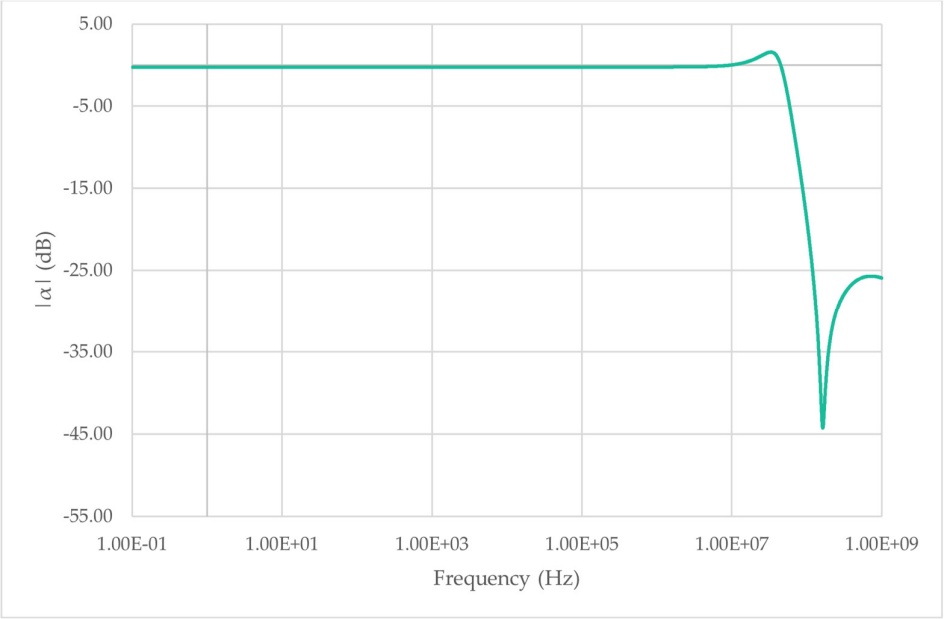


Figure 6.54 AC performances of the α parameter with a 1 pF capacitor connected to the Z node.

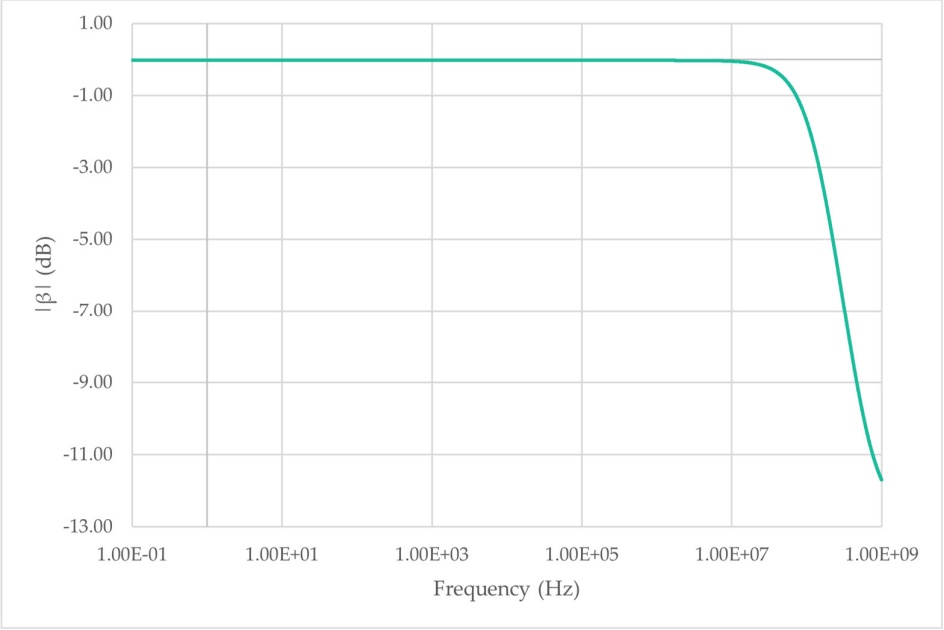


Figure 6.55 AC performances of the β parameter.

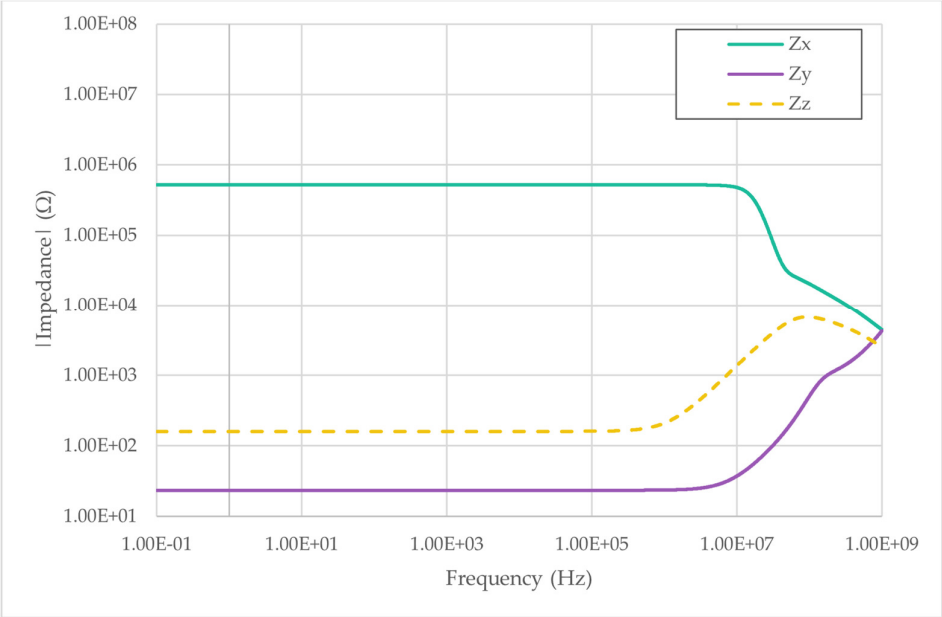


Figure 6.56 Proposed VCII terminal impedances.

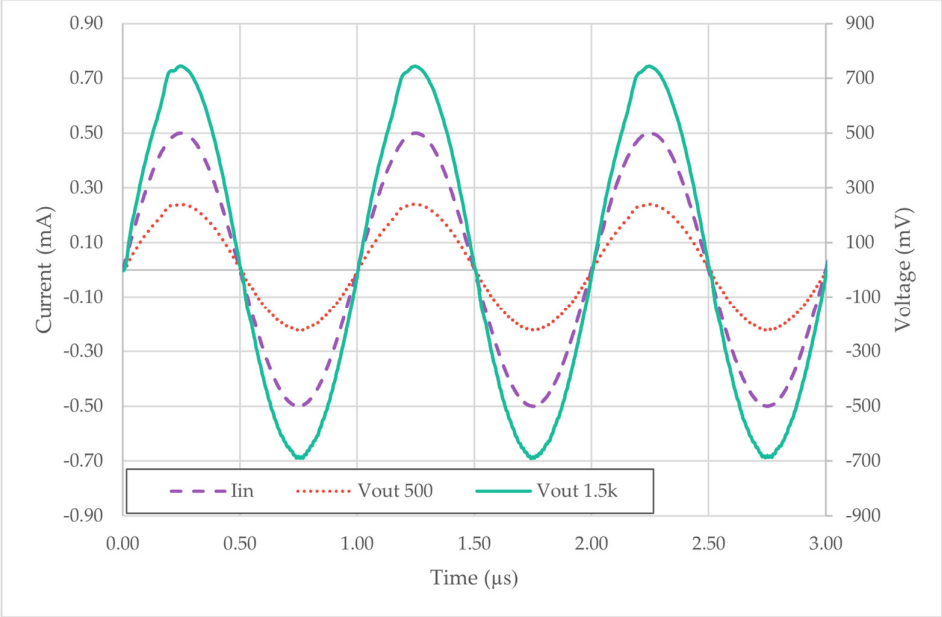


Figure 6.57 VCII used as a TIA.

Table XXXIII summarizes the circuit performance parameters comparing them with works presented in the previous sections as well as other manuscripts from the literature which, although not a specific VCII, propose a universal active device capable of being configured as VCII.

Table XXXIII The proposed VCII performance parameters.

Parameter	This section	Section 6.2.3	Section 6.2.5	[96], [111]	Section 6.2.4
Technology	LFoundry 0.15 µm	AMS 0.35 µm	AMS 0.35 µm	TSMC 0.35 µm	AMS 0.35 µm
Supply voltage	±0.9 V	±1.65 V	±1.65 V	±1.65V	±1.65 V
Impedance at X node	522 kΩ (@100 MHz)	1.2 MΩ	370kΩ	240kΩ	802kΩ
Impedance at Y node	23 Ω (@100 MHz)	6.7 Ω	2mΩ	650mΩ	49mΩ
Impedance at Z node	160 Ω (@100 MHz)	0.7 Ω	2mΩ	1.4Ω	79mΩ
α	-0.24 dB (@100 kHz)	-0.03 dB	-0.07 dB	0.32 dB	-0.04 dB
β	-0.03 dB (@100 kHz)	-0.1 dB	-0.115 dB		-0.04 dB
α bandwidth	55 MHz (1 pF load at Z)	217 MHz (unloaded)	220MHz (unloaded)	74 MHz	340MHz (unloaded)
β bandwidth	165 MHz	200 MHz	22.4 MHz	64MHz	14 MHz
V_Z THD	2.4% (-32.4 dB) (V_X = 1.6 V_{pp}; @1 MHz; 10 harm)	0.068% (-63 dB) (V_X = 1V_{pp}; @1 MHz; 10 harm)	2.48% (V_X = 1V_{pp}; @1 MHz; 10 harm)	2.7% (V_X = 1V_{pp})	N.A.
I_X THD	1.1% (-39 dB) (I_Y = 1 mA_{pp}; @1 MHz; 10 harm)	0.1% (-59 dB) (I_Y = 20 μA_{pp}; @1 MHz; 10 harm)	3.36% (I_Y = 1 mA_{pp}; @1 MHz; 10 harm)	N.A.	N.A.
Static Power Cons.	120 µW	330 µW	320µW	≅ 5mW	700µW
FOM	85	330	320	4950	874

The presented topology manages to achieve overall comparable performances with respect to the other circuits, while greatly improving the dynamic range of the voltage conveyor, as well as reducing its power consumption, as acknowledged by the figure of merit (FOM, in this case, lower is better) parameter in the same table. In this regard, the parameter is calculated as [112]:

$$\boldsymbol{FOM = \frac{V_{DD} + |V_{SS}|}{V_{in,pp\_max}} I[\mu A]} \qquad \textbf{(6.54)}$$

V_{in,pp_max} represents the maximum input peak-to-peak voltage that still allows to achieve acceptable linearity levels and is extracted from the THD evaluations. The parameter *I*, expressed in μA, allows to introduce in the FOM the power consumption of the circuit decoupling it from the actual supply voltage.

As still visible from Table XXXIII, the proposed topology links the current driving capabilities (at the Y terminal) of the one presented in Section 6.2.5 to the extended input dynamic range (at X and Z terminals). Unlike [96], moreover, where the authors make use of a universal active device, the presented architecture uniquely implements a second generation voltage conveyor, therefore largely reducing the overall power consumption.

6.2.6.3 Discussion

We have here presented a new CMOS VCII showing RtR voltage swing at X and Z ports. The dynamic biasing of the Y and X branches ensures a high driving capability at the X terminal with a low quiescent current. These two features, together, allow to achieve high transimpedance conversion gains even for relatively large currents. Simulation results have been given, effectively acknowledging the predicted behavior. A possible application scenario has been proposed for a transimpedance amplifier configuration.

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